

Mobility Model Analysis of on Resistance for InAlN/GaN Hybrid MOS HEMT

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ABSTRACT: GaN based devices have significant advantages in power density, thermal characteristics, and voltage range over those based on conventional compound semiconductors or Silicon. With GaN, materials systems there are significant advantages in cycle time and strength of design from use of TCAD. Since it is naturally normally-off, the hybrid InAlN/GaN MOS-HEMT has a remarkable potential for an advanced GaN-based power switch. Analysis of on resistance for InAlN/GaN hybrid MOS HEMT based on the mobility value is presented in this paper. The methodology presented here can aid the designers to understand the physics and electrically characterize of new generation GaN based devices. The models proposed here are implemented in TCAD simulation packages and studied.

KEYWORDS: Ron, mobility μ_{DEG} and μ_{MOS} , InAlN/GaN.

I. INTRODUCTION

The HEMT or High Electron Mobility Transistor is a form of field effect transistor (FET) that is used to provide very high levels of performance at microwave frequencies. It offers a combination of low noise figure combined with the capability to operate at the very high microwave frequencies. Accordingly the HEMT is used in areas of RF design where high performance is required at very high RF frequencies. The development of the HEMT took many years. Now with their cost somewhat less, they are more widely used, even finding uses in the mobile telecommunications as well as a variety of microwave radio communications links, and many other RF design applications.

The size of the gate, and hence the channel is very small. Typically the gate is only 0.25 microns or less, enabling the device to have a very good high frequency performance. Reduction in the channel sheet carrier resistance and increase in the drain current was observed when compared to the reference HEMTs. The collapse free MOS HEMTs behavior indicates substantial reduction of the surface states after the annealing step. Moreover it was found that InAlN/GaN heterostructure with deposited dielectric film is robust, withstanding long term thermal stress for 5 h at 700 °C without degradation.

The principal advantages and disadvantages of HEMTs based on InP substrates will be addressed in the appropriate sections. If two semiconductors with different band gap energies are coupled together the difference is divided up into a band gap offset in the valence band DE_V and a band gap offset in the conduction band DE_C . 2DEGs are originate in transistor-like structures made from semiconductors. The most commonly encountered 2DEG is the layer of electrons found in MOSFETs. When the transistor is in inversion mode, the electrons underneath the gate oxide are confined to the semiconductor-oxide interface, and thus occupy well defined energy levels. Almost the lowest level is occupied, and so the motion of the electrons perpendicular to the interface can be ignored. though, the electron is free to move parallel to the interface, and so is quasi two-dimensional.

Enhanced device performances of DC and RF, power, and reliability of the present MOS-HEMT are comprehensively investigated as compared with a conventional Schottky-gate HEMT. A 13-nm-thick Al₂O₃ oxide was grown upon the surface of InAlN/GaN barrier layer and served as the gate dielectric layer and the surface passivation layer at the same time to effectively decrease gate leakage current and prevent RF current collapse, which are the critical issues of nitride

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HEMTs.. Fig. 1 shows a projection for the thickness of gate insulators. As shown, the gate insulator needs to be aggressively scaled down to improve the drive current and to suppress short-channel effects.

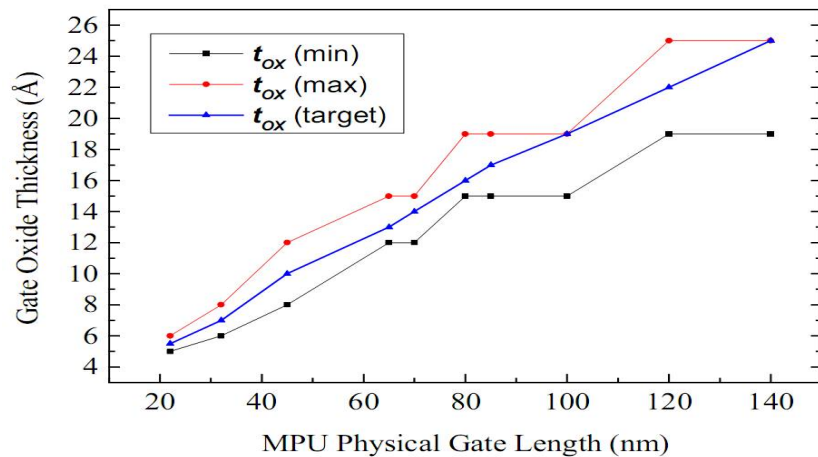


Fig.1: ITRS roadmap for gate insulator thickness as of the year 2001.

II. METHODOLOGY

The methodology offered here can aid the designers to understand the physics and to electrically characterize the new generation of GaN based devices. The models proposed here can also easily be implemented in TCAD simulation packages where models for GaN devices are not mature.

1. To show the TCAD simulations of InAlN/GaN to accurately match measured small signal AC data.
2. To reduce the dc gate leakage currents and to prevent RF current collapse.
3. To demonstrate TCAD AC analysis and RF simulations.
4. To improve the breakdown voltages and RF power handling capability.
5. The performance of InAlN/GaN MOSHEMT for DC, and RF, power and reliability characterization can be improved by using the oxidation method.
6. To influence the method for reducing on-resistance by using the dielectrics with the higher dielectric constant and also by reducing the gate length.

III. ANALYSIS OF ON RESISTANCE FOR InAlN/GaN HYBRID MOS HEMT BY USING MOBILITY MODEL

Since it is naturally normally-off, the hybrid InAlN/GaN MOS-HEMT has a tremendous potential for an advanced GaN-based power switch. An analytical model for the hybrid InAlN/GaN HEMT on-resistance is presented in this work.

It is generally assumed that the new generation of power devices for power converters will be based on Wide Band Gap(WBG) semiconductors to replace traditional silicon power switches. The use of these new power semiconductor materials will allow increasing the efficiency of the electric energy transformations for a more rational use of electric energy thus reducing carbon footprint. The most promising WBG semiconductor materials are SiC and GaN. One of the most interesting properties of GaN for power application is the high electron mobility of the two dimensional electron gas (2DEG) formed in InAlN/GaN heterostructures offering high electron mobilities (over 1200 cm²/V s). In recent years, GaN high electron mobility transistors (HEMTs) have attracted most attention with impressive trade-off between specific on-resistance and breakdown voltage. The GaN HEMTs are expected as microwave power devices used for base station of cellular phone and switching power devices used in the inverter DC/DC converter for the motor and generator [1]. Since the demonstration of the first GaN-based HEMT switches [2], rapid progress has been made in the development of GaN-based HEMT devices. Output power densities at microwave frequencies of GaN-based HEMTs on both sapphire and SiC substrates have improved during the last decade with high output power

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capability larger than 40 W/mm [3]. For high-voltage power switching applications, the Lateral Double Diffused structure (LDD-MOSFET) has the advantage of naturally normally-off operation and large conduction band offset, which makes it less susceptible to hot electron injection and other reliability problems, in particular those related with surface states and current collapse. With an acceptable quality SiO₂/GaN interface, GaN MOSFETs are viable. Lateral GaN MOSFETs with relatively high channel mobility (a peak of 170 cm²/V s) and high blocking voltage (2.5 kV) have been demonstrated [4]. Therefore GaN MOSFET has the advantages of normally-off operation without current collapse problems. However, GaN MOSFET currently exhibits – and probably it will be an unsolved major problem as in the case of SiC – modest inversion channel mobility (below 300 cm²/V s) due to the presence of interface states, surface roughness and other scattering mechanisms.

A way to around this could be the incorporation of InAlN/GaN heterostructure into the RESURF region of GaN MOSFETs. A hybrid MOS-HEMT [5–8] has the advantage of both the MOS gate control and the high mobility 2DEG in InAlN/GaN drift region. A cross-section of the hybrid MOS-HEMT analyzed here is presented in Fig. 2. This hybrid MOS-HEMT has a tremendous potential to be one of the key advanced GaN-based power switches. The analytical modeling for understanding the influence of the main design parameters on the on-resistance of a hybrid MOS-HEMT. Our preliminary point is physical based models for HEMT and MOSFETs which are subsequently combined to determine the on-resistance of the hybrid MOS-HEMT

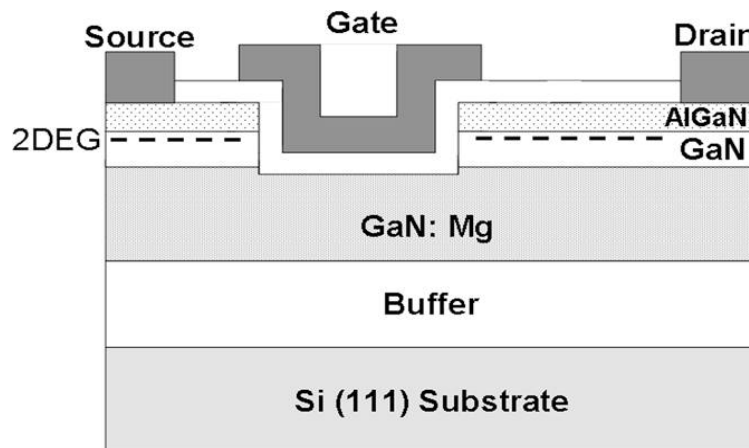


Fig: 2 Cross-sectional view of a hybrid MOS-HEMT.

One immense advantages of GaN as power semiconductor substrate is that transistor effect could be achieved by defining the inversion channel under a MOS gate or by taking advantage of the heterointerface 2DEG charge centroid (Fig. 3). In MOSFET and HEMT transistors on-resistance have been linked to the channel layout and electron mobility properties by analytical relationships for low transverse fields [9]

$$R_{on}(mosfet) = R_{on} = \left[\frac{L_{ch}}{\mu_n C_{ox} (V_{gs} - V_{th})} + \right] (L_{ch} + L_D)$$

$$R_{on}(HEMT) = R_{on,H} = \frac{L_{ds}^2}{q \mu_n n_s}$$

where μ_n is the mobility of carriers in the inversion channel, V_{gs} the gate to source voltage and V_{th} is the threshold voltage. C_{ox} is the gate insulator capacitance per unit area, where ϵ_r is the gate insulator dielectric constant and t_{ox} is the gate insulator thickness. The second term of R_{on} (MOSFET) is incorporated if a low doped drift region (or extended drain) to improve the breakdown voltage is considered (LD-MOSFET). For the HEMT, the sheet carrier density on the 2DEG n_s , may be determined by means of Hall bar measurements and/or capacitance measurements. In is in this case

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the mobility of electrons in the 2DEG channel. The sheet carrier density on the 2DEG ns, can be determined by means of Hall bar measurements and/or capacitance measurements. C_{ox} is the gate oxide capacitance per unit area.

$$R_{on,HM-H} \approx \left[\frac{L_{GS} + L_{GD}}{q\mu_{2DEG}n_s} + \frac{L_G}{\mu_{MOS}C_{ox}(V_{gs} - V_{th})} \right] (L_{GS} + L_{GD} + L_G)$$

The hybrid MOS-HEMT specific on-resistance depends on the layout parameters (L_{GS} , L_G and L_{GD}), the carrier concentration in the 2DEG (n_s) and in the inversion channel ($C_{ox}(V_{gs} - V_{th})$) and their respective mobility values, μ_{DEG} and μ_{MOS} . A hybrid MOSHEMT has the advantage of both the MOS gate control and the high 2DEG mobility in InAlN/GaN drift region. Simple analytical modeling for understanding the influence of the main design parameters on the on-resistance of a hybrid MOS-HEMT. In particular investigate the effect of the layout, the reduced MOS channel mobility, the influence of different high-k dielectrics and the temperature by means of physical models for MOSFET and HEMT devices. It is recommended that an hybrid MOS-HEMT is still competitive in terms of Ron if the gate length is maintained sufficiently small even for modest MOS channel mobilities below 100 cm²/Vs. A high-k dielectric could even improve this Fig

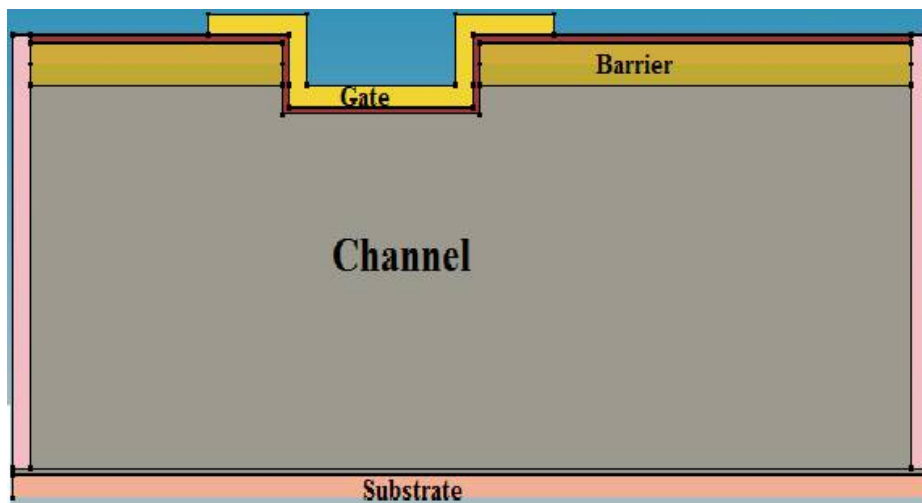


Fig.3. Structure Using Sentaurus Structure Editor In TCAD

Technology computer aided design has become a central part of semiconductor modeling and design. It is important to note that the accurate TCAD simulations and modeling of physical devices depend significantly on calibrated physical models and proper input data. A typical device tool flow the creation of a device structure by a process simulation (Sentaurus Process) followed by re-meshing. Sentaurus Device is used to simulate the electrical characteristics of the device. Sentaurus Device simulates numerically the electrical behavior of a single semiconductor device in isolation or several physical devices combined in a circuit. Terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and the conduction mechanisms. Finally, Tecplot SV is used to visualize the output from the simulation in 2D and 3D, and Inspect is used to plot the electrical characteristics.

An imperative benefit of using TCAD is that it can help in accepting how semiconductor devices work. Assessment of detailed device operation, such as how the energy levels and the carrier (electrons and holes) distribution inside the device varies with the biasing conditions, can provide valuable insights into the relationship between a change in process conditions or device design and the resulting impact on the device performance. These quantities are often

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difficult to obtain experimentally. In contrast, they are readily available through computer simulations, which directly provide the feedback and the guidance for device design.

RESULTS AND DISCUSSIONS

ON RESISTANCE (R_{ON})

The hybrid MOS-HEMT specific on-resistance depends on the layout parameters (L_{GS} , L_G and L_{GD}), the carrier concentration in the 2DEG (n_s) and in the inversion channel ($C_{ox}(V_{gs}-V_{th})$) and their respective mobility values, μ_{DEG} and μ_{MOS} .

A conventional device layout of $1.5/1/6 \mu m$ ($L_{GS}/L_G/L_{GD}$) has been chosen which is typical of power HEMTs for the range of the 600 V. For a given gate bias, the hybrid MOS-HEMT is strongly dependent on MOS channel mobility which is presumably the more difficult parameter to control. As it can be seen in Fig. 4 the R_{on} increases as the channel mobility reduces from the state-of-the-art value of $200 \text{ cm}^2/\text{Vs}$ [4] to values of $20\text{--}100 \text{ cm}^2/\text{Vs}$.

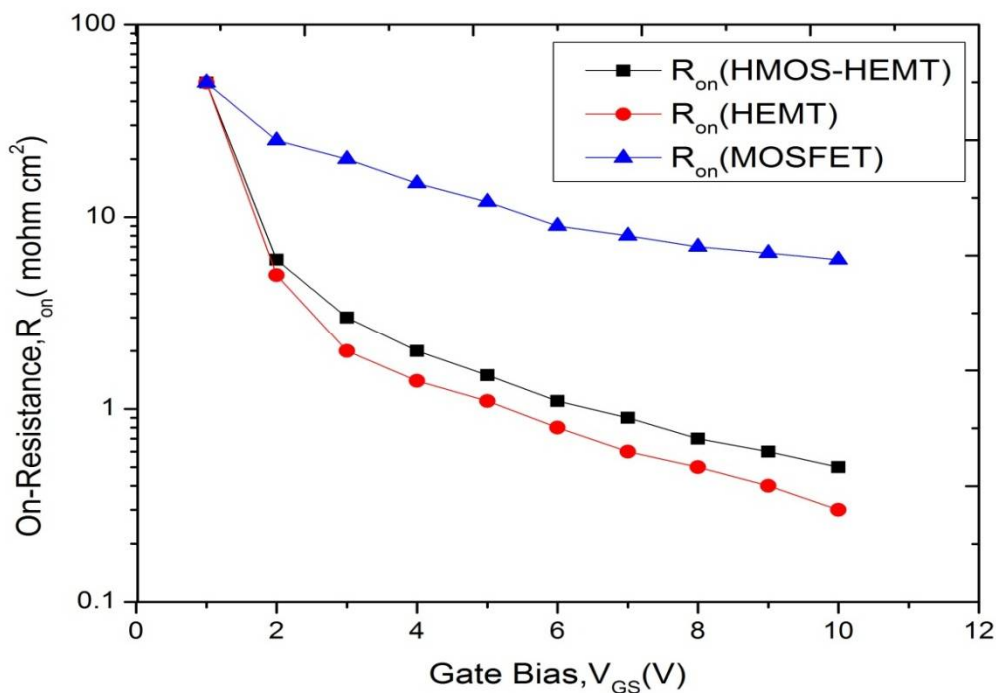


Fig.4 Computed on-resistance vs. gate bias for HEMT and hybrid MOS-HEMT with MOS mobilities of $20 \text{ cm}^2/\text{s}$ and $200 \text{ cm}^2/\text{s}$.

In fig 15 we discussed about the computed on resistance vs gate bias for HEMT and hybrid MOSHEMT based on the mobility value. It shows that the on resistance value vs gate bias for hybrid MOSHEMT is less when compared with HEMT due to its high mobility value. Hence the on resistance value gets decreases when the mobility value increases.

One straight forward method of reducing the on-resistance is to reduce the MOS channel length for a given MOS mobility as it is shown in Fig. 5. It can be seen from the figure that for the smaller MOS gates ($L_G < 1 \mu m$) the on-resistance value approaches to the one from the HEMT even for a reduced value of the channel electron mobility of 200

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cm²/Vs.

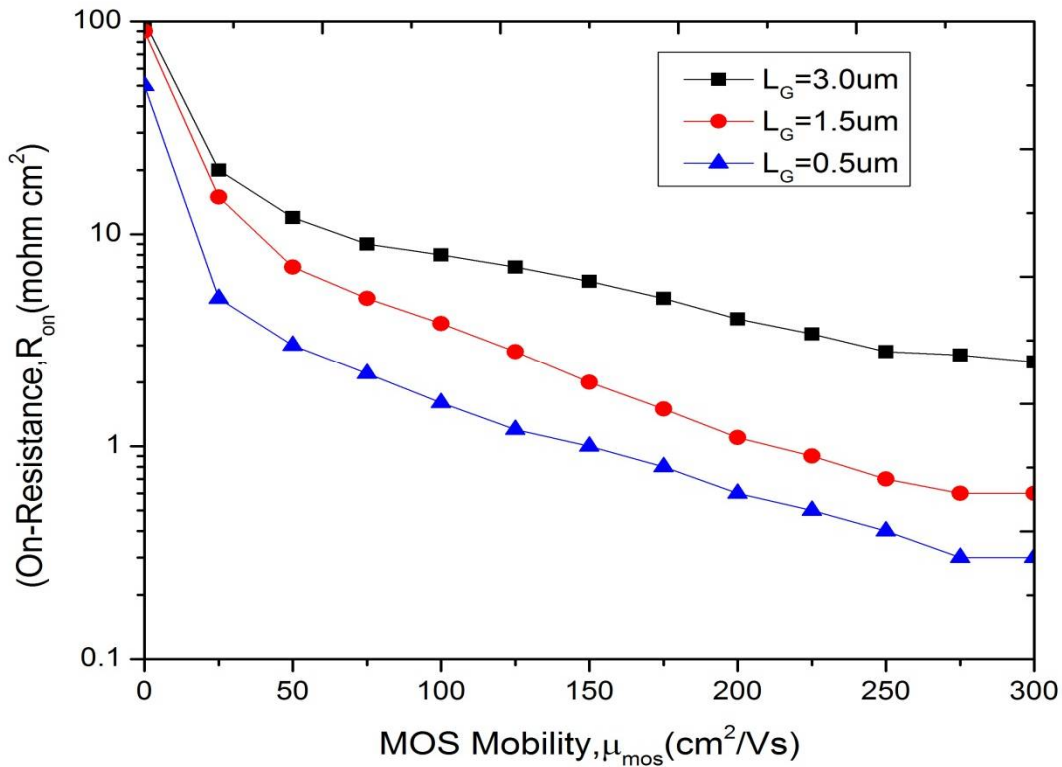


Fig.5 Hybrid MOS-HEMT computed on-resistance vs. MOS mobility value for different channel lengths

Fig 6 shows the comparison of hybrid MOSHEMT computed on resistance vs mobility value for different channel lengths. It shows that the on resistance value gets decreases when the channel length is 0.5 μm .Hence by reducing the channel lengths offers diminish value the on resistance. A way of reducing further the channel on-resistance is shown in fig 6 using insulators with higher dielectric constant. The dielectric constant is 7.4, 10 and 20for SiN_x, Al₂O₃ and HfO₂,

respectively.

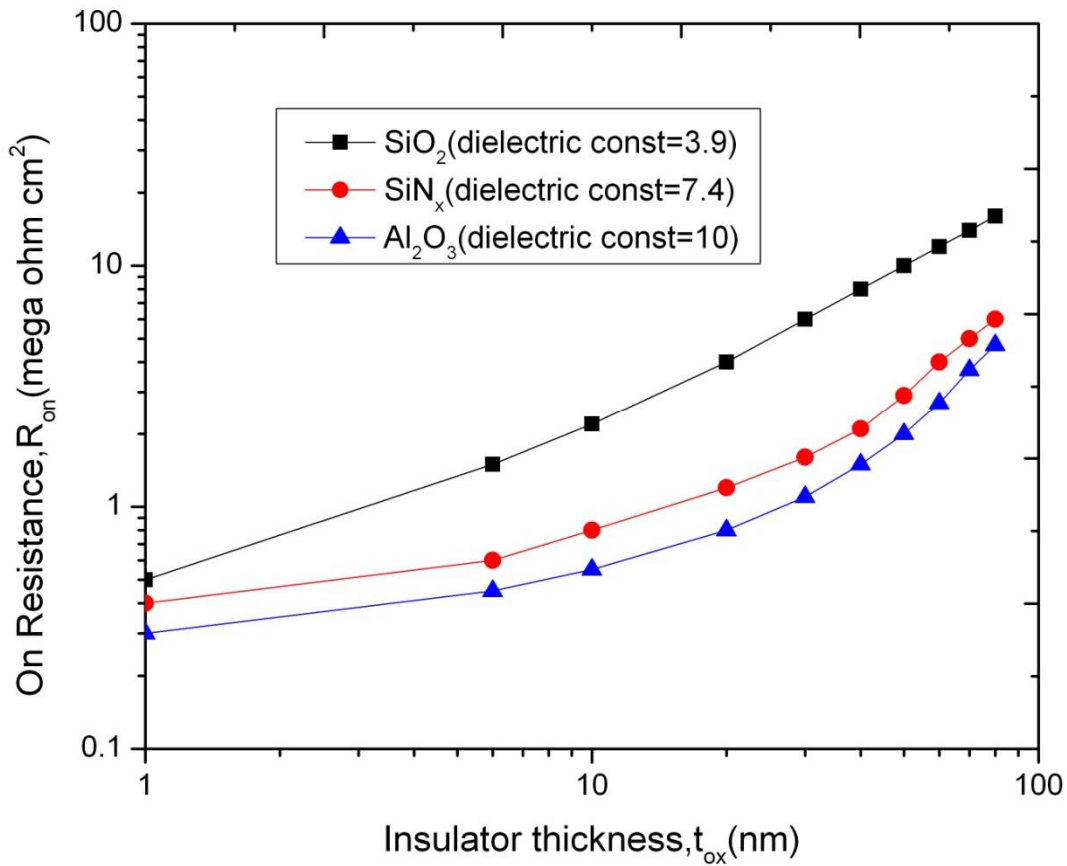


Fig. 6. Hybrid MOS-HEMT computed on-resistance vs. insulator thickness for different dielectrics (SiO_2 , SiN_x , Al_2O_3 and HfO_2).

DC CHARACTERISTICS

Fig.7 shows the transfer characteristics of the hybrid MOS HEMT. The V_{ds} was $0.1 V_{th}$ measuring the characteristics, the gate bias was swept from -10 V to 15 V. The hybrid MOS HEMT. realized normally-off operation with the V_{th} of 2.7 V. The gate leakage current was below 100pA/mm. The low gate leakage current property was probably accomplished by applying Al_2O_3 as the gate insulator.

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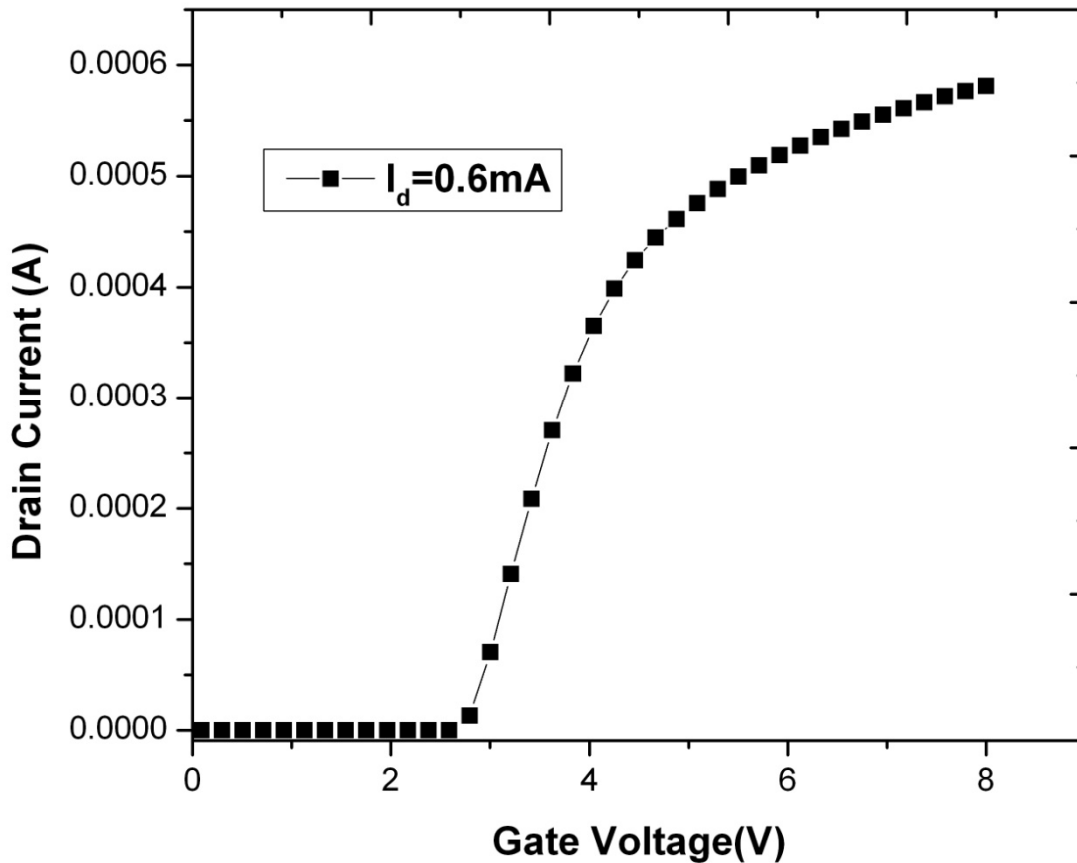


Fig 7. Transfer characteristics of AlInN/GaN hybrid MOS-HEMT. The drain-to source voltage is 0.1 V. The channel length and channel width were 2 μm and 200 μm , respectively

Fig. 8 shows the output characteristics of the fabricated AlInN/GaN hybrid MOS-HEMT. The maximum drain current was over 0.9 A/mm at the gate voltage (V_{gs}) of 20 V and the specific on state-resistance was 9.1 $\text{m}\Omega \text{cm}^2$. From these results above, it is confirmed the basic operation of the AlInN/GaN hybrid MOS-HEMT fabricated by our process.

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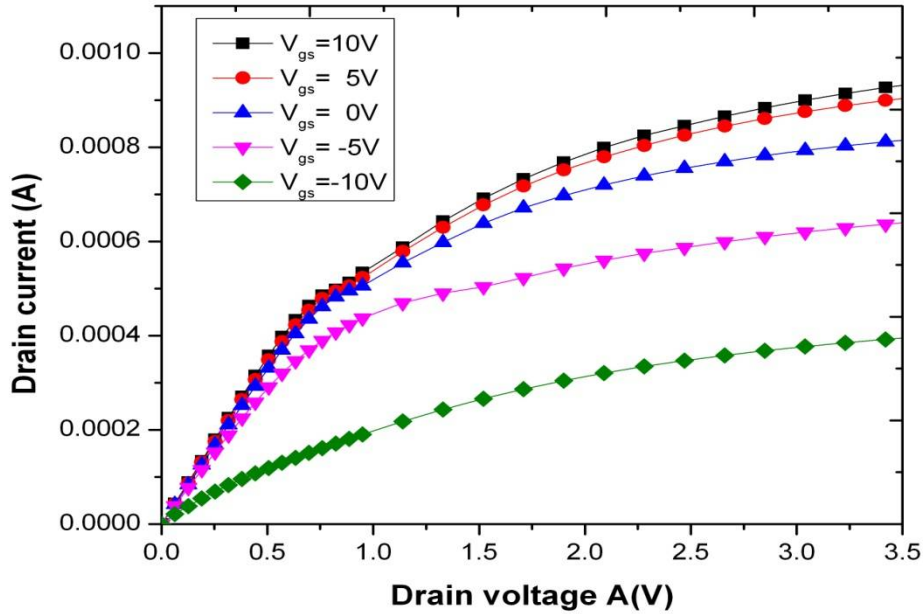


Fig. 8 Output characteristics of AlInN/GaN hybrid MOS-HEMT. The channel length and channel width were 2 μm and 200 μm , respectively.

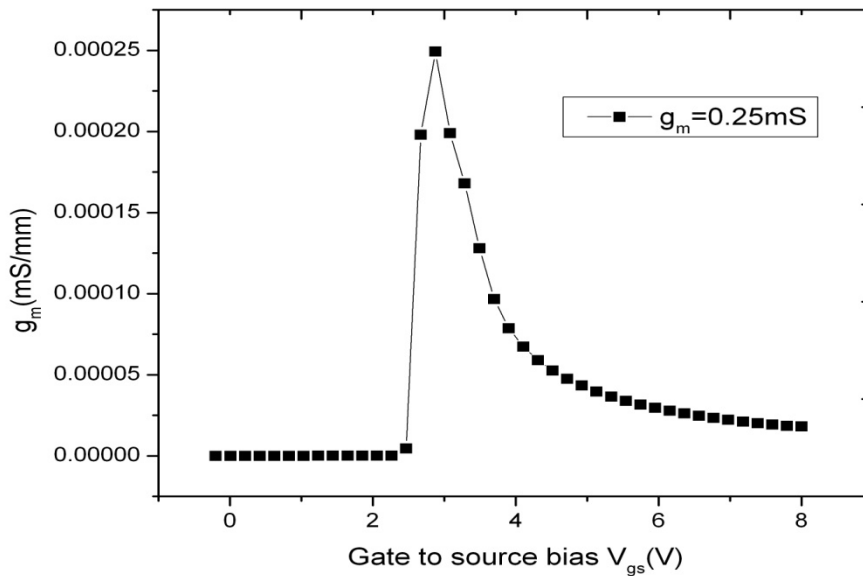


Fig:9 Transconductance of AlInN/GaN hybrid MOS-HEMT with drain-to source voltage 0.1 V.

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ON CURRENT (I_{ON}) AND OFF CURRENT(I_{OFF})

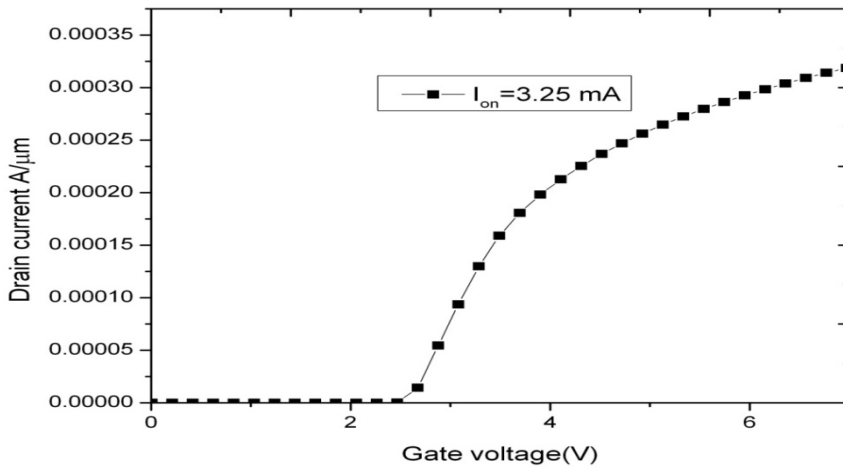


Fig:10 Transfer characteristics of AlInN/GaN hybrid MOS-HEMT On-current. The drain-to-source voltage is 0.1 V. The channel length and channel width were 2 μm and 200 μm , respectively with the on current value($I_{on}=3.25\text{mA}$)

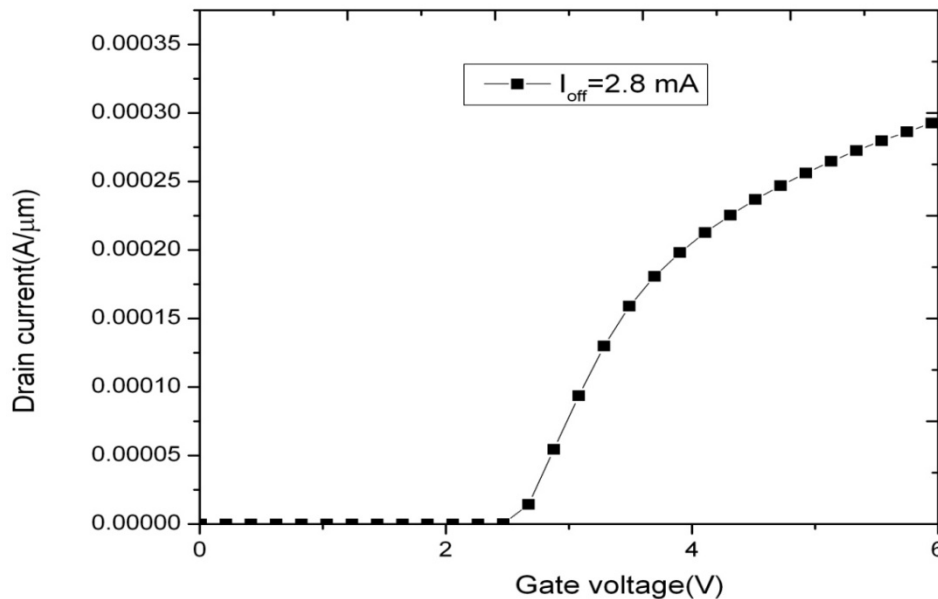


Fig:11 Transfer characteristics of AlInN/GaN hybrid MOS-HEMT. The drain-to-source voltage is 0.1 V. The channel length and channel width were 2 μm and 200 μm , respectively with the off current value($I_{off}=2.8\text{mA}$)

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V. CONCLUSION

A hybrid MOS-HEMT has the advantage of both the MOS gate control and the high 2DEG mobility in InAlN/GaN drift region. In this work, analysis of on-resistance for InAlN/GaN hybrid MOS-HEMT by using mobility model is done. In particular it is investigated on the effect of the layout, reduction of MOS channel mobility, the influence of different high-k dielectrics and the temperature by means of physical models for MOSFET and HEMT devices.

In this work the physical based models for HEMT and MOSFETs which are subsequently combined to determine the on-resistance of the hybrid MOS-HEMT and the method of reducing on-resistance is achieved for the dielectrics with the higher dielectric constant.

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