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A Review on Low Power Compressors for High Speed Arithmetic Circuits

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ABSTRACT: A Multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, Digital Signal Processors (DSPs), Microprocessors etc., A Wallace tree multiplier is an improved version of tree based multiplier architecture. It uses 4:2, 5:2 compressors and a Carry Select Adder (CSA) to reduce the latency and power consumption. In conventional methods, 10T XNOR structure is used for Full adder design. In proposed method, 3T XNOR gate cell is used for Full adder design. Using this 3T XNOR technology, a 4:2 compressor has been designed and the design of a 5:2 compressor is proposed sing 3T XNOR technology which results in 8T Full adder design which reduces the transistor count when compared to conventional full adders. Hence the proposed compressors can remarkably reduces power consumption. In this review article, various architectures and designs of arithmetic circuits are discussed.

KEYWORDS: XNOR-XOR module, Full adder, Compressors, Multiplier.

I. INTRODUCTION

In recent years, the focus of VLSI design is mainly on high performance microprocessors. There is an increase in demand for high speed, small area, low power and low cost designs. It is due to rapid growth of portable battery operated devices such as personal computing devices, wireless communication systems (PDAs and mobile phones), medical applications and other portable devices.

In many VLSI systems such as microprocessors and application specific DSP architectures, addition is the fundamental operation. Full adder is the basic functional block for most of the arithmetic operations such as compressors, comparators, parity checkers, multipliers, etc. It is the core of many other useful operations such as multiplication, division, subtraction, exponentiation, address calculation and it can significantly influence the overall performances of the system.

Generally there are three stages of multipliers. They are Generation of Partial products, Addition of partial products and final addition stage. In the first stage, both the multiplier and the multiplicand are multiplied bit by bit to generate the partial products. The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing. This article discusses various designs of arithmetic circuits such as full adders, compressors which are all applicable to the field of low power architectural design.

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II. LITERATURE REVIEW

A. Ultra Low-Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits [2004]

In this paper the author presents various architectures and designs of low-power 4-2 and 5-2 compressors capable of operating at ultra low supply voltages. Each architecture has different configurations includes a number of novel 4-2 and 5-2 compressor designs. They are prototyped and simulated to evaluate their performance in speed, power dissipation and power-delay product. The proposed new circuit for the XOR–XNOR module described in this paper

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eliminates the weak logic on the internal nodes of pass transistors with a pair of feedback NMOS–PMOS transistors. Driving capability has been considered in the design as well as in the simulation setup so that these 4-2 and 5-2 compressor cells can operate reliably in any tree structured parallel multiplier at very low supply voltages. In this paper the author conclude that a new low-power circuit with good drivability is proposed for the complex XOR logic module which is used to co-generate the XNOR-XOR outputs. Novel 5-2 compressor architecture of delay is also proposed. A new design of the carry generator cell has been spawned as a result of this unique architecture.

B. Novel and Efficient 4:2 and 5:2 Compressors with Minimum number of Transistors Designed for Low-Power Operations [2006]

This paper proposes efficient and optimal 4:2 and 5:2 compressors. The compressors are highly optimized in terms of transistor count. These designs have the principle advantage that in addition to reduced transition activity, they have no direct connections to the power-supply and is totally driven by the input signals, leading to a noticeable reduction in short-circuit power consumption. The proposed 4-2 and 5-2 compressor designs have been implemented with a bare minimum of 20 and 30 transistors respectively. The speed, area and power consumption of the multipliers will be in direct proportion to the efficiency of the compressors. This paper provides novel designs of 4:2 and 5:2 compressors with minimum number of transistors. The proposed designs are highly efficient in terms of small area low power and high throughput. In this paper, the author first described about the existing architecture of 4:2 and 5:2 compressors. In the proposed compressor design, the XOR gate and MUX designs are appropriately replaced with minimum transistor implementation to design the circuit such that it has no direct supply from VDD. It can be inferred that the proposed 4:2 compressor design is an optimized version as the authors have optimized the entire design starting from the basic cell level.

C. A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design [2007]

In this paper, the author proposed a full adder design using only ten transistors per bit. The proposed design features lower operating voltage, higher computing speed and lower energy operation when compared with existing methods. The design uses inverter buffered XOR/XNOR designs to eliminate the threshold voltage loss problem. This problem prevents the full adder from operating in low supply voltage. The proposed design embeds the buffering circuit in the full adder design and the transistor count is minimized. The improved buffering helps to operate under lower supply voltage compared with existing works. It also enhances the speed performance of the cascaded operation significantly while maintaining the performance edge in energy consumption. Both dc and performances of the proposed design against various full adder designs are evaluated via extensive HSPICE simulations.

D. Novel Architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Compressors [2007]

In this paper, the author presented novel architectures and designs of high speed, low power 3- 2, 4-2 and 5-2 compressors capable of operating at ultra-low voltages. The power consumption, delay and area of these new compressor architectures are compared with existing and recently proposed compressor architectures and are shown to perform better. The proposed architecture lays emphasis on the use of multiplexers in arithmetic circuits that result in high speed and efficient design. In the proposed architecture these outputs are efficiently utilized when compared to existing designs to improve the performance of compressors. In the proposed novel architectures of 3-2, 4-2 and 5-2 compressors, the author replaces some XOR blocks with MUX blocks. Since the availability of the select bits before the input bits arrive completes the switching activity of the transistors, the overall delay in the critical path is reduced while using MUX blocks. This paper concludes by analyzing the proposed architectures of 3-2, 4-2, 5-2 compressors with the conventional architectures.

E. Ultra Low Power 1-Bit Full Adder [2011]

In this paper the author proposed a new 9 transistor 1-bit full adder. The proposed circuit performs efficiently in subthreshold region to employ in ultra low power applications. The main design objective for this new circuit is low power consumption and full voltage swing at a low supply voltage. The proposed cell also remarkably improves the power consumption, power delay product and has better noise immunity when compared to the existing deigns. One way to achieve ultra low is by running digital circuits in subthreshold mode. Subthreshold current of an MOSFET transistor occurs when the gate-to-source voltage (*VGS*) of a transistor is lower than its threshold voltage (*VTH*). In standard CMOS design, this current is a subthreshold parasitic leakage, but if the supply voltage (*VDD*) is lowered below *VTH*, the circuit can be operated using the subthreshold current with ultra-low power consumption. In this paper

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the author proposed the new 9T full adder circuit by modifying the existing 8T full adder circuit with a cost of one transistor. Though the area is increased due to that transistor, power is reduced than the existing architecture. In this paper the author concluded by proposing a new improved design of 1-bit full adder cell performing efficiently in subthreshold region outperforming the existing 8T full adder.

F. Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate [2011]

In this paper, a new XNOR gate using three transistors has been proposed, which shows power dissipation of 550.7272µW in 0.35µm technology with supply voltage of 3.3V. A single bit full adder using 8T has been designed using proposed XNOR cell, which shows power dissipation of 581.542µW. Power consumption of proposed XNOR gate and full adder has been compared with earlier reported circuits and proposed circuits shows better performance in terms of power consumption and transistor count. The design and operation of 3T XNOR gate is discussed first. The XNOR-XOR module can be obtained by adding an inverter circuit to the XNOR gate. The full adder circuit can be implemented by different combinations of XNOR gate and multiplexer. The sum output is implemented by cascading the 3T XNOR and the carry output can be implemented by using 3T XNOR gate and 2T MUX.

G. An efficient high speed Wallace tree multiplier [2013]

An improved version of the tree based multiplier architecture is called Wallace tree multiplier. It uses carry save addition algorithm to reduce the latency. This paper aims to further reducing the latency and power consumption of the Wallace tree multiplier and it is accomplished by using 4-2 and 5-2 compressors and a proposed carry select adder. The Wallace tree basically multiplies two unsigned integers. The conventional Wallace tree multiplier architecture comprises of an AND array for computing the partial products a carry save adder for adding the partial products so obtained and a carry propagate adder in the final stage of addition. In the proposed architecture, partial product reduction is accomplished by the use of 4:2, 5:2 compressor structures and the final stage of addition is performed by a proposed carry select adder. The latency in the Wallace tree multiplier can be reduced by decreasing the number of adders in the partial products reduction stage. The combined factors of low power, low transistor count and minimum delay makes the 5:2 and 4:2 compressors, the appropriate choice. The use of two full adders would introduce a delay of 4 whereas the use of 4:2 compressors reduces the latency to 3. Two full adders are replaced by a single 4:2 compressor and 5:2 compressors replace three full adders. Then a carry select adder is proposed. In the conventional Wallace tree, the major cause of delay is the propagation of the carry out from the previous stages to the next stage. Therefore the total latency of the given structure when calculated is 27. In the proposed Wallace tree, full adders are replaced by compressors which reduce the latency to 15.

H. Low Power Full Adder using 9T Structure [2013]

In this paper, the author proposed a new 9T 1-bit full adder. The main objective is full output voltage swing, low power consumption and temperature sustainability. The proposed design is more reliable in terms of power consumption, Power Delay Product (PDP) and temperature sustainability as compared to the existing full adder designs. In this paper, the author first illustrates the existing 8T full adder. It suffers from threshold loss problem due to simultaneous enabling of NMOS and PMOS transistor. Then the existing 9T full adder design is discussed which has additional transistor to improve the performance of the 8T full adder design. The problems in the 8T full adder circuit for certain input vectors were overcome in the existing 9T full adder. Though the power consumption is reduced, the existing 9T full adder circuit still suffers from threshold loss problem. Hence the proposed 9T full adder design is presented where the sum output is implemented by a cascaded 3T XOR and 2T MUX and the carry output is implemented by a 3T XOR and a 2T MUX. The proposed 9T full adder design has better performance when compared to the existing full adder designs.

I. Low Power 9T Full adder using Inversion Logic [2013]

In this paper, pre-layout and post-layout simulations of a new 9T full adder cell at low voltages are presented. The main objective of design is low power consumption and full voltage swing which is achieved at low supply voltage. The proposed design shows its superiority against existing adder in terms of power consumption, power-delay product (PDP), temperature sustainability and noise immunity. In this paper, the author first presented the existing 9T full adder architecture and discusses its problems for certain input vectors. The main drawback of this design is threshold loss problem. For certain input vectors there is a major degradation in output logic level which may leads to functional failure. Hence a proposed 9T full adder is designed. In this design the sum output has been implemented using 3T XOR

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gate, an inverter and a 2T MUX and the carry output has been implemented using 3T XOR gate and a 2T MUX. This circuit reduces the power consumption and also improves the temperature sustainability.

J. A New Design of Full Adder based on XNOR-XOR Circuit [2013]

In this paper the simulations of a proposed 8T full adder design using a proposed 3T XNOR gate cell is presented. The author describes the main drawback of the existing 3T XNOR gate. The full adder design using the existing 3T XNOR gate confronted with problems for certain input vectors. It doesn't give good logic levels in the output. This drawback is overcome in the proposed 3T XNOR gate. In this the output terminal is connected to drain of all transistors. Then the performance of the proposed design is compared with the existing one and it shows the better results. Using the proposed XNOR module, a new 8T full adder circuit is designed. It overcomes the confronted problems that occurred in the existing full adder design.

K. Low power 4-2 Compressors for Arithmetic Circuits [2013]

In this paper, the author presents 4-2 compressor using two different 8T full adder designs. The aim of this paper is to reduce the power consumption of 4-2 compressor without compromising the speed and performance. A multiplier is typically composed of three stages- Partial products generation stage, partial products addition stage, and the final addition stage. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing. The author first describes about the 4-2 compressors which consists of 5 inputs and 3 outputs. It is called compressors since it compress four partial products into two. In this paper 4-2 compressors using full adders which is made up of existing and proposed 3T XNOR gate is design and discussed. It is designed by compressing two 8T full adder architectures.

L. Array multiplier using XNOR-XOR cell [2013]

This paper presents an application of the proposed XNOR-XOR cell for a 2x2 array multiplier and its performance has been analysed and compared in terms of power consumption and PDP with varying input voltage, temperature and frequency as compared to the existing XNOR-XOR cell based 2x2 array multiplier. Different kinds of multipliers are Serial, Sequential, Array and Tree multipliers. Array and tree multipliers are two of the most popular kinds of multiplier. Array multiplier has a regular structure that simplifies the wiring and layout, so the design time of array multiplier is much less compare to the other ones. The basic process of binary array multiplication involves the AND operation of multiplicand and multiplier bits and subsequent addition. The author describes the multiplier with the existing XNOR-XOR gate and proposed XNOR-XOR gate.

III. RESULTS AND DISCUSSION

In [1], the simulation results show that the 4-2 and 5-2 compressors constructed with the novel XOR cell is able to function down to 0.6 V, and features high speed and low-power characteristics. The 5-2 compressor proposed by the author outperforms all the other architectures. The author summarizes that a library of excellent power efficiency 4-2 and 5-2 compressor cells based on CMOS process technology has been developed for implementing high speed and low-power multipliers operable at ultra low supply voltages. In [2], the simulation is done in Tanner spice and the technology being used is 0.35-um CMOS digital technology with a 3.3-V supply voltage. The propagation delay is measured when the changing input reaches 50% of the transition to the time when the output reaches its 50%. Finally the author concluded that the proposed designs have the advantage that in addition to reduced transition activity, they have no direct connections to the power-supply and are totally driven by the input signals, leading to a noticeable reduction in short-circuit power consumption.

In [3], the simulation results are based on TSMC 2P4M 0.35- m process models, indicate that the proposed design has the lowest working Vdd and highest working frequency among all designs using 10T. It also shows the power consumption is low per addition among these designs. And also, the performance edge of the proposed design in both speed and energy consumption becomes even more significant as the word length of the adder increases. The CLRCL design requires the lowest power supply among all 10T designs. The CLRCL design has the capable of the highest working frequency. In [4], all the simulations have been done using Cadence Tools with 0.18-µm technology. The calculation of power (including glitch power) and delay are carried out using the Virtual Analog Simulation tool already integrated into Cadence Tools. The simulations are performed under various voltages ranging from 0.9V to

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3.3V. The proposed architectures perform better than the existing ones in every aspect i.e., area, power, delay and power-delay product over the complete voltage range simulated.

In [5], all simulations are performed on 45nm technology standard models in subthreshold region on Tanner EDA tool version 12.6 with input voltage ranges from 0.1V to 0.25V in steps of 0.05V. The combination of improved power dissipation, power-delay product, and threshold loss and noise immunity makes the proposed full adder a viable option for ultra low power applications. In [6], the simulations are carried out and the results are compared with the existing different types of architectures. The results show that the power consumption of the proposed 3T XNOR gate and the proposed full adder using that 3T XNOR gate is very much less when compared to the existing architectures. Hence the proposed circuits not only reduce the power consumption but also reduce the transistor count.

In [7], the simulations have been carried out using the Modelsim and Xilinx tools. The result shows that the proposed Wallace tree multiplier is 44.4% faster than the conventional Wallace tree multiplier, along with realization of 11% of reduced power consumption. In [8], the simulations are performed using Tanner EDA Tool version 13.0 at 45nm technology with the input voltage ranges from 0.4V to 1.4V in step of 0.2V. Finally the author concluded that, the simulation results shows that the proposed design offers a better and more competitive result than other existing designs so it can be operated at low voltage and has better output voltage swing. The proposed 9T full adder design shows 75%, 82% improvement in terms of power consumption and 76%, 69% improvement in terms of PDP in comparison to existing 8T, 9T full adder design respectively. Thus, the proposed design is a good option for low power applications.

In [9], all pre-layout and post layout simulations have been performed on Tanner EDA tool version 12.6 using 45nm technology with input voltage ranging from 0.4V to 1V in steps of 0.1V. Finally the author concluded that Pre-layout and post-layout of proposed 9T full adder and existing 9T full adder have been designed and simulated. Also the output noise voltage simulated is better than the existing design. The proposed circuit has been tested to have better temperature sustainability and significantly less power consumption, power-delay product to achieve high performance. Hence, the proposed design can be a viable option for low-power application. In [10], all schematic simulations have been performed on Tanner EDA tool version 12.6 at 45nm technology with input voltage ranging from 0.6V to 1V in steps of 0.1V. The simulation results shows that the power consumption and power-delay product of the proposed 8T full adder is 90% to 95% and 99% reduced than the existing 8T full adder design respectively and the proposed 8T full adder design have 72% to 99% better temperature sustainability compare to the existing 8T full adder design. This proves to be a viable option for low power and energy efficient applications. It also shows nearly 82% improvements in threshold loss as compared to the existing 8T full adder.

In [11], all schematic simulations are performed on Tanner EDA tool version 12.6 at 45nm technology with input voltage ranging from 0.4 V to 1.0 V in steps of 0.1 V. Both the designs are analysed in terms of power consumption and power-delay product at varying input voltages, frequencies and temperatures. The results shows that the 4-2 compressor using proposed 8T full adder has better temperature sustainability which remains constant over large range of temperature than 4-2 compressor using existing 8T full adder. The proposed design shows 92% and 99% improvement in terms of power consumption and PDP in comparison to existing design. Hence, it proves itself to be a better option for low power devices and complex systems. In [12], all pre-layout and post-layout simulations have been performed on Tanner EDA tool version 12.6 at 45nm technology with input voltage ranging from 0.6V to 1V in steps of 0.1V. The proposed design shows 57-81% improvement with varying input voltage, 54-65% with varying temperature and 39-54% with varying frequency in term of PDP in comparison to existing design. Hence, the 2x2 array multiplier based on proposed XNOR-XOR cell has been proved to be a better option for low power complex system design.

IV. CONCLUSION

This review article illustrates various architectures and designs of arithmetic circuits. Multipliers are the most critical components for the efficient implementation of DSP and ALU as they lie in the critical path. The critical path determines the overall performance of the system. This article aims at designing efficient multiplier architecture for high speed arithmetic circuits. Out of the three phases in the implementation of multipliers, Compressors are used in the

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second phase which replaces the full adders by compressing them. So the full adders are the basic blocks for designing the compressors efficiently. The operation of full adders is based on XOR operation. For 1-bit full adder, the sum output is obtained by XOR operation of the 3 inputs. Therefore an efficient XOR circuits should be designed. This article analyses many architectures of XNOR-XOR module and a 3T XNOR gate structure is suitable for low power designs. Using this gate structure, a 4-2 compressor has been designed and a 5-2 compressor is proposed using the same. This will reduce the overall power consumption when compared to the existing one and will be suitable for low power applications.

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