

A Review Of Conventional And Emerging Power Gating Techniques For Leakage Power Reduction

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Abstract—Leakage power reduction has become one of the top design priorities in battery operated ultra low power circuits. Reduction in threshold voltage causes leakage power to increase exponentially. Several techniques have been proposed that effectively minimize leakage power consumption. The most effective technique involve power gating in which a circuit is cut off from its power supply in sleep mode by means of a current switch. In this paper we present a review of conventional as well as emerging power gating schemes which are employed to reduce leakage power dissipation.

Keywords—power gating; leakage reduction; sleep transistors; nanoelectromechanical systems; carbon nanotube field effect transistor.

I. INTRODUCTION

CMOS devices have been scaled down aggressively in each technology generations to achieve higher transistor count per unit area, to achieve better performance and to reduce power consumption. However, the leakage current has increased exponentially with technology scaling and hence leakage power reduction has become one of the top design priorities[1]. Over the years, enhancing chip performance has come through increased circuit complexity and number of transistors. But despite down scaling of circuit propagation delay, supply and threshold voltages for every technology generation, the power dissipation in circuits has continued to increase. This increased power dissipation shortens battery life, requires complex cooling and packaging methods, and degrades system performance. The exponential increase of the number of on chip active devices, the constant decrease of the threshold Voltage (V_{th}) and reduction of the gate oxide thickness (T_{ox}) result in a significant amount of static power in circuits designed in deep sub-micron technologies. Static power consumption is because of leakage currents. Leakage currents are the currents that flow through the devices when the devices are in off state and the total currents are expected to be zero. Increase in leakage power is the major concern that circuit designers need to address, especially for circuits that have low-duty cycles, bursty operation and rely on batteries for long periods of time. At nano scale regime subthreshold leakage current, gate leakage current, punch-through leakage, GIDL, and reverse bias leakage current increased significantly with bulk MOS. Due to this static power consumption becomes comparable with dynamic power consumption. In recent years, increasing demand of portable devices, increased leakage power dissipation, thermal management and self heating of devices makes power consumption a vital design constraint for portable applications. Increased leakage power dissipation in nanometer regime can be tolerable for highest performance circuits. However, it is the most demanding design issue for intended Ultra Low Power (ULP) applications to extend the battery life. There is a special class of emerging ULP applications like wireless sensor networks, biomedical implants, energy scavenging devices that do not require high speed. The primary motivation for these applications is ULP consumption so as to prolong the battery life or to employ energy harvesting effectively[2-4]. The leakage current in a nano-scale CMOS device is mainly due to (1) subthreshold conduction, (2) gate direct tunneling current, (3) junction tunneling leakage, (4) gate induced drain leakage (GIDL), (5) hot carrier injection current, (6) punchthrough current, etc. The three main components of leakage, namely subthreshold, gate tunneling, and junction tunneling leakage [1] are shown in Fig. 1.

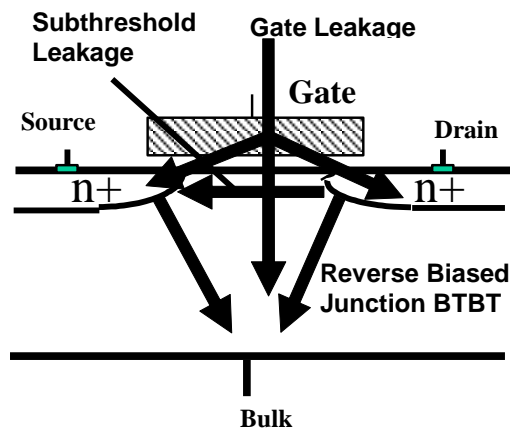


Fig. 1. Leakage current mechanisms [1]

II. POWER GATING

There are a wide array of techniques designed to reduce leakage currents. The most effective techniques involve power gating [5-7] in which a circuit is cut off from its power supply in sleep mode by means of a current switch. Power gating was originally proposed in the form of a circuit called a switched source impedance (SSI) [5]. The concept of multithreshold-voltage CMOS (MTCMOS) was proposed in [6]. MTCMOS circuit shown in Fig.2 is now a days more frequently called power gating wherein only one switch either a header Q1, or a footer, Q2, is usually employed. In sleep mode, input SL is kept high, Q1 and Q2 are turned off, and V_{ddv} and V_{ssv} float; leakage from the low-V_t circuit is thus limited by high-V_t switches. In active mode, SL is kept low, Q1 and Q2 are turned on, and V_{ddv} and V_{ssv} are maintained close to V_{dd} and V_{ss} respectively. Low-V_t is used within the circuit itself to achieve high performance, and high-V_t is used in the switches to achieve low subthreshold leakage [8]. The concept of power-gating is to disconnect the devices from their power or ground sources when off, thus reducing the leakage current flow by creating a break in the power or ground networks. This is usually accomplished through the addition of one or more “switch” circuits to the power or ground network that connect the block or chip level power or ground networks to the external power and ground networks, respectively. Power gating switches are called as sleep transistors. There are two different types of sleep transistors: header-type Fig.3(a), and a footer-type Fig.3(b). Sleep transistors can also be categorized as fine-grain Fig.3(c) and coarse-grain types Fig.3(d). In the case of fine-grain sleep transistor, each digital gate is separated from the power supply independently by one sleep device; however, in the coarse-grain implementation, one sleep transistor is responsible for separation of a block of digital gates [10-11].

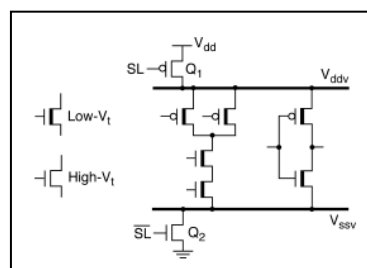


Fig.2. MTCMOS power gating

The basic strategy of power gating is to provide two power modes: a low power mode and an active mode. The goal is to switch between these modes at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance. During active periods, the circuit is reconnected to the power supply in a process known as “wake up” or power up. To accommodate the growing popularity of mobile, wireless, and sensor processing, all of which have substantial idle times, industry has widely adopted power-gating and software-controlled sleep modes. Power-gating, or MTCMOS switching, is rapidly being adopted as a method for controlling off-state standby leakage in high-performance, low-power designs.

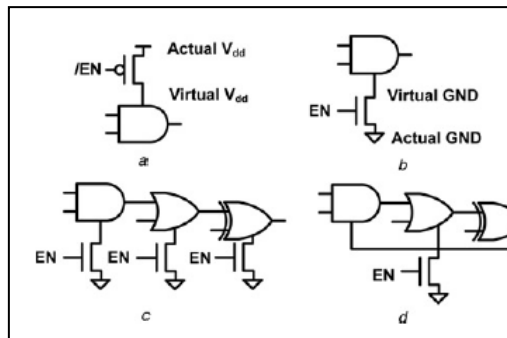


Fig.3. Types of sleep transistors (a) header (b) footer (C) fine-grain (d) course-grain

A limitation of MTCMOS is that the time required for recovering from the idle mode, referred to as the wake-up time, is long relative to circuit clock rates; therefore, the wake-up time prohibits the use of power switches during short periods of inactivity [9]. Transistor power gates have several drawbacks. When a circuit is turned off, the transistor power-gates themselves leak, meaning leakage is reduced, but not eliminated. Also, a voltage drop is created across the power-gate, which lowers the effective supply voltage of the power-gated circuit, thus slowing it down. Making a transistor power-gate wider decreases the voltage drop, but increases the off-state leakage, meaning a trade-off exists. This trade-off and the desire to achieve a large reduction in idle-state leakage without impacting performance has motivated the examination of emerging technologies such as NEMS switches as power-gating structures. In this paper section III and IV describes, emerging technologies, the Nanoelectromechanical-Systems (NEMS) Switch and CNFETs, as an alternate power-gating switch.

III. HYBRID CMOS AND NEM-FET POWER GATING

Nanoelectromechanical system (NEMS) switches as shown in Fig. 4 are nanoscale relays with a suspended cantilever beam (representing the source) that bends under electrostatic force from the gate to form an ohmic contact with the drain.

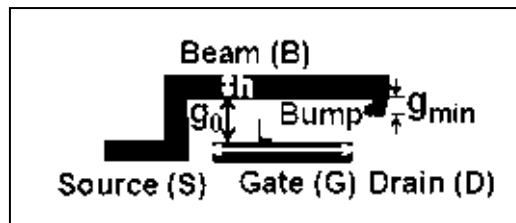
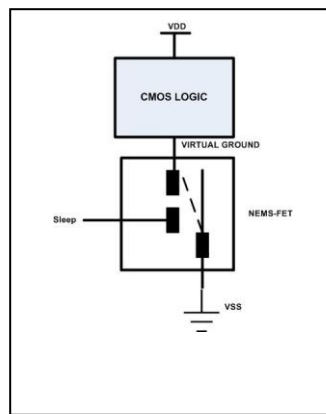


Fig. 4. NEMS switch

Due to an air-gap, NEMS switches have a nearly infinite off-resistance, which essentially eliminates off-state leakage. They also have a very low on-resistance due to the ohmic contact. Since NEMS devices demonstrate ultra-low leakage characteristics, they are an ideal choice as sleep transistors and can be used as power gating elements for CMOS-based

logic to reduce the leakage [12-13]. Although the NEMS switches can be slower than MOS switches, once turned ON, they can provide a low-resistance path to ground, whereas, in the OFF state, they can be used to reduce leakage current due to absence of any conducting path between the beam and the drain. NEMS switch based power gating elements are illustrated in Fig. 5.



A comparison between ON-state resistance and OFF-state leakage of NEMS- and CMOS-based sleep transistors for different device areas [12-13] is shown in Fig. 6. It can be observed that NEMS-based sleep device outperforms CMOS-based sleep transistor in terms of OFF-state leakage current. However, it can also be noticed that NEMS devices exhibit higher ON resistance for equal area size, because of lower drain current of NEMS devices. It can be observed from Fig. 6 that for larger sleep transistors, the difference between the ON resistance of NEMS and CMOS sleep transistors become minimal. Hence, the NEMS sleep transistors can be sized-up to offer up to three orders of magnitude lower leakage current with negligible performance degradation compared to that of their CMOS counterparts [12-13].

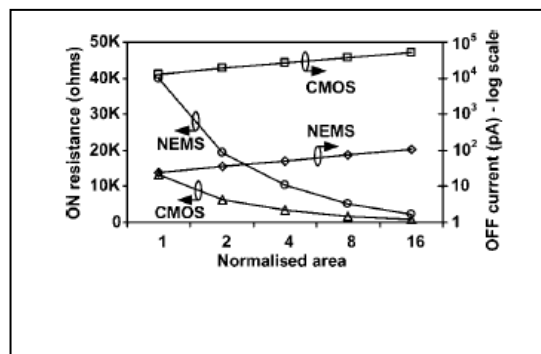


Fig. 6. ON resistance and OFF current of NEMS and CMOS sleep transistors [12-13]

IV. HYBRID CMOS AND CNFET POWER GATING

Carbon nanotube FETs employ semiconducting single-wall carbon nanotubes to assemble electronic devices, and the singlewalled CNFET is obtained by replacing the channel of a conventional MOSFET with carbon nanotubes. The nanotubes can be either a metallic (conductor) or a semiconducting (semiconductor) depending on the angle (represented as a chirality integer vector (n,m)) of the atom arrangement along the nanotube. The nanotube is metallic if

($n = m$) or ($n - m = \text{'a multiple of 3'}$); otherwise, the tube is semiconducting. As shown in Fig. 7, the CNFETs are fabricated on an oxidized Si substrate that can be used as a back-gate in the CNFET.

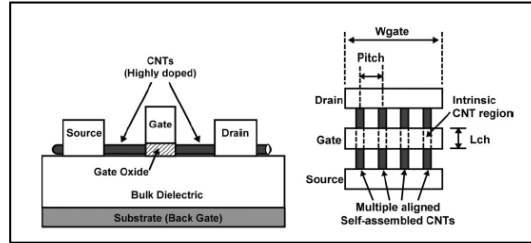


Fig. 7. CNFET structure

Each device has one or more single-wall semiconducting carbon nanotubes. The currents of the CNFET device are controlled by adjusting device parameters such as gate length (L_{ch}), the number of nanotubes, chirality vector, and pitch between nanotubes. As the gate voltage increases or decreases, the device is electrostatically turned ON or OFF through the gate node.

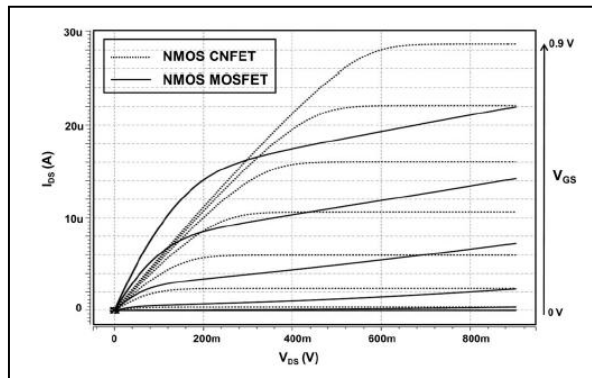


Fig. 8. Drain to source current as a function of drain to source voltage for different gate to source voltage[14]

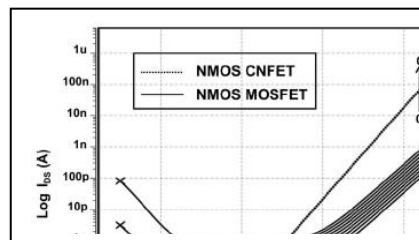


Fig. 9. Drain to source current as a function of gate to source voltage for different drain to source voltage[14]

As shown in the Fig. 8, CNFET on current is higher and leakage current is lower than the MOSFET transistor. Fig. 9 illustrates I_{DS} characteristics of the N-type CNFET in the weak inversion region, which implies that the CNFET would be a more practical solution even in the subthreshold logic design requiring a smaller area than the MOSFET[14]. Hybrid MOSFET and CNFET power gating scheme using 32nm technology in the ultra low voltage region is proposed in [14]. Fig. 10 shows the hybrid PG structure diagram, where an N-CNFET (footer) is placed in series with low- V_{th} CMOS circuits, and the back-gate node of the N-CNFET is connected to the ground. The hybrid structure addresses the low-performance issue caused by high V_{th} of the conventional MOSFET PG structure at the low voltage while keeping low leakage power dissipation in sleep mode.

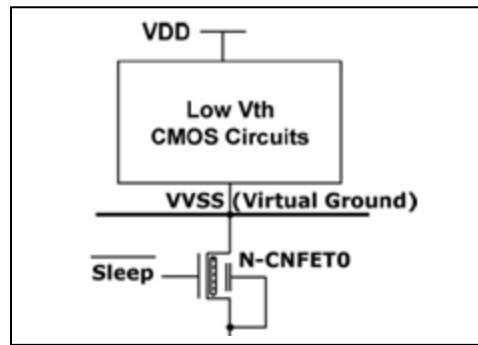


Fig. 10. CNFET based power gating

Fig. 11 presents the simulation results showing the impact of the power supply voltage on the circuit delay of the hybrid PG and MOSFET PG [14]. The authors compared simulation results with those of the inverter chains without PG footer. The area overhead of the MOSFET PG is 10% of the total NMOS width, and the area overhead of the hybrid PG is 1% (number of nanotube = 100, pitch = 5 nm, and chirality vector = (17,0)) of the total NMOS width. As VDD decreases below 0.7V in active mode, the hybrid PG structure becomes faster than the MOSFET PG structure by factor of more than two, and its delay decreases by 70% compared to the MOSFET PG structure at 0.5V. Moreover, the delay of the MOSFET PG structure is exponentially increased at VDD below 0.6. In addition, as the supply voltage scales down, the wake-up time of the MOSFET PG structure significantly increases due to the high threshold voltage of the MOSFET footer as shown in Fig. 12. On the other hand, the wake-up time of the hybrid PG structure increases a little, which is small enough to be ignorable compared to the wake-up time of the MOSFET PG. These simulation results demonstrate that the proposed hybrid MOSFET/CNFET PG structure is very effective in the low-voltage region.

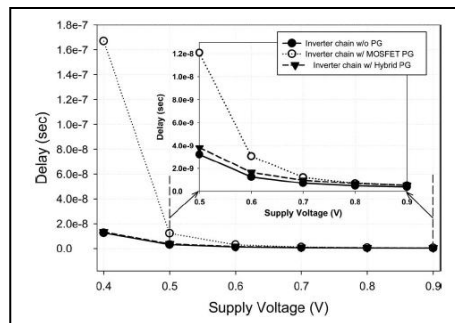


Fig. 11. Delay dependence of power gating on supply voltage[14]

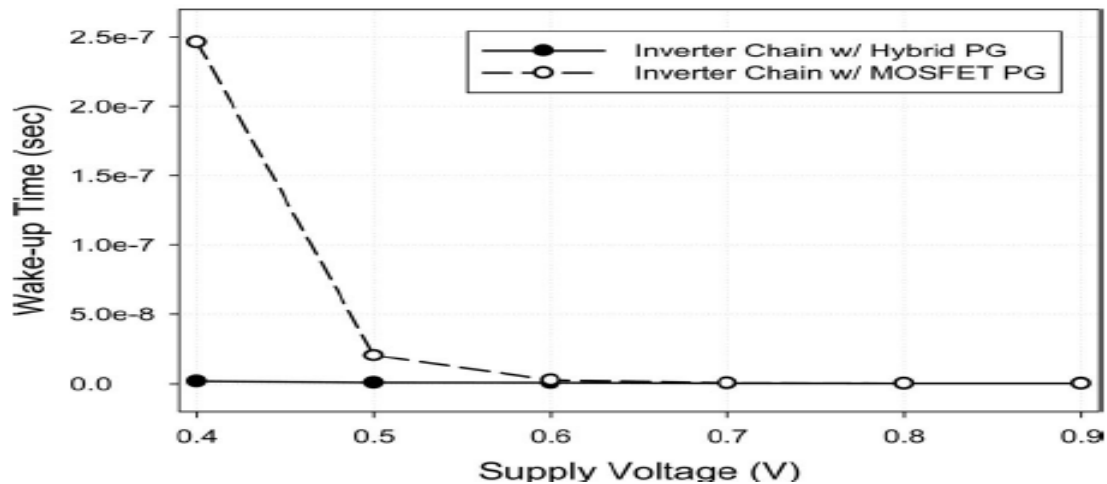


Fig. 12. Wakeup time dependence of power gating on supply voltage[14]

IV. CONCLUSION

We have presented a review of different power gating schemes employed for leakage power reduction. Superior properties of emerging nano-electronic devices such as carbon nanotube field effect transistors and nano-electromechanical switches can be utilized for leakage power reduction in battery powered ultra low power systems. CNFETs and NEMFETs can be effectively used as a replacement for conventional CMOS sleep transistors. Hybrid CNFET-CMOS or NEMS-CMOS based power gating schemes provide considerable improvement over conventional power gating schemes.

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