

# **Multi-Level Inverter Capable Of Power Factor Control with DC Link Switches**

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**ABSTRACT:** this paper proposes a new multi-level inverter topology based on a H-bridge structure with four switches connected to the dc-link. Based on a POD (Phase opposition disposition) modulation method, a new PWM method which requires only one carrier signal is suggested. The switching sequence to balance the capacitor voltage is also considered. In addition to these, the proposed topology requires minimum number of component count to increase the number of voltage level. Operating principle of the proposed inverter is verified through simulation and experiment.

## **I. INTRODUCTION**

Due to the increasing demand on the renewable energy sources, grid connected inverter systems are becoming more and more important than ever before. For grid connected operation, the inverter should meet the following requirements.

1. The inverter has to generate a pure sinusoidal output voltage.
2. The inverter output current should have low total harmonic distortion (THD).

Traditionally, two-level PWM inverter is used for grid-tied operation. In case of a two-level inverter, the switching frequency should be high or the inductance of the output filter inductor need to be big enough to satisfy the required THD. To cope with the problems associated with the two-level inverter, multi-level inverters (MLIs) are introduced for gridconnected inverter. Several MLI topologies have been suggested so far and they can be mainly classified as three types in Fig. 1; neutral point clamped (NPC), flying capacitor (FC), and cascaded type [3-5].

Advantage of the MLIs is that their switching frequency and device voltage rating can be much lower than those of a traditional two-level inverter for the same output voltage. Therefore, IGBT switching loss can be reduced significantly and thus the inverter system efficiency can be increased [6-8].

In this paper, a circuit based on a H-bridge topology with four switches connected to the dc-link is proposed as a MLI topology. Fig. 2 shows the proposed MLI. Also it is simple because the proposed PWM method uses one carrier signal for generating PWM signals. In addition, the switching sequence considering the voltage balance of dc-link was proposed. Finally, the proposed topology of the multi-level inverter is verified by showing the feasibility through the simulation and the experiment.

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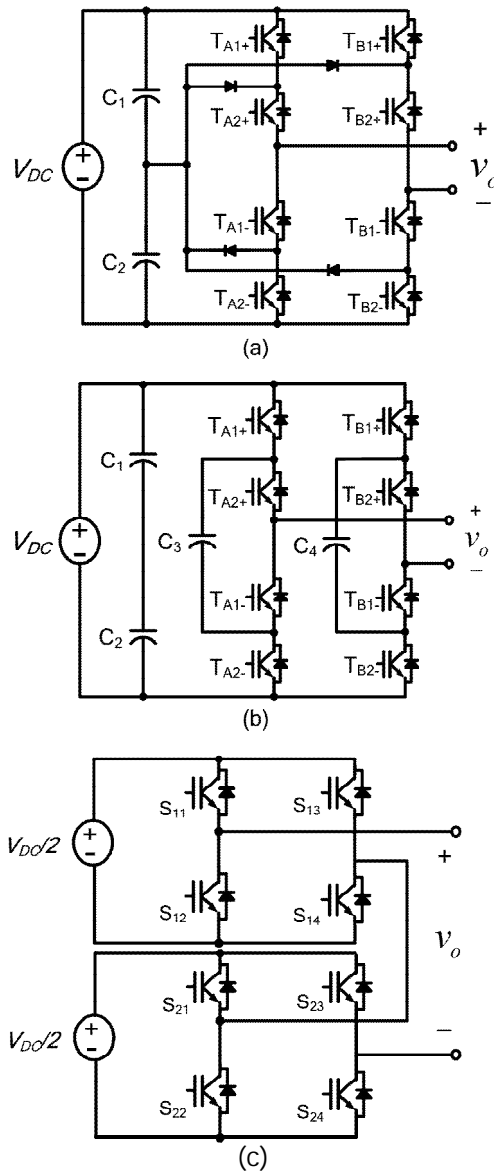


Fig. 1. Topologies of multi-level inverters. (a) neutral point clamped (NPC) type. (b) Flying capacitor (FC) type. (c) Cascade type.

## II. PROPOSED MULTI-LEVEL INVERTER

### A. Topology of multi-level inverter

As shown in Fig. 2, the proposed MLI is composed of two dc-link capacitors ( $C_1$ ,  $C_2$ ) and four switching devices ( $T_A^+$ ,  $T_A^-$ ,  $T_B^+$ ,  $T_B^-$ ) comprising a H-bridge, and four active switches ( $T_P^+$ ,  $T_P^-$ ,  $T_N^+$ ,  $T_N^-$ ) located between dc-link and H-bridge. The voltage across the switching devices in the dc-link ( $T_P^+$ ,  $T_P^-$ ,  $T_N^+$ ,  $T_N^-$ ) is  $V_{DC}/2$  and operated at a switching

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frequency. Whereas, voltage across the switching devices in the H-bridge ( $T_A^+$ ,  $T_A^-$ ,  $T_B^+$ ,  $T_B^-$ ) is  $V_{DC}$  and the switches ( $T_A^+$ ,  $T_A^-$ ,  $T_B^+$ ,  $T_B^-$ ) are switched at a frequency of the fundamental component of the output voltage (e.g. 50 or 60 Hz). Thus, the dc-link switches ( $T_P^+$ ,  $T_P^-$ ,  $T_N^+$ ,  $T_N^-$ ) and the Hbridge switches ( $T_A^+$ ,  $T_A^-$ ,  $T_B^+$ ,  $T_B^-$ ) can be strategically selected based on the rated power of the inverter system in order to reduce system cost and increase efficiency. Table I shows the output voltage according to the switching states.

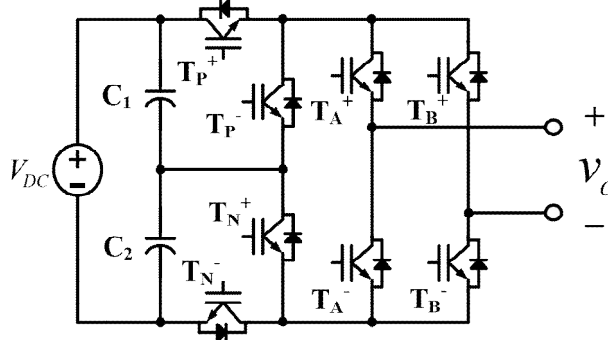


Fig. 2. Proposed single-phase multi-level inverter topology.

TABLE I  
Output voltage according to switching states

Output voltage ( $V_o$ )	Switching condition					
	TP+	TP-	TN+	TN-	TA+, TB-	TA-, TB+
$V_{DC}$	ON	OFF	OFF	ON	ON	OFF
$V_{DC}/2$	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
$-V_{DC}$	OFF	ON	OFF	ON	OFF	ON
$-V_{DC}/2$	ON	OFF	ON	OFF	OFF	ON
$-V_{DC}$	ON	OFF	OFF	ON	OFF	ON

TABLE II  
Operating mode of the proposed MLI

Operating mode	Reference voltage range	Output voltage
Mode 1	$V_c \leq v_{ref} < 2V_c$	$V_{DC}/2$ or $V_{DC}$
Mode 2	$0 \leq v_{ref} < V_c$	0 or $V_{DC}$
Mode 3	$-V_c \leq v_{ref} < 0$	$-V_{DC}/2$ or 0
Mode 4	$-2V_c \leq v_{ref} < -V_c$	$-V_{DC}$ or $-V_{DC}/2$

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### B. Operating modes and proposed PWM strategy

The output voltage of the proposed MLI shown in Fig. 2 has five levels ( $V_{DC}$ ,  $V_{DC}/2$ ,  $0$ ,  $-V_{DC}/2$ ,  $-V_{DC}$ ) according to the switching states of the inverter. There are four operation modes depending on the instantaneous value of the reference voltage,  $v_{ref}$  and the maximum value of the carrier signal,  $V_c$  (see Fig. 4). Table II shows the possible inverter output voltage level according to the operating mode.

In case of the N-level NPC type multi-level inverter, N-1 triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range  $+V_{DC}$  to  $-V_{DC}$ . A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. Three dispositions of the carrier signal are considered to generate the PWM signal [9-11].

- 1) Phase disposition (PD); where all carriers are in phase.
- 2) Alternative phase opposition disposition (APOD); where each carrier is phase shifted by 180 degree from its adjacent carrier.
- 3) Phase opposition disposition (POD); where the carriers above zero voltage are 180 degree out of phase with those below zero voltage.

Fig. 3 shows the reference signal and the carrier signal arrangements for PD modulation, POD modulation, and APOD modulation.

A new PWM strategy based on POD modulation which requires only a single carrier signal ( $v_{carrier}$ ) is proposed and the detailed PWM strategy is depicted in Fig. 4. If the

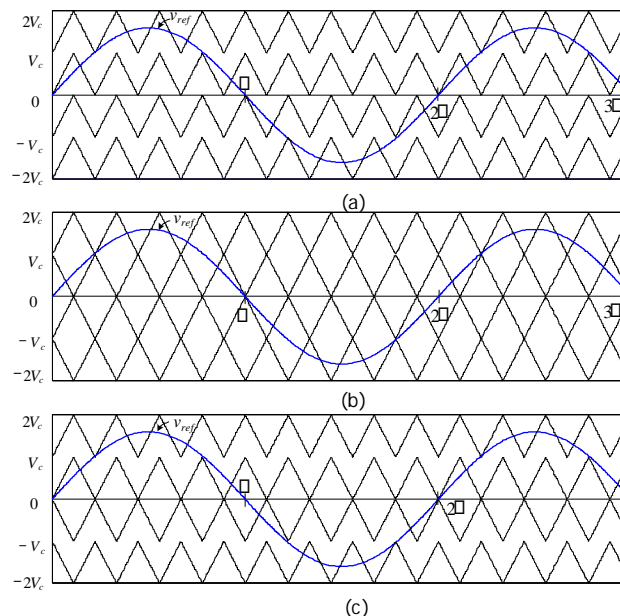


Fig. 3. Carrier and reference signal arrangements for: (a) Phase disposition (PD). (b) Alternative phase opposition disposition (APOD). (c) Phase opposition disposition (POD).

reference signal is positive, then the switch pair ( $T_A^+$ ,  $T_B^-$ ) are turned on, and if it is negative, then the switch pair ( $T_A^-$ ,  $T_B^+$ ) are turned on. Thus the switches composing the H bridge inverter turned on and turned off once during the period of the reference signal. The voltage across the switch at blocking state is  $V_{DC}$ . The switches ( $T_P^-$ ,  $T_N^+$ ) are operated

complementally to the switches ( $T_P^+$ ,  $T_N^-$ ). The generation of the PWM signal for dc-link switches ( $T_P^+$ ,  $T_N^-$ ) can be explained as follows.

- Mode 1: a signal subtracted from the reference signal by

$V_c$  is compared with the carrier signal. If  $v_{ref} - V_c > v_{carrier}$ , then all switches  $T_P^+$  and  $T_N^-$  are turned on. If  $v_{ref} - V_c < v_{carrier}$ , then the switch  $T_P^+$  or  $T_N^-$  is turned off alternately.

- Mode 2: the reference signal is directly compared with a carrier signal. If  $v_{ref} > v_{carrier}$ , then the switch  $T_P^+$  or  $T_N^-$  is turned on alternately. If  $v_{ref} < v_{carrier}$ , then all switches  $T_P^+$  and  $T_N^-$  are turned off.

- Mode 3:  $-v_{ref}$  is directly compared with a carrier signal.

If  $-v_{ref} > v_{carrier}$ , then the switch  $T_P^+$  or  $T_N^-$  is turned on alternately. If  $-v_{ref} < v_{carrier}$ , then all switches  $T_P^+$  and  $T_N^-$  are turned off.

- Mode 4: a signal subtracted from  $-v_{ref}$  by  $V_c$  is compared with the carrier signal. If  $-v_{ref} - V_c > v_{carrier}$ , then all switches  $T_P^+$  and  $T_N^-$  are turned on. If  $-v_{ref} - V_c < v_{carrier}$ , then the switch  $T_P^+$  or  $T_N^-$  is turned off alternately.

Only one carrier signal is used to generate eight PWM signals in the proposed PWM method. Thus it is quite simple.

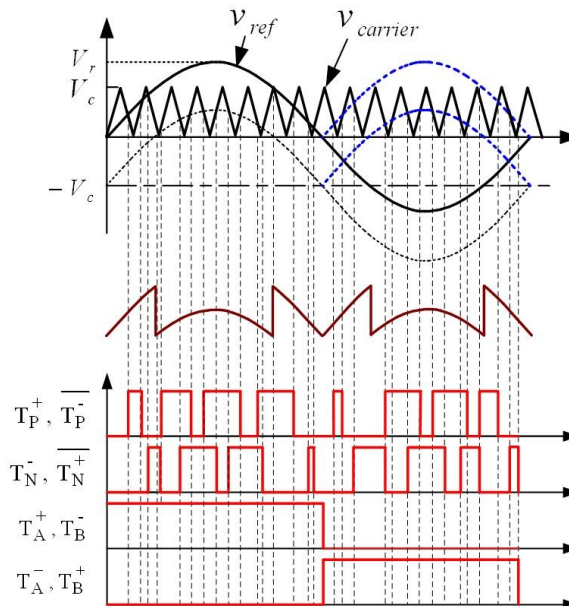


Fig. 4. PWM strategy based on POD with single carrier signal

### C. Voltage balancing of dc-link capacitor

One of the important issues about multi-level inverter is the voltage balance of the dc-link capacitor. The voltage of capacitor  $C_1$  and  $C_2$  should be equally balanced to  $V_{DC}/2$ . However the midpoint voltage fluctuates when  $C_1$  and  $C_2$  charge and discharge continuously. If the capacitor voltage is unbalanced, the output voltage becomes unsymmetrical and it results in a high harmonic content in the load current.

To solve this problem, the switching state should be selected appropriately in Fig. 5. If only one switch in a dc-link is turned on, the output voltage becomes  $V_{DC}/2$ . In order to balance the voltage of dc-link capacitor, dc-link switches ( $T_P^+$ ,  $T_N^-$ ) are alternately turned on at mode 2, and alternately turned off at mode 1. And switches ( $T_P^-$ ,  $T_N^+$ ) are operated complementally to switches ( $T_P^+$ ,  $T_N^-$ ). Therefore, the switching sequence of mode 1 is (a)-(b)-(a)-(c), and the switching sequence of mode 2 is (d)-(b)-(d)-(c). The switching sequence of mode 3 and mode 4 are similar that of mode 1 and mode 2. The switching sequence of mode 3 is (h)-(f)-(h)(g), and the switching sequence of mode 4 is (e)-(f)-(e)-(g).

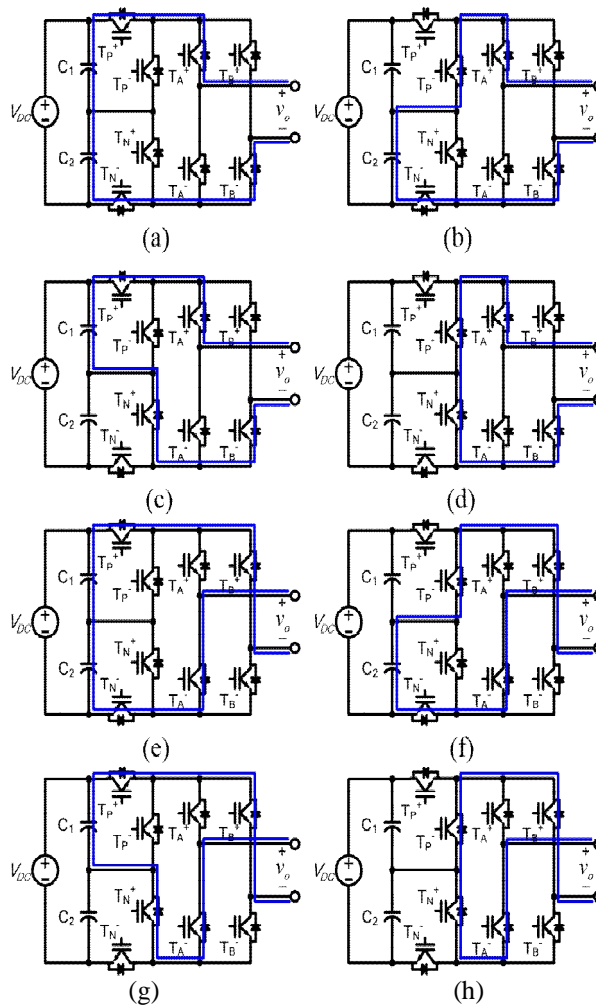


Fig. 5. Switching states of the proposed inverter in one cycle. (a) state 1 :  $v_o = 0$ . (b) state 2 :  $v_o = V_{DC}/2$ . (c) state 3 :  $v_o = V_{DC}/2$ . (d) state 4 :  $v_o = V_{DC}$ . (e) state 5 :  $v_o = 0$ . (f) state 6 :  $v_o = -V_{DC}/2$ . (g) state 7 :  $v_o = V_{DC}/2$ . (h) state 8 :  $v_o = V_{DC}$ .

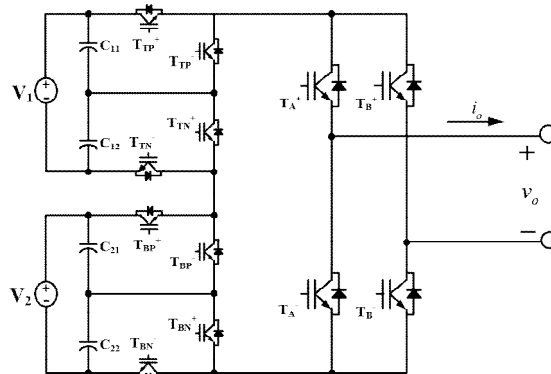


Fig. 6. Proposed 9-level inverter topology

#### D. Extension to 9-level inverter

It should be noted that although the number of the switching devices in the proposed 5-level inverter (shown in Fig. 2) is the same as that of the conventional cascaded H-bridge MLI, the switches ( $T_A^+$ ,  $T_A^-$ ,  $T_B^+$ ,  $T_B^-$ ) in the proposed MLI are switched at a low frequency (60 Hz). Moreover, unlike the cascaded H-bridge MLI, the proposed 5-level inverter requires only one isolated voltage source,  $V_{DC}$ .

In order to maximize the effectiveness of the proposed MLI, 9-level inverter which was extended from 5-level inverter shown in Fig. 2 is also proposed in this paper and the overall circuit diagram is shown in Fig. 6. As shown in Fig. 6, in case of 9-level inverter, the proposed inverter requires less active devices than 9-level cascaded H-bridge MLI. Therefore, number of switching devices in the proposed MLI can be reduced significantly as the number of voltage level increases.

### III. SIMULATION AND EXPERIMENTAL RESULTS

The proposed 5-level inverter is tested to verify the operating principle of the proposed MLI. The LC filter is inserted between the output of the inverter and the load. Electrical specifications of the proposed inverter are summarized in Table III. Fig. 7 and 8 show simulation waveforms of the proposed inverter in 5-level. Fig. 7 shows the waveforms of the inverter output voltage, load voltage and the load current when the power factor becomes unity. Fig. 8 shows the waveforms of the inverter output voltage, load voltage and the load current during the lagging power factor.

TABLE III  
Electrical specifications of the proposed single-phase 5-level inverter

dc-link voltage	200V
Output voltage	110 $V_{rms}$
dc-link capacitor	2200 $\mu F$
Filter inductor ( $L_f$ )	300 $\mu H$
Filter capacitor ( $C_f$ )	150 $\mu F$
Switching frequency ( $f_{sw}$ )	5 kHz
Output frequency ( $f_o$ )	60 Hz



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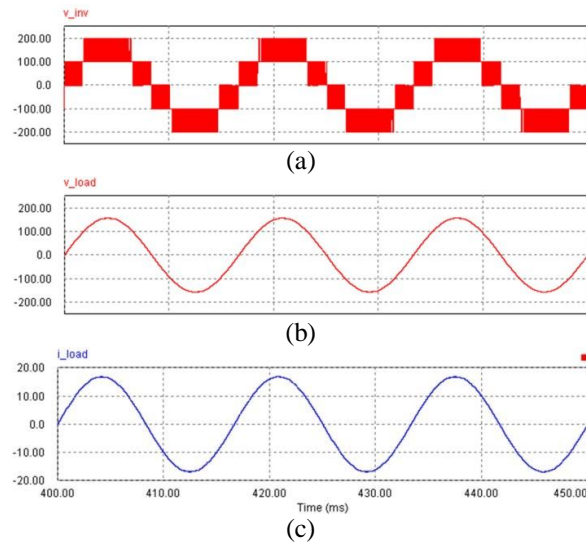


Fig. 7. Waveforms of 5-level inverter (Load :  $R = 9.3 \Omega$ ). (a) Output voltage of the inverter. (b) load voltage. (c) load current.

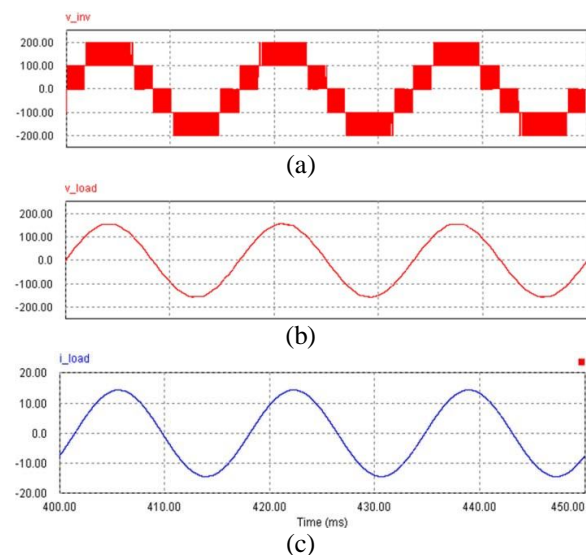


Fig. 8. Waveforms of 5-level inverter (Load :  $R = 9.3 \Omega$ ,  $L = 14.9\text{mH}$ ). (a) Output voltage of the inverter. (b) load voltage. (c) load current.

Based on the simulation results, the experiment was conducted. Rating and the parameters of the system which was used in the experiment are the same with those of the simulation. Configuration for the experiment is shown in Fig. 9. Fig. 10 shows that the capacitor voltages ( $V_{C1}$ ,  $V_{C2}$ ) are controlled constantly. The capacitor voltages ( $V_{C1}$ ,  $V_{C2}$ ) are well balanced at the voltage of 100[V]. Fig. 11 shows the waveforms of the inverter output voltage, load voltage and the load current. The inverter output voltage is 5-level voltage and the load current and the load voltage waveforms are closer to the sinusoidal waveform. Experimental output waveforms can be found consistent with the simulation result.



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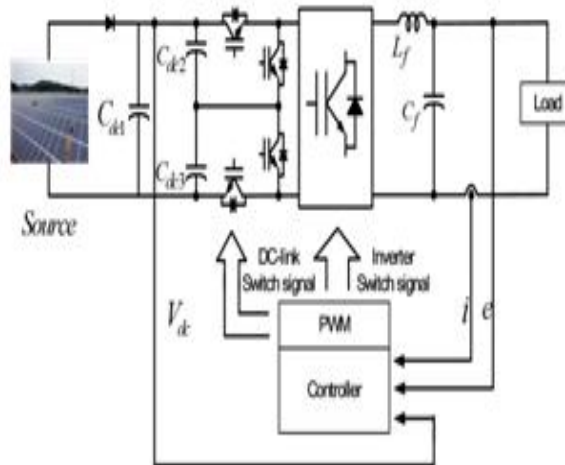


Fig. 9. Single phase inverter system

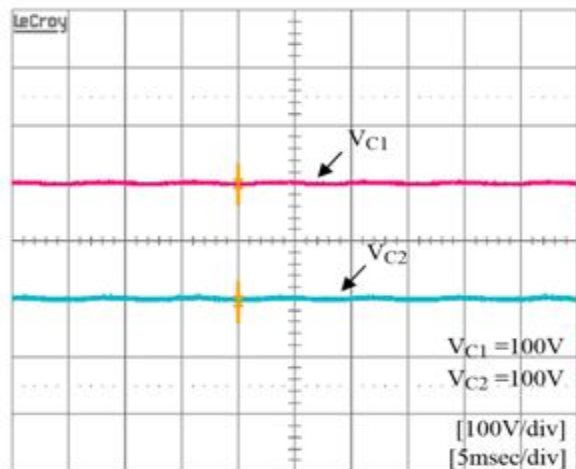


Fig. 10. Voltage balancing waveforms of de-link capacitor ( $C_1, C_2$ ).

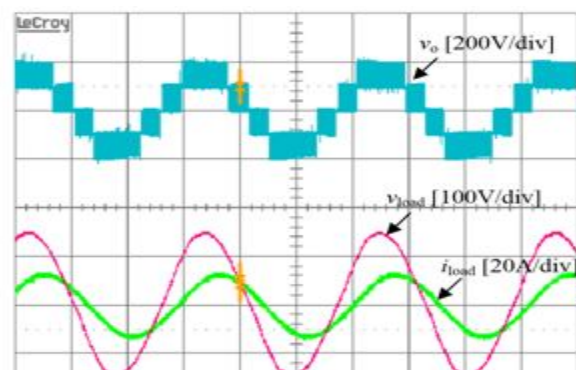


Fig. 11. Waveforms of 5-level inverter ( Load :  $R = 9.3 \Omega, L = 14.9\text{mH}$ )

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## IV. CONCLUSION

This paper proposed a new multi-level inverter topology based on a H-bridge inverter with four switches connected to the dc-link. The proposed MLI has the following advantages over the conventional inverters.

1. Number of devices of the proposed multi-level inverter is fewer than that of the conventional multi-level inverters. Therefore, the proposed system is more reliable and cost competitive than the conventional two-level and multilevel inverters.
2. The four switches ( $T_A^+$ ,  $T_A^-$ ,  $T_B^+$ ,  $T_B^-$ ) in the H-bridge are switched at a low frequency (e.g. 60 Hz). Therefore, switching loss of The four switches ( $T_A^+$ ,  $T_A^-$ ,  $T_B^+$ ,  $T_B^-$ ) is almost negligible.
3. Only one carrier signal is required to generate the PWM signals for 4 switching devices ( $T_P^+$ ,  $T_P^-$ ,  $T_N^+$ ,  $T_N^-$ ).
4. The proposed topology can be easily extended to 9-level or higher level with minimized active device component count.

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