

# Characterization of InAs Composite Channel M-HEMT For Thz Frequency Applications

R.Saravanakumar<sup>1</sup>, A.Sarathi<sup>2</sup>

Associate Professor, Department of Electronics and Communication Engineering, SKP Engineering College  
Tiruvannamalai, Tamilnadu, India<sup>1</sup>

Assistant Professor, Department of Electronics and Communication Engineering, SKP Engineering College  
Tiruvannamalai, Tamilnadu, India<sup>2</sup>

**ABSTRACT:** We have designed a 30 nm InAs channel Inverted-Type HEMTs with outstanding logic performance, scalability and high frequency characteristics. The motivation for this work is the demonstration of reduced gate leakage current in the Inverted HEMT structure and investigated the trade- offs involved in thinning down the channel of III-V FETs with the ultimate goal of enhancing the electrostatic integrity and scalability of these devices. To do so, we have designed InAs HEMTs with a channel thickness of  $t_{ch} = 10$  nm. But this reduced channel size somehow poorer transport in the channel which leads to lower electron mobility in the epitaxial structure. So we inserted InAs in InGaAs sub-channel and made it as composite channel. The simulated devices show excellent  $L_g$  scalability down to 30 nm.  $L_g = 30$  nm devices have been simulated with exhibit  $g_m = 1.8mS/\mu m$ . More significantly, the removal of dopants from the barrier suppresses forward gate leakage current by over 100X when compared with equivalent normal HEMTs. The  $L_g = 30$  nm devices also feature record high-frequency characteristics for an inverted- type HEMT design with  $f_T = 400$  GHz and  $f_{max} = 650$  GHz.

## I.INTRODUCTION

As conventional Si CMOS scaling approaches the end of the roadmap, III-V based MOSFETs are seriously being considered as an alternative technology to continue Moore's law [1- 2]. In the quest to map the potential of III-Vs for future CMOS applications, the High Electron Mobility Transistor (HEMT) has emerged as a valuable model system to understand relevant physics issues. The High Electron Mobility Transistor (HEMT) is a hetero structure Field Effect Transistor (FET). Its principle is based on a hetero junction which consists of at least two different semiconducting materials brought into intimate contact. Because of the different band gaps and their relative alignment to each other, band discontinuities occur at the interface between the semiconducting materials. These discontinuities are referred to as the conduction and valence band offsets  $\Delta E_c$  and  $\Delta E_v$ . By choosing proper materials and compositions thereof, the conduction band offset can form triangular shaped potential well confining electrons in the horizontal direction. Within the well electrons can only move in a two- dimensional plane parallel to the hetero interface and are therefore referred to as a two-dimensional electron gas (2DEG). To determine the exact shape of the conduction and valence bands, the Schrödinger and Poisson equations must be solved self-consistently. It is illustrated in Figure 1 and 2.

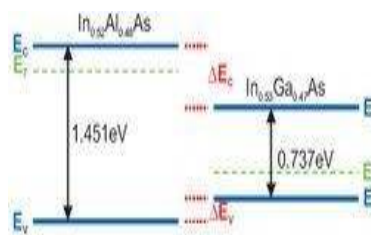


Figure 1. Diagram of the band structures of two InAlAs and InGaAs at the equilibrium.

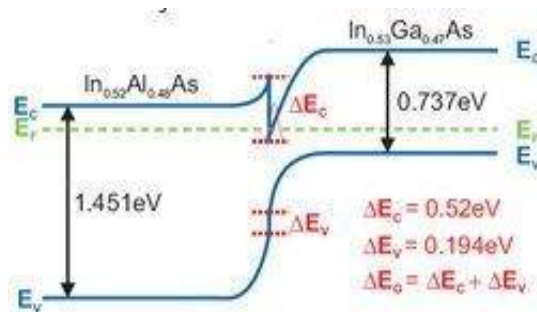


Figure 2. Semiconductors in contact at the equilibrium. A 2DEG is formed at the interface.

## II. GENERAL STRUCTURE OF InP HEMT

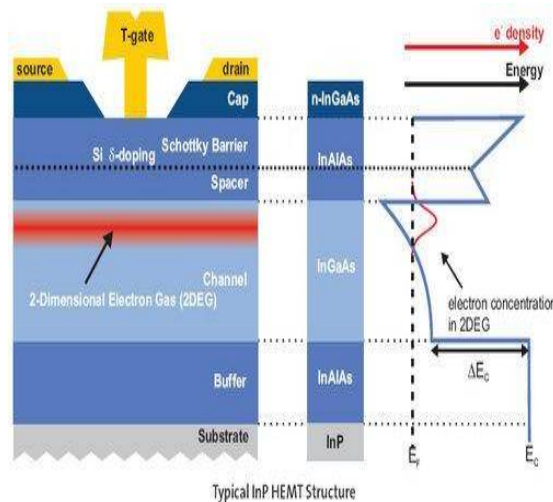


Figure 3: General InP HEMT structure

Taking advantage of the fact that the 2DEG offers exceptional high carrier mobility's compared to bulk material, a typical InPHEMT has the following layer structure:

1) Silicon  $\delta$ -doping layer. Highly doped layer with only few atomic layers thickness. Located between the Schottky-Barrier and Spacer layer. Acting as a donor of charge carriers, it provides electrons to the channel. Since electrons tend to occupy the lowest allowed energy state, they drain into the potential well and form the confined 2DEG in the channel. A high  $\delta$ -doping level provides high electron densities in the channel and therefore results in high transconductances, current densities and cut-off frequencies.

2) The Spacer layer assures the separation between the electrons and their positively charged Si-donors, reducing impurity scattering and hence enhancing electron mobility.

3) The Schottky-Barrier layer, in contrast to the Ohmic source and drain contacts, provides a so-called Schottky contact between gate-metal and semiconductor material with a rectifying characteristic. It prevents large

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currents from flowing through the gate and limits tunneling to the channel.

4) Channel properties have a major impact on the device performance. This is why InGaAs, with its excellent electron mobility properties at room and cryogenic temperatures, is the material of choice.

The special T-shape of the gate helps minimize the gate resistance by enlarging the cross section while maintaining a small foot-print and thus a small gate length.

### III. PROPOSED STRUCTURE

Figure.4 shows a cross-sectional view of the devices simulated in this work. Our devices are built in an InP substrate. Here the hetero structures are formed through the wideband gap material InAlAs and lower band gap material InGaAs. Recent research on InAlAs/ InGaAs HEMTs has demonstrated that these devices exhibit excellent logic characteristics down to about 60nm. This has been accomplished by thinning down the InAlAs barrier ( $t_{ins}$ ) to the 3-4 nm range. Further lateral scaling is going to require scaling of the channel thickness ( $t_{ch}$ ) as well. However as  $t_{ch}$  scales down, carrier transport in the channel deteriorates. Mainly, as a consequence of the increased carrier scattering mechanisms. In this paper we explored a solution to this problem through the introduction of pure thin layer of InAs in the channel. InAs is a very attractive material with an electron mobility as high  $20000\text{cm}^2/\text{v.s}$  at room temperature.

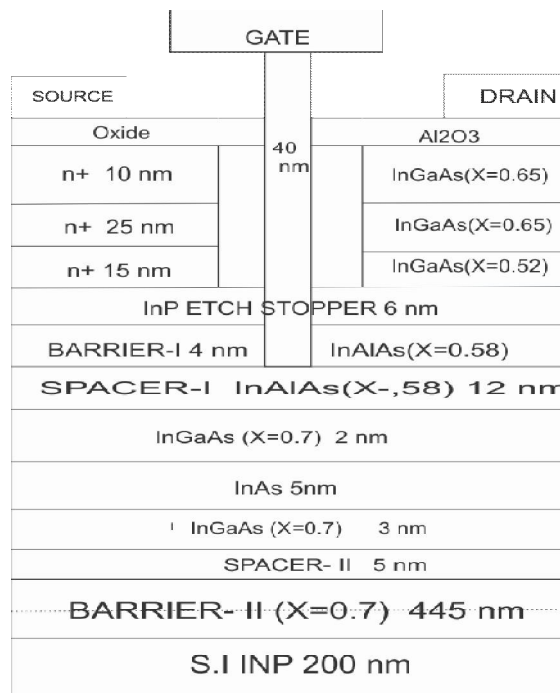


Figure.4 Cross-sectional view of the device.

The introduction of InAs is expected to mitigate the deleterious effect of channel thickness scaling. And also our device features an InAlAs/InGaAs double-heterostructure design where the upper Si-doping is located further away from the channel than in conventional designs (8 nm vs. about 3 nm). As a result, after a triple recess process the dopant layer is eliminated in the intrinsic device resulting in a dopant-free InAlAs barrier. This gives rise to a conduction band shape for the barrier that, for the same sheet carrier concentration, is more rectangular than in

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the conventional design, as shown in Figure.5. This should significantly suppress gate leakage current, especially in the forward gate bias regime.

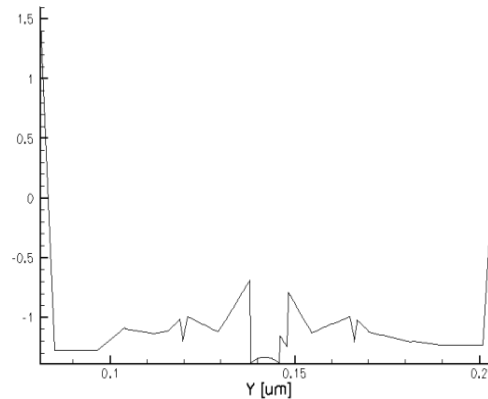


Figure.5 Conduction band profile.

Figure 6. represents the Structure of simulated Composite channel HEMT. Plot of  $f_{max}$  as a function of  $V_{gs}$  at  $V_{ds}=0.5$  V for  $L_g=30$  nm. Excellent values of  $f_T$  and  $f_{max}$  have been obtained and shown in Figure.7. This is due to the improved output conductance characteristics. The improvement in transistor scaling with insulator scaling is evident clearly in the transconductance shown in Figure.8 Most important that the peak  $g_m$  continues by scaling down the  $L_g$ .

Figure.6 Structure of simulated Composite channel HEMT

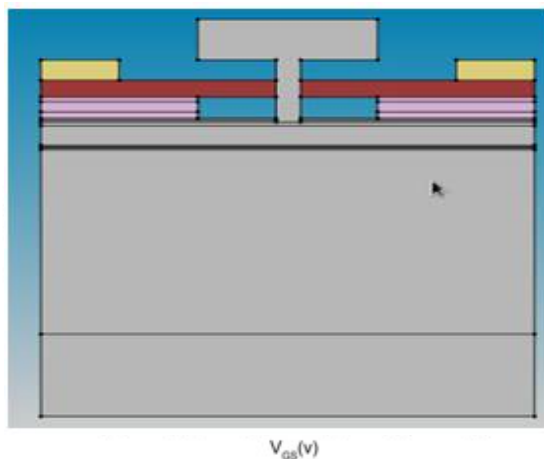


Figure.7 Bias dependence of  $f_{max}$  for  $L_g=30$  nm.

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Figure.9 shows excellent subthreshold characteristics of composite channel HEMT over normal sub-channel HEMT. The device exhibits lower off state current and gate leakage current. Figure 10. shows the output characteristics of a Composite channel HEMT with 30 nm of gate length. The device exhibits excellent pinch-off and saturation characteristics.

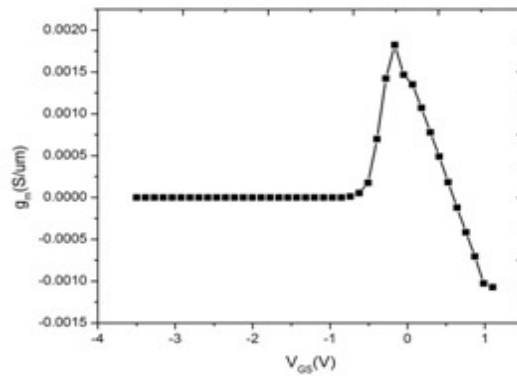


Figure.8 Transconductance characteristics of HEMT

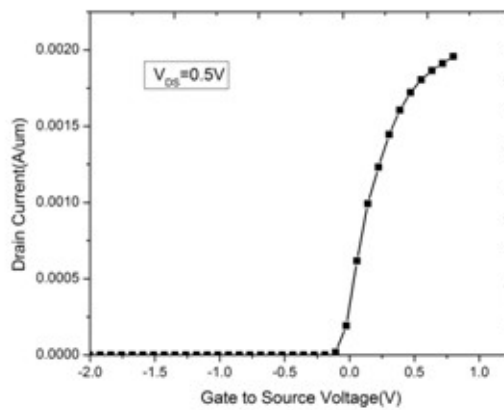


Figure9. Drain characteristics of composite channel HEMT.

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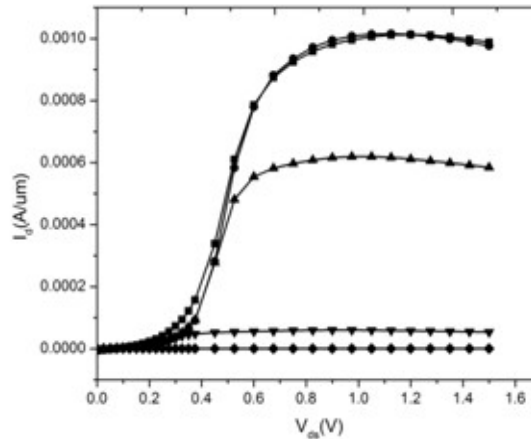


Figure 10. Output characteristics of composite channel HEMT.

## IV. CONCLUSION

We have demonstrated 30nm Composite channel HEMT which exhibit  $g_m = 1.8 \text{ mS}/\mu\text{m}$ . More significantly, the removal of dopants from the barrier suppresses forward gate leakage current by over 100X when compared with equivalent normal HEMTs. The  $L_g = 30 \text{ nm}$  devices also feature record high-frequency characteristics for an inverted-type HEMT design with  $f_T = 400 \text{ GHz}$  and  $f_{\text{max}} = 650 \text{ GHz}$ . InAs is, needed a channel material with great potential for beyond Si CMOS Logic applications.

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