

VLSI Implementation of WiMAX Channel without Using Floor Function

Mamatha T Chinchali¹, Maltesh Bjantri²

P.G. Student, Department of ECE, Shridevi Engineering College, Sira road, Karnataka, India¹

Associate Professor, Department of ECE, Shridevi Engineering College, Sira road, Karnataka,, India²

ABSTRACT: The Worldwide Interoperability for Microwave Access (WiMAX) is currently one of the hottest technologies in wireless. The Institute of Electrical and Electronics Engineers (IEEE) 802 committee, which sets networking standards such as Ethernet (802.3) and WiFi (802.11), has published a set of standards that define WiMAX. IEEE 802.16-2004. These operate in the 2.5GHz, 3.5GHz and 5.8 GHz frequency bands. WiMAX, is based on an RF technology called Orthogonal Frequency Division Multiplexing (OFDM), which is a very effective means of transferring data when carriers of width of 5MHz or greater can be used. WiMAX is a standard-based wireless technology that provides high throughput broadband connections over long distance. WiMAX can be used for a number of applications, including “last mile” broadband connections, hotspots and high-speed connectivity for business customers.

This work proposes an algorithm on address generation circuitry of Deinterleaver using QPSK and 16 QAM modulations for WiMAX transceiver. The floor function associated with the implementation of FPGA is very difficult in IEEE 802.16e standard. The requirement of floor function can be eliminated by using a simple mathematical algorithm. The main aim of the work is to concentrate on performance improvement by reducing interconnection delay, lesser power consumption, and efficient resource utilization by comparing with prevailing technique. This work focuses on removing the complexities and excess hardware involvement in the implementation of the permutations involved in Deinterleaver designs as defined by IEEE 802.16.

KEYWORDS: Floor function, Modulation schemes, Interleaver, Deinterleaver.

I. INTRODUCTION

Broadband wireless access (BWA) is continuously becoming a more challenging competitor to the conventional wired last mile access technologies. IEEE has developed standards for mobile BWA (IEEE 802.16e) popularly referred to as mobile WiMAX. The channel interleaver employed in the WiMAX transceiver plays a vital role in minimizing the effect of burst error. The floor function associated with the implementation of the steps, required for the permutation of the incoming bit stream in channel interleaver/deinterleaver for IEEE 802.16e standard is very difficult to implement in FPGA. In this brief, a novel, low-complexity, high-speed, and resource-efficient address generator for the channel deinterleaver used in the WiMAX transceiver eliminating the requirement of floor function is proposed. Very few works related to hardware implementation of the interleaver/deinterleaver used in a WiMAX system is available in the literature.

II. RELATED WORK

1. Novel design of WiMAX multimode interleaver for efficient FPGA implementation using finite state machine based address generator.

Author: Bijoy Kumar Upadhyaya, and Salil Kumar Sanyal

This paper presents a full FPGA implementation of WiMAX multimode interleaver. It proposes a novel finite state machine based address generator used for generation of write and read addresses for the interleaver memory. The

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Vol. 4, Issue 4, April 2015

interleaver memory is implemented using dual port Block RAM of Xilinx Spartan-3 FPGA. The presented circuit supports all the code rates and modulation schemes permitted under IEEE 802.16e standard. The simulation results endorse the correct operation of both address generator and interleaver as a whole. The novelty of our approach includes higher operating frequency and better resource utilization in FPGA.

2. 2-D Realization of WiMAX Channel Interleaver for Efficient Hardware Implementation.

Author: Rizwan Asghar and Dake Liu

This work provides the mathematical transformation of the one dimensional WiMAX interleaver equations mentioned in the standard to two dimensional space. This 2D transformation leads to optimized hardware architecture for address generation of the WiMAX interleaver. Due to presence of modulus and floor operators within the interleaver functions use of standard algebraic rules does not work always. Thus the structural analysis along with progressive generation of the equivalent set of equations for 2D space is used to reach to the low cost solution.

3. Simulation of WiMAX Physical Layer: IEEE 802.16e.

Author: M.A. Mohamed, F.W. Zaki, R.H. Mosbeh

This paper described current trends in WiMAX systems for achieving high speed mobile wireless access services and outlined the technologies supporting these systems. The performance of the WiMAX-PHY layer based on the IEEE 802.16e standard, was evaluated and assessed at different: (i) modulation schemes; (ii) coding rates; (iii) FEC coding schemes, and (iv) noise levels. As a result of the comparative study, it was found that: when channel conditions are poor, energy efficient schemes such as BPSK or QPSK were used and as the channel quality improves, 16-QAM or 64-QAM was used. It adjusts the modulation method almost instantaneously for optimum data transfer, thus making a most efficient use of the bandwidth and increasing the overall system capacity. Actually, this simulation phase was done as a first step in implementing WiMAX networks using field programmable gate array (FPGA) systems.

III. SYSTEM DEVELOPMENT

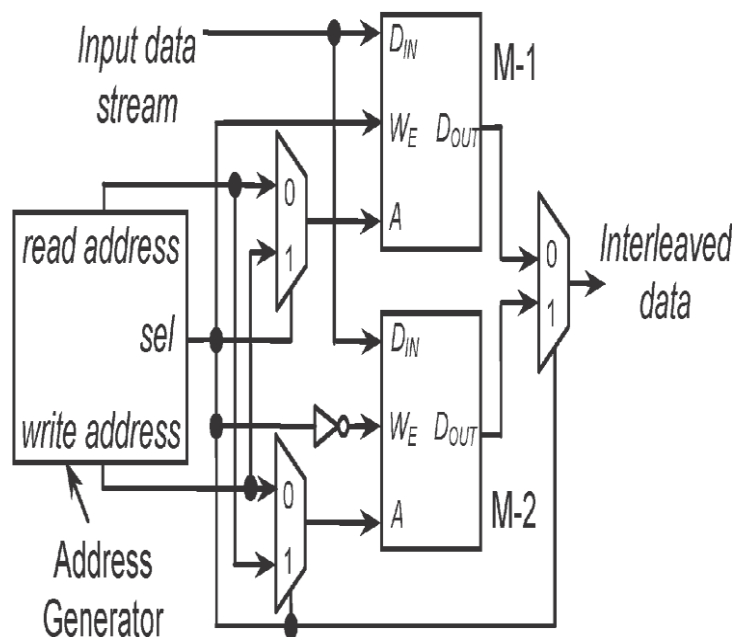


Fig. 1. Interleaver/deinterleaver structure.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

Two dimensional block interleaver/deinterleaver structure, which is used as a channel interleaver/deinterleaver in the WiMAX system, is described in Fig.3.2.1 It has two memory blocks, namely, $M-1/2$ and an address generator. In block interleaving, when one memory block is being written, the other one is read, and vice versa. When $sel = 1$, write enabled signal WE of $M-1$ is active. During this period, the input data stream is written in $M-1$ as it receives the write addresses. Simultaneously, an interleaved data stream is read from $M-2$ as it is supplied with the read addresses. After the memory blocks are written/read up to the desired location as specified by interleaver depth, the status of sel signal is changed to swap the read/write operation.

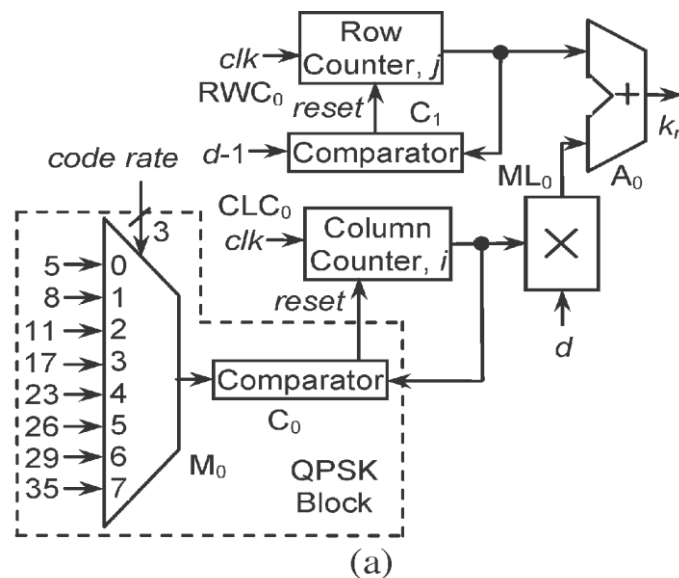


Fig (a) Hardware structure of the address generator for QPSK.

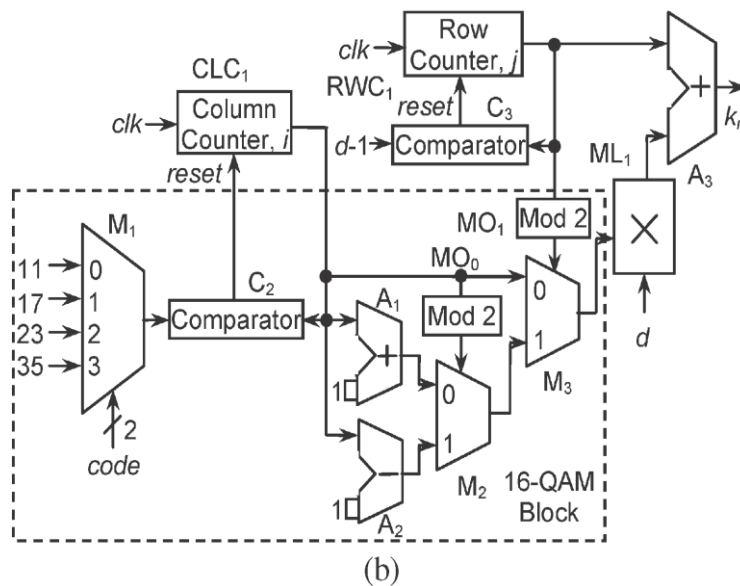


Fig. (b) Hard- ware structure of address generator for 16-QAM.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

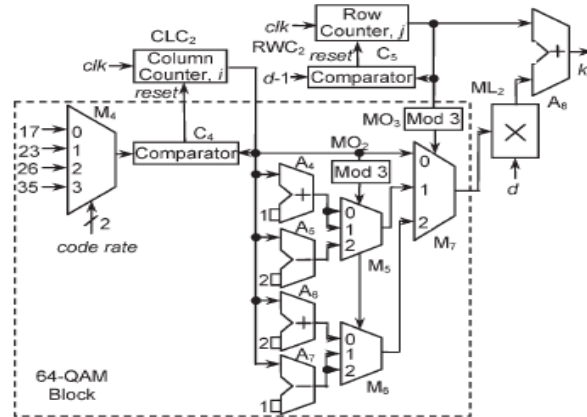


Fig.(c) Hardware structure of address generator for 64-QAM.

| N_{cbps} , code rate and modulation type | De-interleaver addresses | | | | |
|---|--------------------------|----|----|----|----|
| $N_{cbps} = 96$ -bits, $\frac{1}{2}$ code rate, QPSK | 0 | 16 | 32 | 48 | 64 |
| | 1 | 17 | 33 | 49 | 65 |
| | 2 | 18 | 34 | 50 | 66 |
| | 3 | 19 | 35 | 51 | 67 |
| $N_{cbps} = 192$ -bits, $\frac{1}{2}$ code rate, 16-QAM | 0 | 16 | 32 | 48 | 64 |
| | 17 | 1 | 49 | 33 | 81 |
| | 2 | 18 | 34 | 50 | 66 |
| | 19 | 3 | 51 | 35 | 83 |
| $N_{cbps} = 576$ -bits, $\frac{3}{4}$ code rate, 64-QAM | 0 | 16 | 32 | 48 | 64 |
| | 17 | 33 | 1 | 65 | 81 |
| | 34 | 2 | 18 | 82 | 50 |
| | 3 | 19 | 35 | 51 | 67 |

Table 2: First four rows and five columns of deinterleaver sample addresses for three code rates and modulation types

| Row no.(j) | Column no. (i) → | 0 | 1 | 2 | 3 | 4 |
|------------|---|------------|------------|------------|------------|------------|
| 0 | $N_{cbps} = 96$ -bits, $\frac{1}{2}$ code rate, QPSK | $d.0+0=0$ | $d.1+0=16$ | $d.2+0=32$ | $d.3+0=48$ | $d.4+0=64$ |
| 1 | | $d.0+1=1$ | $d.1+1=17$ | $d.2+1=33$ | $d.3+1=49$ | $d.4+1=65$ |
| 2 | | $d.0+2=2$ | $d.1+2=18$ | $d.2+2=34$ | $d.3+2=50$ | $d.4+2=66$ |
| 3 | | $d.0+3=3$ | $d.1+3=19$ | $d.2+3=35$ | $d.3+3=51$ | $d.4+3=67$ |
| 0 | $N_{cbps} = 192$ -bits, $\frac{1}{2}$ code rate, 16-QAM | $d.0+0=0$ | $d.1+0=16$ | $d.2+0=32$ | $d.3+0=48$ | $d.4+0=64$ |
| 1 | | $d.1+1=17$ | $d.0+1=1$ | $d.3+1=49$ | $d.2+1=33$ | $d.5+1=81$ |
| 2 | | $d.0+2=2$ | $d.1+2=18$ | $d.2+2=34$ | $d.3+2=50$ | $d.4+2=66$ |
| 3 | | $d.1+3=19$ | $d.0+3=3$ | $d.3+3=51$ | $d.2+3=35$ | $d.5+3=83$ |
| 0 | $N_{cbps} = 576$ -bits, $\frac{3}{4}$ code rate, 64-QAM | $d.0+0=0$ | $d.1+0=16$ | $d.2+0=32$ | $d.3+0=48$ | $d.4+0=64$ |
| 1 | | $d.1+1=17$ | $d.2+1=33$ | $d.0+1=1$ | $d.4+1=65$ | $d.5+1=81$ |
| 2 | | $d.2+2=34$ | $d.0+2=2$ | $d.1+2=18$ | $d.5+2=82$ | $d.3+2=50$ |
| 3 | | $d.0+3=3$ | $d.1+3=19$ | $d.2+3=35$ | $d.3+3=51$ | $d.4+3=67$ |

Table 3: Determination of correlation between addresses

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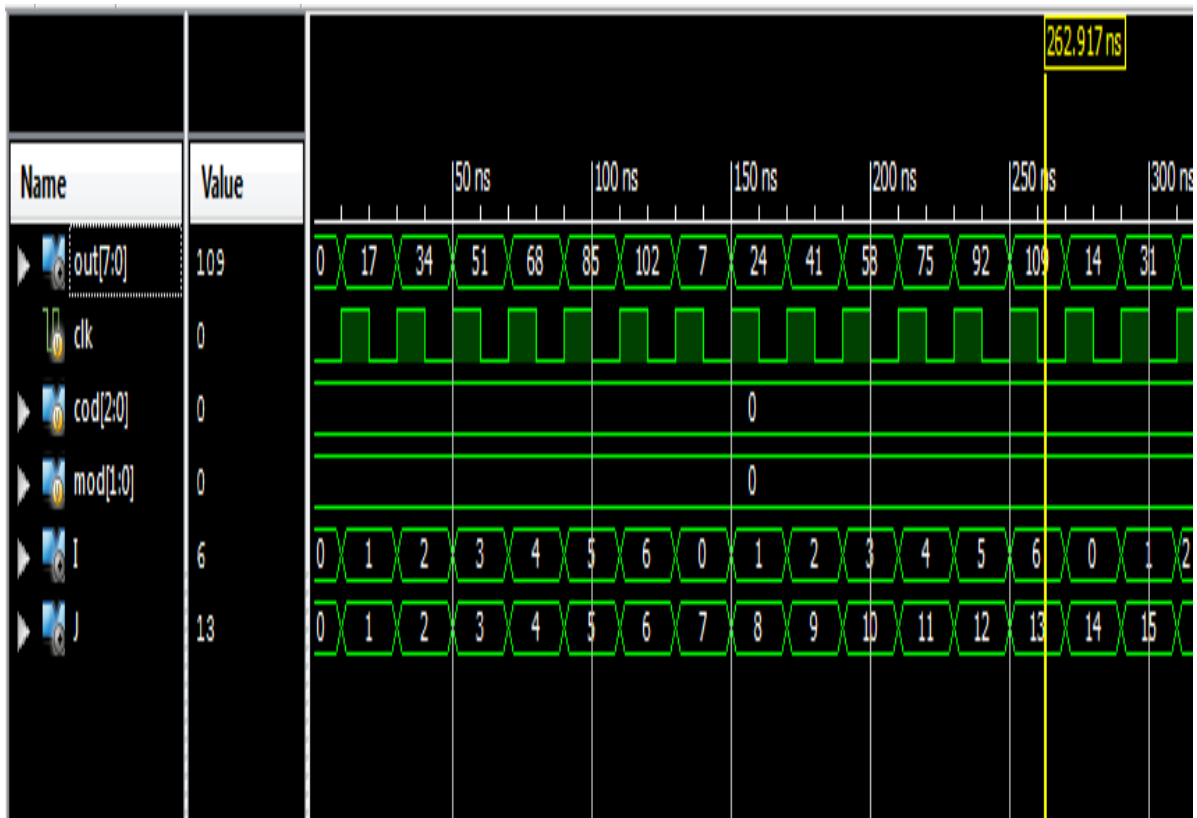
Vol. 4, Issue 4, April 2015

The address generator of the WiMAX deinterleaver with all modulation schemes, transformation of these algorithms into digital circuits are made and are shown in Fig. 10.4. The QPSK hardware shown in Fig. 10.1 has a row counter RWC0 to generate row numbers between 0 and $d - 1$. A column counter CLC0 with multiplexer M0 and comparator C0 generate the variable column numbers to implement permissible N_{cbps} . A multiplier ML0 and an adder A0 perform the desired operations to implement equations. The address generator for 16-QAM follows a similar structure, such as that of QPSK with few additional modules. These modules are designed with an incrementer, a decremter, two modulo-2 blocks, and two multiplexers, as shown in Fig. 10.2. The design procedure used in 16-QAM is extended in 64-QAM to meet this requirement with the use of

additional hardware and is shown in Fig. 10.3. A simple up counter generates the read addresses for the 2-D deinterleaver.

IV. EXPERIMENTAL RESULTS

a) QPSK Simulation Output



International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

V. CONCLUSION

This brief has proposed a novel algorithm along with its mathematical formulation, including proof for address generation circuitry of the WiMAX channel deinterleaver supporting all possible code rates and modulation patterns as per IEEE 802.16e. The proposed algorithm is converted into an optimized digital hardware circuit. The hardware is implemented on the Xilinx FPGA using Verilog. Comparison of our proposed work with a conventional LUT-based method has shown a significant improvement on resource utilization.

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