

Design and Implementation of Dual Mode Logic Based Phase Locked Loop with Sleepy Stack Approach

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ABSTRACT: - This paper deals with Type-I Phase Locked Loop designed for an operating frequency of 1MHz, capture to lock frequency ratio as 0.63. Further the design is extended with low power techniques which aim at reducing the leakage power of the design. Two low power novel techniques called sleepy stack approach and dual mode logic are used. The existing design is modified with these two approaches and their combination for low power designs. The designs are simulated in HSPICE synopsis tool and the waveforms are verified in Avancees tool. The proposed design of PLL using both dual mode logic and sleepy stack approach reduces the power dissipation by nearly 95% when compared to the existing design. Hence the low power PLL is best suited for practical applications as it doesn't deviate much from the specifications.

KEYWORDS: Type-I PLL, Sleepy Stack Approach, Dual Mode Logic, VCO, Phase detector.

I. INTRODUCTION

A PLL [1] is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

$$\phi_{out}(t) = \phi_{in}(t) + const.$$

$$\omega_{out}(t) = \omega_{in}(t)$$

The PLL [2] output can be taken from either V_{cont} , the filtered (almost DC) VCO control voltage, or from the output of the VCO depending on the application. The former provides a baseband output that tracks the phase variation at the input. The VCO output can be used as a local oscillator or to generate a clock signal for a digital system. Either phase or frequency can be used as the input or output variables as shown in figure 1.

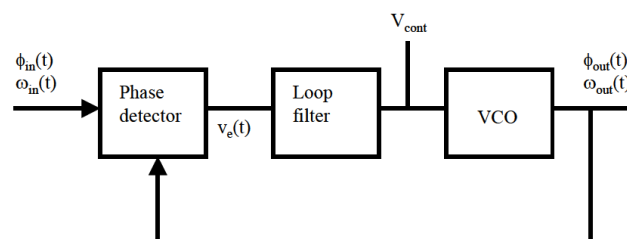


Figure 1: Block Diagram of PLL

The phase and frequency are interrelated by

$$\omega(t) = \frac{d\phi}{dt}$$

$$\phi(t) = \phi(0) + \int_0^t \omega(t') dt'$$

The basic applications of PLL include Clock Generation, Frequency Synthesizer, Clock recovery in a serial data link, etc.

II. EXISTING PLL

The PLL is designed with the following specifications i.e., for Wideband FM with operating frequency $f_0=1\text{MHz}$, $k_f=250\text{kHz/V}$, $k_d=0.1\text{ V/rad}$, $R=10\text{K}\Omega$, $C=1000\text{pF}$, the lock range frequency is $f_{\text{lock}} = k_f \cdot k_d \cdot \pi / 2 = 39\text{kHz}$, and the corresponding voltage lock value is $v_{\text{lock}} = k_d \cdot \pi / 2 = 0.157$. The capture to lock range is $f_{\text{capture}} / f_{\text{lock}} \sim 1 / \sqrt{2 \cdot \pi \cdot R \cdot C \cdot f_{\text{lock}}} = 0.63$, the corresponding capture potential is $v_{\text{capture}} \sim 0.100$.

III. LOW POWER TECHNIQUES

In this paper, two low power techniques are used i.e., Sleepy Stack approach and Dual Mode Logic. Both of these techniques aim at reducing the power dissipated. Also the sleepy stack approach is designed to reduce the leakage power.

A. Sleepy Stack approach

The sleepy stack approach [3] combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors [4], reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals as shown in figure 2.

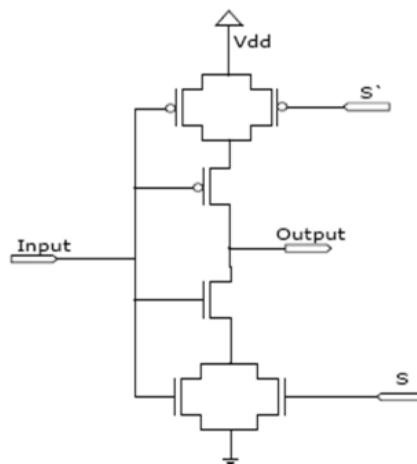


Figure 2: Sleepy Stack approach

B. Dual Mode Logic

The basic DML (Dual Mode Logic) gate is having an normal static logic gate, which can be an conventional CMOS logic gate and at the output side we are connecting an normal transistor. And whose gate is connected to a global clock signal is applied to it as switching circuit. The whole operation is based upon the external connected transistor and its clock signal speed. The DML [5] can be arranged as two ways depending upon the type of transistor using at the output side either PMOS or NMOS transistor as following way shown in the figure 3.

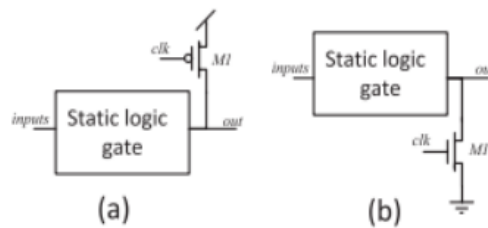


Figure 3: DML Topology (a) Type A (b) Type B

The DML [6] provides the designer with a very high flexibility to overcome the disadvantages of the following two methods – 1) static mode and, 2) dynamic mode. Since, in static mode of operation the power dissipation is low and speed is also very low compared to the dynamic mode. Similarly in dynamic mode the speed is very high and power dissipation is also high compared with static mode.

IV. PERFORMANCE & DIFFERENCE BETWEEN EXISTING AND PROPOSED PLL DESIGNS

The PLL is designed in four ways i.e., with (i) existing technique, (ii) Sleepy Stack approach (iii) Dual Mode Logic and (iv) both sleepy stack and dual mode logic.

In the existing design, the power is obtained in terms of mW. In sleepy stack approach, as the technique is applied to only PLL, the design doesn't vary much with existing design. In dual mode approach using type B, the design slightly decreases the power dissipation. But with the combination of both dual mode logic and sleepy stack approach, the power is reduced drastically as shown in table 1.

Table 1: Comparison in terms of Power dissipation

PLL Design	Power Dissipation (W)
Existing PLL	2.4749E-03
Sleepy Stack based PLL	2.4749E-03
DML based PLL	2.4328E-03
DML based PLL with Sleepy Stack	1.1396E-04

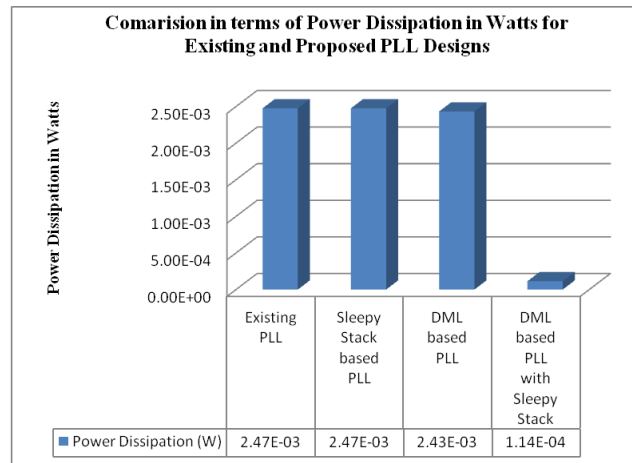


Figure 4: Graphical comparison of Power dissipation of existing and proposed PLL designs.

The graphical representation is shown in figure 4. From figure 4 and table 1, it is shown that the design of PLL with DML logic reduces by 2% but in combination with sleepy stack approach, it reduces by 95% when compared with existing PLL design.

IV. RESULTS

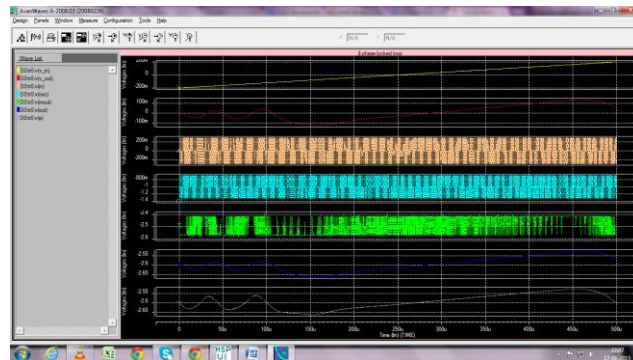


Figure 5: Simulation Results of PLL

The simulation results are shown in figure 5 which are obtained from Avanwaves wave viewer of HSPICE Synopsys tool. The designs are coded in SPICE (Simulation Program with Integrated Circuit Emphasis) language. In the figure 5, V_{in} represents the actual input signal, $v(out)$ represents the output signal of PLL which clearly shows the lock range and capture range. $v(in)$ represents the input to PLL, $v(osc)$ represents the voltage controlled oscillator output signal, $v(mout)$ represents the phase detector output signal, $v(out)$ and $v(e)$ represent the corresponding output and intermediate signals. The results clearly show the capture range of nearly 24.5KHz and the lock range frequency to be 39KHz. The waveforms of existing and proposed designs are similar; hence only one wave form is shown for results. Thus the results in the implementation indicate that the designs satisfy the specifications and are well suited for low power applications.

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The PLL is designed for an operating frequency of 1MHz, capture to lock frequency ratio as 0.63 using low power techniques like sleepy stack approach and dual mode logic. The existing design is modified with these two approaches and their combination for low power designs with reduction in overall power dissipation. The low power designs aim at reducing the leakage power and increase the speed. The designs are simulated in HSPICE synopsis tool and the waveforms are verified in Avanwaves tool. The proposed design of PLL using both dual mode logic and sleepy stack approach reduces the power dissipation by nearly 95% when compared to the existing design, which makes it suited for practical applications like clock generation, frequency synthesizer, etc.

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