

2N2N2P-An Efficient Adiabatic Logic for VLSI Design

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ABSTRACT: Now-a-days, the achievement of high speed, small circuitry area and low power consumption is being considered by designers to fabricate modern digital circuits. For these full adders are one of the most important components for its wide use in subtraction, multiplication, filtering, DSP processors and Microprocessors. So, it is of a great interest of the designers to design Carry Look Ahead (CLA) adder because of its high speed operation. In this paper we have considered the power consumption and delay of a 4 bit CLA adder implemented in static CMOS and adiabatic 2n2n2p logic.

KEYWORDS: Adiabatic Logic, Low power, CMOS, ECRL.

I. INTRODUCTION

We have chosen the CLA adder because of its speed of addition. To speed up the carry computation CLA adder can be used predominantly. Figure 1 shows the schematic for the sum output of a 4-bit CLA adder. Actually in the CLA adder the carry computation is divided into two steps starting with the computation of two intermediate values. For two specified inputs A_i and B_i of the CLA adder, the propagate and generate may be written as:

$$P_i = A_i(Xor)B_i \quad (1)$$

$$G_i = A_i \cdot B_i \quad (2)$$

Both propagate and generate signals depend only on the input bits. The sum and carry output can be written as follows

$$C_{i+1} = G_i + P_i C_i \quad (3)$$

$$S_i = C_i (Xor) A_i (Xor) B_i \quad (4)$$

So, C_{i+1} is a function of inputs and C_i .

Thus for the generation of the carry signal either of the bits A_i and B_i should be 1 or both of them should be 1.

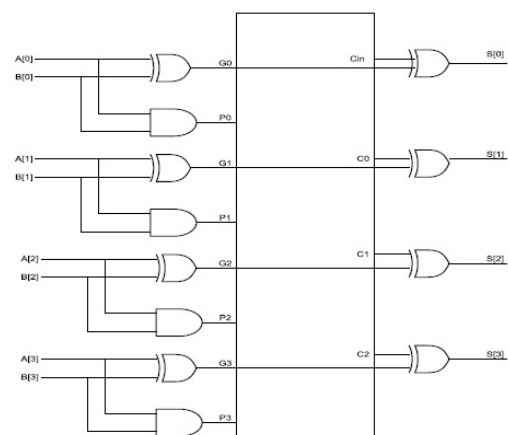


Fig.1 Schematic diagram of output sum

II. ADDER IMPLEMENTATION

The adder is implemented by two methods.

A. STATIC CMOS LOGIC

Fig. 2 shows a simple RC tree, where the transition of a circuit node from low to high can be considered as charging the RC tree through a switch from a constant voltage source. When the switch is closed, there is a flow of current through the circuit and the capacitor charges exponentially to V_{dd} .

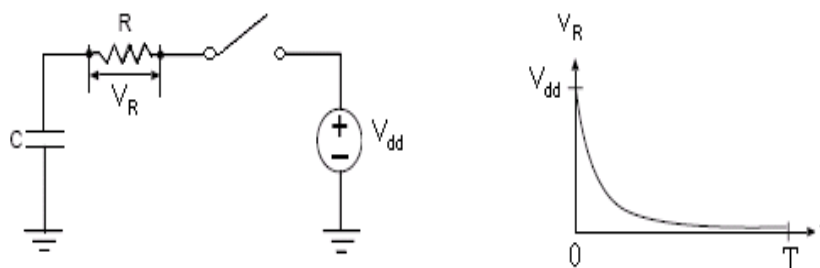


Fig.2. Charging an RC tree with a switch

The energy taken from the power supply is CV^2_{dd} . But half of this ($\frac{1}{2} CV^2_{dd}$), is stored in the capacitor (C) and the other half is dissipated in the resistor (R). This dissipation does not depend on the value of R during the discharge of the node the energy in the capacitor is dissipated in the discharging resistor. For the total cycle of charging and discharging of the node, energy of CV^2_{dd} is drawn from the source and is dissipated to the surroundings. To reduce power dissipation, transistor sizes may be decreased or the supply voltage may be reduced or the switching activities can be minimized. Since shrinking of transistor size does not provide benefits in power dissipation, the reduction of supply voltage is thus the best choice to reduce power consumption significantly.

B. ADIABATIC 2N2N2P LOGIC

Adiabatic switching [1] can be achieved by ensuring small potential across the switching devices as shown in Figure 2. Figure 3 shows the adiabatic charging in an RC tree.

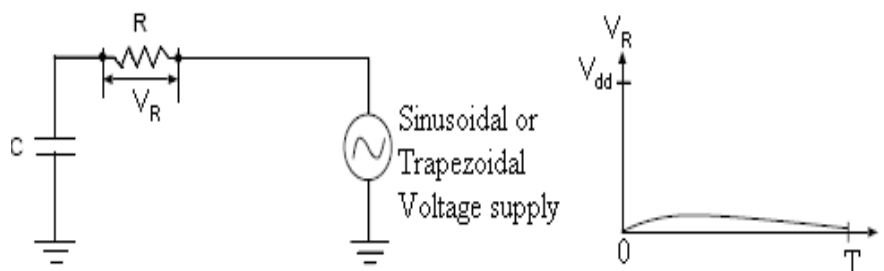


Fig.3. Adiabatic Charging in an RC tree.

Adiabatic charging may be achieved by charging the capacitor from a time varying source that starts at 0V. The Adiabatic charging may be achieved by charging the capacitor and the energy dissipated is given by,

$$E_{Res} = \frac{RC}{T} C V_{DD}^2 \quad (5)$$

An increase in T results a decrease in power dissipation. Now if $T \gg RC$, energy dissipation in the resistor during charging tends to zero and so the total energy taken from the supply is $CV^2_{dd} / 2$, which is the minimum, required to charge the capacitor and hold the logic state. This stored energy may be returned to the supply during the discharging cycle. There are two fundamental rules which the adiabatic logic circuits should follow [6]:

- If there is a significant voltage drop across the source and drain of the transistor it will not turned on.
- If there is a significant current flowing through the channel of the transistor it is never turned off.

Violation of these, results in significant power dissipation. Following cautious design, every transistor can operate in a nearly adiabatic fashion. However, it is tough to have all the circuit elements working in adiabatic fashion. This is because a gate in a later stage is controlled by gates in earlier stages. Thus a gate should and operate in such a way that the subsequent gates can switch adiabatically.

2N2N2P family belongs to the quasi-adiabatic logic family, derived from ECRL in order to reduce the coupling effect. Figure 5 shows the schematic of 2N-2N2P family. Its main advantage [2] over ECRL is the cross coupling of nmosfets switches which leads to non floating outputs for major part of the recovery phase. A variant of the ECRL logic family is 2N2N2P family with the only difference that it has a pair of cross-coupled NMOS transistors in addition to the cross coupled PMOS transistors common to both the families. 2N2N2P family is very similar to a standard SRAM cell as it has cross coupled full inverters.

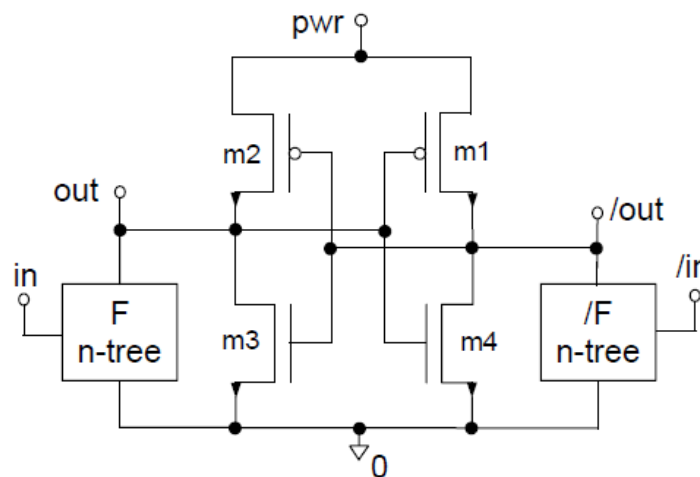


Fig. 4 General schematic for 2N-2N2P logic family

III. RESULT ANALYSIS

In this paper we have calculated the power dissipation for static CMOS and 2N2N2P adiabatic 4 bit CLA adder using T-SPICE simulation tool. The observed power and delay are shown in Figure 5 and Figure 6 respectively. From the calculation we have done, it has been found that CLA using 2N2N2P logic have low power dissipation. So, it can be used to design low power circuits. The transistor count and delay is larger than static CMOS logic. Table I indicates the no of transistor required in both logic and Table II gives a comparative study for the power and delay at different voltages.

TABLE I
TRANSISTORS REQUIRED

Logic style	AND Gate	XOR Gate	4 bit CLA
Static CMOS	6	12	144
2N2N2P	12	16	224

TABLE II
VARIATION OF POWER & DELAY FOR DIFFERENT SUPPLY VOLTAGES

Logic style	V _{DD} =1V		V _{DD} =1.2 V		V _{DD} =1.4 V		V _{DD} =1.6 V	
	Power	Delay	Power	Delay	Power	Delay	Power	Delay
Static CMOS	1.89E-06	3.38E-10	2.49E-06	2.59E-10	3.62E-06	2.01E-10	4.84E-06	1.76E-10
2N2N2P	6.65E-07	2.77E-10	7.24E-07	2.39E-10	8.10E-07	1.90E-10	8.97E-07	1.65E-10

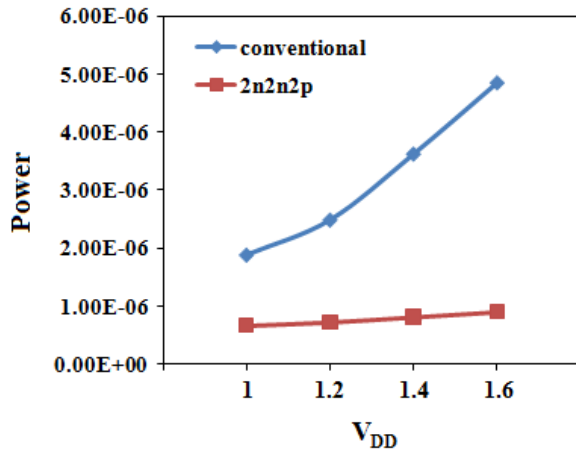


Fig. 5 Observed power of 4 bit CLA

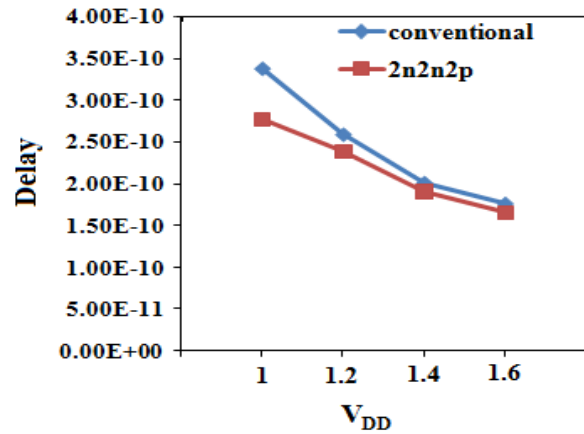


Fig. 6 Observed delay of 4 bit CLA

IV. CONCLUSION

Adiabatic logic is an efficient technique for designing low power circuits compared to conventional CMOS logic. Simulation indicates it is a power saving logic. From the analysis we can conclude CLA using ECRL logic is a good option for low power circuit design.

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