

# Power and Delay Analysis of a 4 to 1 Multiplexer Implemented in different Logic Style

Debika Chaudhuri<sup>1</sup>, Atanu Nag<sup>2\*</sup>, Sukanta Bose<sup>3</sup>, Suchismita Mitra<sup>1</sup>, Hemanta Ghosh<sup>1</sup>

Department of Electronics & Communication Engineering, Modern Institute of Engineering & Technology, Hooghly, West Bengal, India<sup>1</sup>

Department of Physics, Modern Institute of Engineering & Technology, Hooghly, West Bengal, India<sup>2</sup>

CEGESS, BESU, Shibpur, West Bengal, India<sup>3</sup>

**ABSTRACT:** Power dissipation is the most commonly concerned issue in the low power VLSI design circuits. The aim of the paper is to reduce power or energy dissipation. We have used the technique of adiabatic switching based on different logic to achieve VLSI circuit design with low power. It is proposed by implementing pmos and nmos transistors as pull up and pull down network. In this paper the power dissipation of various adiabatic 4:1 multiplexers (DCVSL, MDCVSL) is calculated and then simulated using T-SPICE tool. We have also implemented the multiplexing technique using Transmission Gate Logic (TGL). From the calculated result it is obvious that the multiplexer using adiabatic logic and TGL can effectively reduce the power dissipation as compared to the conventional CMOS design. From the results of calculation it is observed that among the discussed logic used for multiplexer implementation TGL exhibits the minimum power dissipation.

**KEYWORDS:** VLSI, Adiabatic logic, TGL, T-SPICE

## I. INTRODUCTION

Due to the restricted power supplied by the batteries the circuitry involved in the modern portable electronic devices must be designed to consume less power avoiding the requirement of expensive and noise cooling supply and power consumption circuits. Now for the purpose of digital design multiplexer is an essential component. Thus diminution of the power dissipation of the multiplexer is one of the major concerns of low power design [1]. Generally, the techniques of power saving needs the scaling of the power supply to undergo significant increase in sub-threshold leakage current. For this some other technique is required which is independent of voltage scaling. It has been established that there is essential connection between computation and power dissipation. There are various methods broadly used for reducing the power dissipation in circuits by reducing supply voltage, load capacitances, switching activities although most of the energy down from dc power supply is absolutely dissipated in the circuit [2].

Power dissipation can also be reduced by implementing the adiabatic logic, transmission gate logic etc. The power dissipation in these circuits can be reduced by recycling the energy by utilizing the ac power stored into the load capacitances rather than to dissipate it in the form of heat [3] and it can be implemented by using pmos and nmos transistors as pull up and pull down network. The inverter used with the adiabatic logic concept has less power dissipation compared to conventional one. Both the pmos and nmos transistors can be assumed as an ideal switch in series with a resistor for the illustration of the effective channel resistance of the switch. In addition to the interrelated resistance in the circuit as shown in Figure 1 where with the load capacitance, pull up and pull down networks are connected. Figure 2 illustrates the equivalent model of the charging process in adiabatic circuits [4, 5].

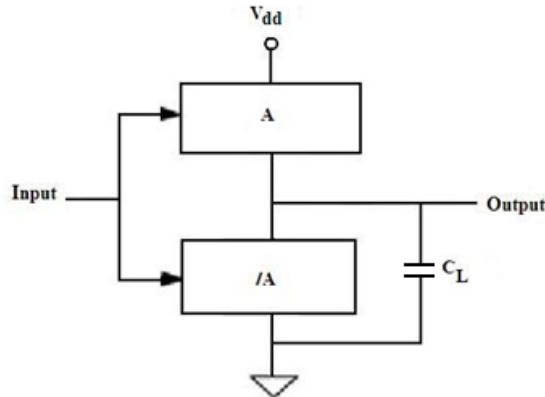


Fig.1 Conventional CMOS logic circuit with pull-up (A) and pull down (/A) network

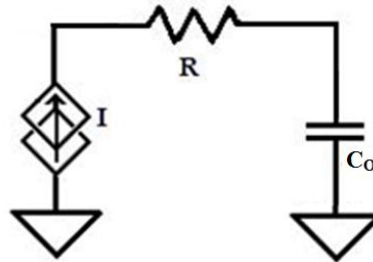


Fig. 2 Equivalent model during charging process in adiabatic circuits

Adiabatic circuits do not utilize standard power supplies as in CMOS circuits it uses pulsed power supply [6]. Figure 3 represents a CMOS adiabatic inverter. The adiabatic switching technique is commonly used to minimize the energy loss during the charging and discharging of the load capacitor [7, 8]. In adiabatic circuits all of the capacitors are charged or discharged at a constant current for the minimization of the power dissipation. In this paper we have calculated the power dissipation for DCVSL and MDCVSL adiabatic 4:1 MUX and TGL 4:1 MUX using T-SPICE simulation tool. From our analysis it is obvious that the TGL multiplexer exhibits minimum number of PMOS and NMOS, minimum delay and minimum power dissipation. So, it can be used to design low power circuits.

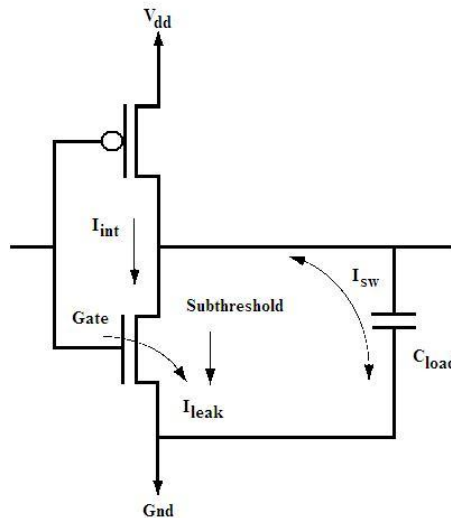


Fig. 3 Adiabatic CMOS inverter

**II. MULTIPLEXER DESIGNS**

A logic style may affect the size, speed, power consumption and wiring density of a circuit. All these vary considerably from one logic to another and so we have to formulate the proper choice of logic for having an efficient logic with low power circuit performance [9]. In modern digital circuit design multiplexer is an essential component and the need is to implement a logic convenient to produce low power consumption. Figure 4 shows the conventional 4:1 mux whereas figure 5 shows the 4:1 mux implemented by using Differential Cascade Voltage Switch Logic (DCVSL) logic. The advantage of this logic is that the logic implements all functions using nmos only and the pmos serve only as the pull up devices. DCVSL circuit can be divided into two basic components a differential latching circuit and a cascaded complementary logic array [10]. The latch in these logic circuits is being realized with two cross coupled pmos transistors and the cascade complementary logic array is being realized with a nmos logic tree [11].

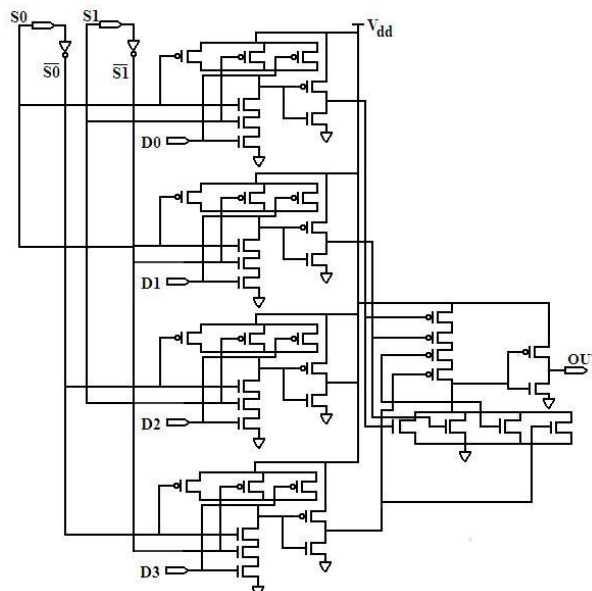


Fig. 4 Conventional 4:1 MUX

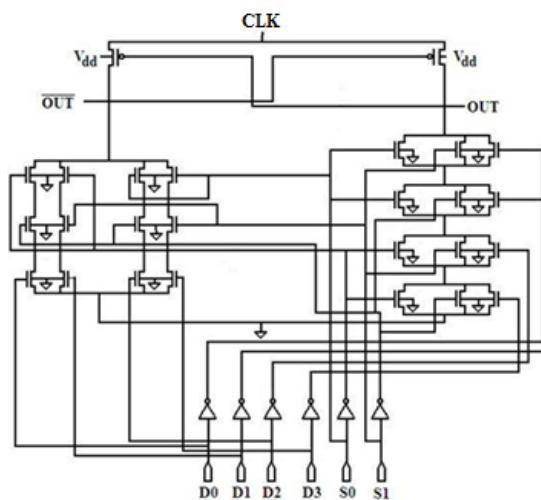


Fig. 5 Schematic design of DCVSL 4:1 Multiplexer [12].

Figure 6 shows the 4:1 MUX implemented by using MDCVSL logic. The MDCVSL stands for modified differential cascade voltage switch logic. Delay has been improved by adding two NMOS in the previous design [11].

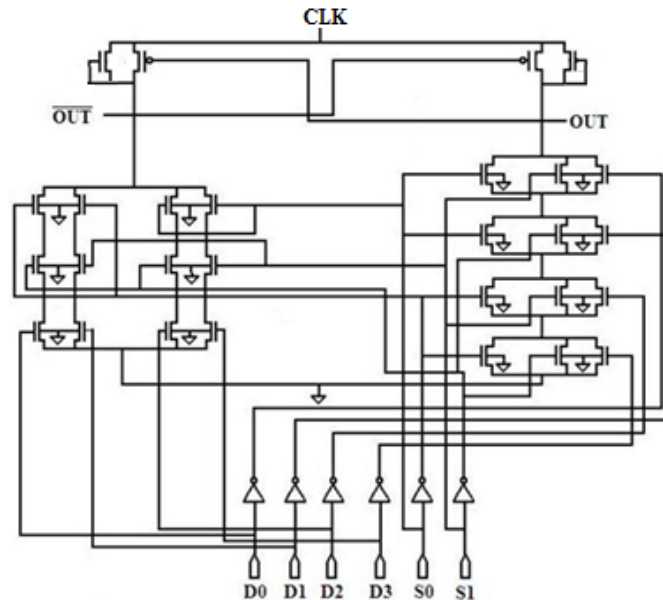


Fig. 6 Schematic design of MDCVSL 4:1 Multiplexer [12].

Figure 7 shows the 4:1 mux implemented by using TGL. The advantages of this logic are minimization of the circuit complexity less area requirement and achievement of strong output level without degradation

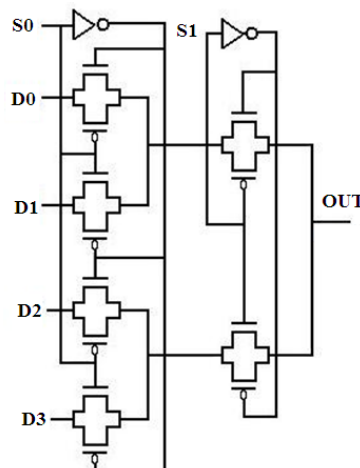


Fig. 7 Schematic design of TGL 4:1 Multiplexer

### III. RESULTS & COMPARISON

Different 4:1 multiplexers designs such as dcvsl [10] mdcvsl [11] tgl are simulated and compared with conventional multiplexer in terms of power consumption Delay and power delay product pdp simulated results are shown in table i It has been observed that among all chosen multiplexers tgl uses minimum number of pmos and nmos and for this logic the average power and delay are observed to be Small as compared to the conventional and the DCVSL or MDCVSL 4:1 mux. The graphical illustration of the delay produced by the different implemented mux is shown in figure 8 Corresponding average power variation and pdp variation are shown in Figure 9 and Figure 10 respectively.

Table I Comparison of different 4:1 Multiplexer

Parameters	Conventional	DCVSL	MDCVSL	TGL
No of MOSFETs	23 PMOS 23NMOS	8 PMOS 30NMOS	8PMOS 32NMOS	8 PMOS 8NMOS
Average power(in $\mu$ W)	3.44	0.29	0.295	0.0644
Delay(in nS)	0.588	4.23	4.14	0.0755
PDP( $10^{-17}$ J)	202	1.23	1.22	0.486

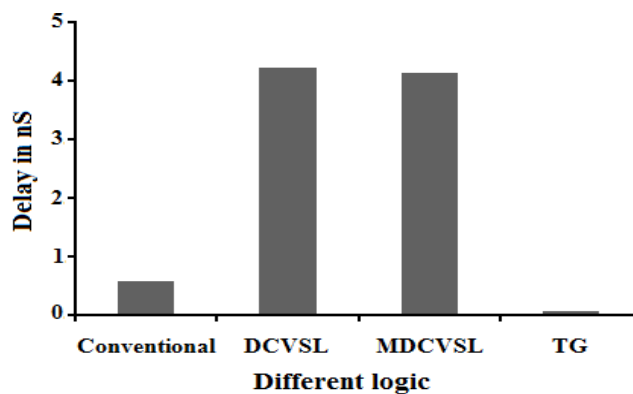


Fig. 8 Observed delay in the implemented 4:1 MUX using different logic

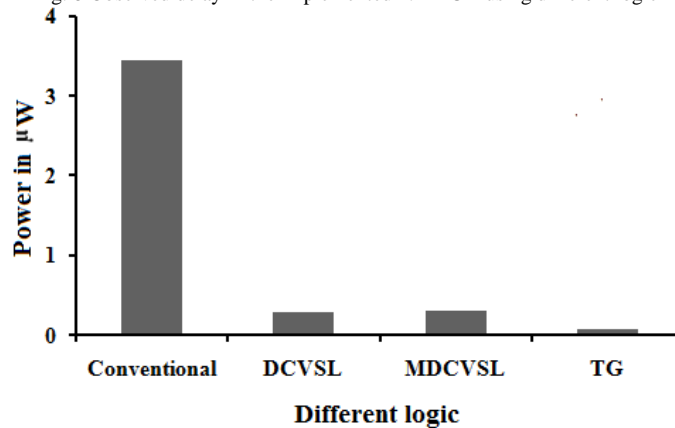


Fig. 9 Observed average power in the implemented 4:1 MUX using different logic

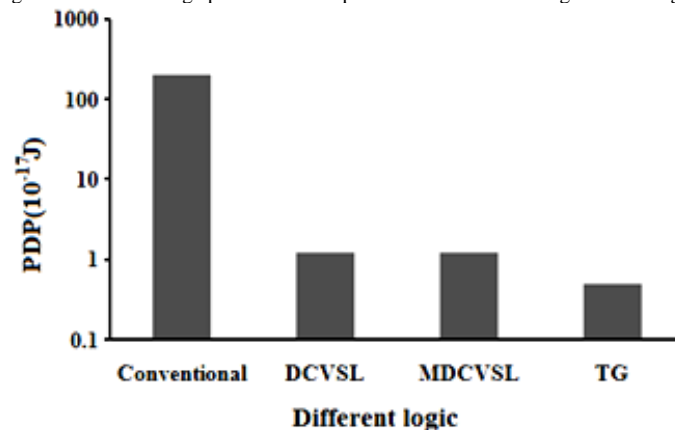


Fig. 10 Observed PDP in the implemented 4:1 MUX using different logic

#### IV. CONCLUSION

From the analysis we can conclude that for designing low power circuits, adiabatic logic is an efficient technique as compared to conventional CMOS logic. TGL 4:1 mux is the most efficient among the implemented ones as it requires minimum number of MOS and thereby possessing low power consumption and minimum delay.

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