

# RF & Logical Performance Inas Based DMG HEMT High Speed & High Power Application

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**ABSTRACT:** In this paper we have double material gate (DMG) HEMT. It has variation in barrier layer thickness affects nitride-based HEMTs more strongly than antimonide-based DMG HEMTs. Higher Electron Mobility and drift velocity can be realized by reducing of  $L_g$  and increasing the indium content in the InAs channel. Due to the high electron mobility, velocity and large conduction band offset InAs. InAs-channel HEMT is promising for high speed logic applications. Greater potential of 40nm InAs HEMTs. InAs HEMTs has ultra low-noise, sub-millimeter wave and terahertz applications.

**KEYWORDS:** InAs, HEMT, Dual Material Gate (DMG), RF, high speed and high power application.

## I. INTRODUCTION

Antimonide-based compound semiconductors are opening a new field for semiconductor industry as they can be used both as third generation infrared photo-detectors and ultra-high speed, ultra-low power consuming integrated circuit fabrication [1]. DMG structure is more effective to reducing SCEs for antimonide-based HEMTs than nitride-based HEMT, while nitride-based DMG HEMT give more efficient carrier transport than antimonide-based counterpart [2]. In the field device technology, HEMTs are gain interest due to their potential to replace MOSFETs. In HEMTs are faster, low power consuming and easy to fabricate compare to MOSFET [3].

Scaling of device is a fundamental in semiconductor industry to make smaller, fast and less power consume chips HEMTs follow the trend [4]. In DMG FET, two gates made different materials of different work functions is joining laterally to create a single gate. The work function one of gate M1 is chosen to be greater than the other M2. Gate M1 works as controlling gate and gate M2 works as screening gate of drain voltage. It enhances electric field and inserts a step function in channel potential at interface of double gates. The enhanced average electric field improves the carrier transport efficient and the step functions reduce the short channel effects. But the scaling going in to deep sub-microns level, the need for an analytical modelling of subthreshold behavior of DMG HEMT emerges. S.P.Kumar et al. [5] first proposed an analytical model for the subthreshold behavior of nitride-based DMG FET. In our previous paper [2] the model of [5] was modified and an analytical model for antimonide-based HEMTs was developed.

In [2], the  $Al_{0.7}In_{0.3}Sb/InAs$  combination used of barrier and channel. Among the antimony-based material AISb and GaSb are approximately lattice match to InAs and these semiconductors are jointly known as 6.1  $\text{\AA}$  family. In this paper we also study the  $Al_{0.7}Ga_{0.3}Sb/GaSb$  and  $Al_{0.7}Ga_{0.3}Sb/In_{0.15}Ga_{0.85}Sb$  barrier and channel combinations and compare their results.

## II. DEVICE FABRICATION

Fig.1 is the schematic of symmetric Double-Metal-Gate (DMG)  $In_{0.3}Al_{0.7}Sb/InAs$  HEMT. The work function of metal M1 and M2 respectively. As it will be n-channel HEMT, so M1 must be greater than M2 [5]. We have chosen the value

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of gate work function for M1 and M2 5.2eV and 4.2eV respectively the barrier layer completely depleted under normal condition and to confined electron in the heterointerface  $\text{In}_{0.3}\text{Al}_{0.7}\text{Sb}/\text{InAs}$ . Table 1 show the parameter used in the HEMT model.

Table.1 LIST OF PARAMETERS

Parameters	Name of the parameter	Value
Nd	Doping in the barrier layer	$10^{19}$ cm
$N_d^+$	Doping in source and drain region	$10^{17}$ cm
T	Operating temperature	300K
L	Total Effective channel length	120nm
$d_d$	Thickness of doped barrier layer	25nm
$d_i$	Thickness of spacer layer	5nm
$\epsilon_s$	Dielectric constant of	12.6

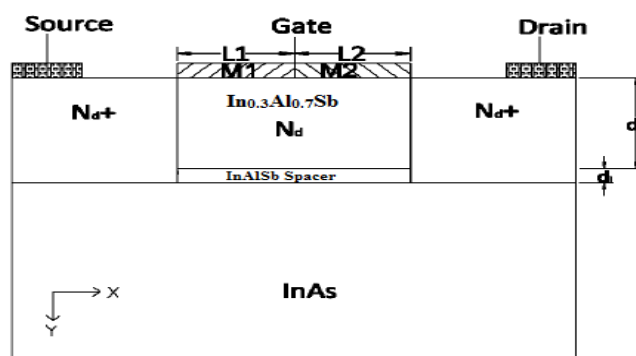


Figure 1 Schematic of symmetric Double-Metal-gate InAlSb/InAs HEMT

### III. RESULTS AND DISCUSSIONS

We used TCAD device simulator of channel potential and electric field distribution along the channel to verify the model of [2] Fig.2 show electric field Variations vs. normalized channel length and the channel potential vs. normalized channel length for DMG  $\text{In}_{0.3}\text{Al}_{0.7}\text{Sb}/\text{InAs}$  HEMT.

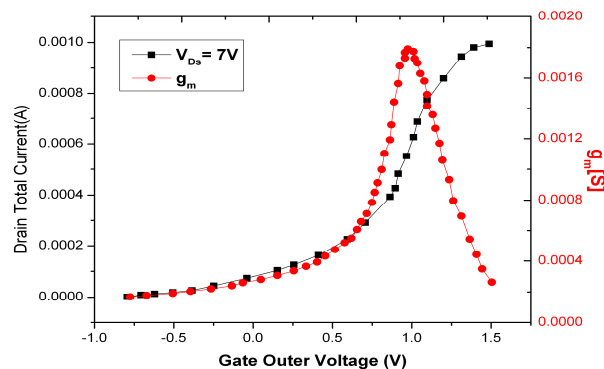


Figure 2  $I_{DS}-V_{GS}$  characteristics of the device with  $L_G=120\text{nm}$

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We have shown the effects of varying gate length metal 1 gate keep go to the total length  $L$  constant. As we can see in the figures 1, the minimum potential barrier and thus enhances the drive current ( $I_{on}$ ). The total current drain of  $g_m = 0.0015950$  and  $V_T = 0.6160125$ . Its show the increases in control of gate over than channel potential.

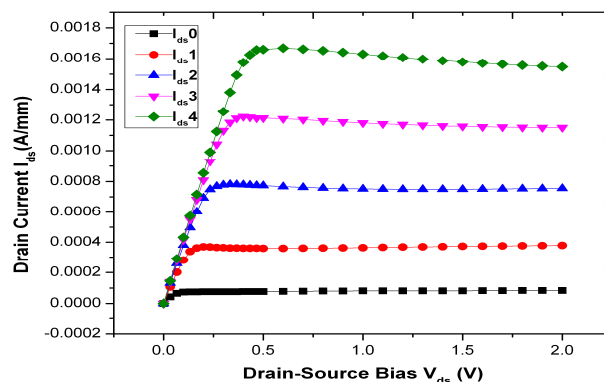


Figure 3  $I_{DS}$ - $V_{DS}$  characteristics of the device with  $L_G = 120$  nm

Device current-voltage ( $I$ - $V$ ) measurements were carried out on devices with a gate-source distance  $L_{gs}$  of  $0.04\mu\text{m}$ , a gate length  $L_g$  of  $0.12\mu\text{m}$ , and a gate-drain distance  $L_{gd}$  of  $0.04\mu\text{m}$ . For these simulations, the gate1 voltage is kept at  $5.3\text{V}$  and various gate2 voltage  $4.5\sim 5\text{V}$ .

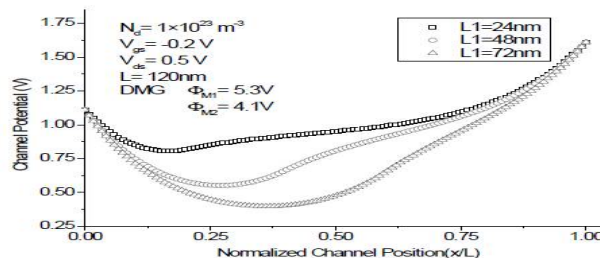


Figure 4 Variation of channel potential with normalized channel position for different combination of gate length  $L_1$  and  $L_2$ , keeping the  $L$  constant for gate  $\text{In}_{0.3}\text{Al}_{0.7}\text{Sb}/\text{InAs}$  HEMT

In figure 4 we have shown the effects of varying the gate length of first metal gate ( $L_1$ ) keeping the total gate length  $L_{\text{constant}}$ . As we can see in the figure-4, the minimum potential increases as the  $L_1$  decreases. It reduces the potential barrier and thus enhances the drive current ( $I_{on}$ ). Moreover it increases the control of gate over the channel potential. The change in with change in  $L_1$  for various formations of HEMTs.

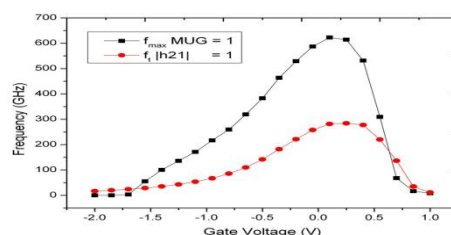


Figure 5  $L$  constant for gate  $L_g = 120$  nm  $\text{In}_{0.3}\text{Al}_{0.7}\text{Sb}/\text{InAs}$  HEMT having a simultaneous record  $f_T$  of  $280$  GHz and an  $f_{\text{max}}$  of  $621$  GHz at  $V_{DS} = 0.5$  V.

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To avoid this problem, we have focused on  $V_{DS} \leq 0.5$  V because in this region  $L_g$  is relatively well behaved and our small signal model predicts the gain characteristics. Using this model, Figure 1 we extrapolated a value of  $f_{max}$  of 621 GHz at  $V_{DS} = 0.5$  V. The average  $f_{max}$  obtained the various systems at this bias point is 661GHz  $\pm$ 4 GHz. We are confident in reporting an  $f_{max}$  of 621 GHz at the bias point. Our small-signal model extraction reveals that this excellent value of  $f_{max}$  arises from a combination of  $gm/go = 15.4$  and  $C_{gs}/C_{gd} = 6.3$ . The relatively low values of  $C_{gd}$  arise partly from the widening  $L_{side}$ . To our knowledge of the authors, this is the first simultaneous demonstration of both  $f_T$  and  $f_{max}$  in excess of 621GHz in any transistor technology on this material system.

## IV. CONCLUSIONS

To solve the problem of short channel effect and carrier transport inefficiency of the HEMTs, a new structure called Double Material Gate (DMG) was proposed. In the work gate threshold voltage not good efficiently so improving threshold MOSHEMT were alternative solutions for solve this problem. The result of the proposed model matches very well with results obtained from TCAD device simulator.

Moreover, our model has reducing SCEs and increasing transport efficiencies. So our model opens up solutions for short channel effects removing in the interesting field of semiconductor technology. Further we can improve triple material gate (TMG) and also Double Gate on this model by that DIBL still reduce more and frequency increase on HEMT. Than more we can develop HEMT structure into MOSHEMT.

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