

# Development of ARM-based Hardware Platform for Implementation of Low Power Management and Fault Tolerance

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**ABSTRACT:** Power consumption is the most critical issue in embedded devices. Not only power consumption but there are other embedded design challenges such as low-cost, fast processing speed, low-memory requirements and low energy. The basic requirements of embedded system are high fault tolerance and low power consumption. In this paper, we are implementing a hardware platform for experimenting with the different power management techniques and fault tolerance techniques. At the system level, most of the power management techniques concentrate on the core processor as, it consumes more power. But we can get the optimized solution for power management if we apply these techniques to the whole microcontroller. Total power consumption would be reduced by using these techniques on both core processor and peripherals. In this hardware platform, two ARM microcontrollers and a co-processor AT89C51 are used for its implementation. Dynamic power management and peripheral power down for power management and standby sparing techniques are used for experimenting with this hardware platform.

**KEYWORDS:** Dynamic power management (DPM), peripheral power down, fault tolerance.

## I. INTRODUCTION

Low power and high performance are most important constraints of embedded system designs. Furthermore, low power involves lower cost of operation of device and smaller battery size to make system more mobile. . As, for many of these systems , there is no possibility of frequently charging or replacing their batteries , they are highly energy constrained[1],[2],[4].Most of the embedded products are battery operated, including portable data terminals handheld gaming consoles, media players ,portable medical diagnostic equipment , smart watches , communications hot spots , battery-backed home and building automation navigation system ,test and measurement devices, mobile robots, smart displays and many more[1]. Furthermore, with increasing facilities of embedded system its complexity is also increasing day-by-day.

Today's embedded systems deal with the time-to-market pressure, try to deliver correct-the-first-time products with multiple system requirements, the use of commercial off-the- shelf (COTS) devices [1][4][6][8] is very beneficial in designing embedded systems. There are also reconfigurable hardware solutions to stimulate the design process and offer a various programmable logic devices (PLD) -based evaluation kit [1][9] (eg Xilinx). As these platforms allows functionality test of the SOC or ASIC devices, but doesn't focus on embedded system. Reconfigurable hardware solution such as Xilinx, these platforms do not provide facilities to experiment with energy management techniques. Embedded systems consist of the number of microcontrollers. Microcontroller consists of inbuilt processor core integrated with memories and other peripherals in a single chip [1],[5],[8]. Some laboratory experiments have been performed on microcontroller based platforms in reference [6]. In reference [15] a prototyping platforms for ARM-based embedded system has implemented. However, these platforms do not provide experimentation with power management techniques. Therefore, developing a hardware platform for embedded system which allows

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experimentation with power management and fault tolerance is very important. In this paper, we are proposing a hardware platform for experimenting with low power and fault tolerance based on two ARM microcontrollers. In dealing with low-power techniques, selecting a particular embedded system criteria is important. Implementation of these techniques should have the goals as system are hard-real time or soft-real time and high reliability. This is a general concept, we need to customize this concept with particular application. DVFS and DPM are the most popular technique are used for power management [1][3]. But there are disadvantages of both of these techniques if not applied it on correct application. Considering an application is hard real time application, if we apply DPM technique on this system, then system will take time to come from idle mode to active mode. In such case, system can miss its deadline which is not beneficial in hard real time system, therefore DVFS technique is suitable for this system as it adjusts its voltage and frequency as per the given workload of the system. Unlike with the soft-real time system, DPM is more suitable. Dynamic voltage scaling(DVS) have negative impact on the system reliability [3]. Also for dynamic frequency techniques, at low-frequency processor gets low, as its execution time will increase which leads to more heat dissipation and slower the execution. We if are dealing with low-power hard-real time system we have to apply both methods simultaneously. Most of the techniques are only applied to the processor core, here we are applying these methods on both processor core and peripherals.

The main contribution of this paper are

1. We are implementing a hardware platform for low power management and fault tolerance with the development of application. Here we choose to develop soft real time and high reliability application. In this system, we are developing “**Smart Library Assistant Device**”. This device will simply show the book’s section like a human library assistant does.
2. As we select to develop a soft-real time system, we can implement the DPM for power management for processors and peripheral power down for peripherals.
3. For fault tolerance, we have selected a cold standby sparing techniques as it suitable for low-power consumption.

## II. HARDWARE PLATFORM DESIGN

ARM7TDMI is the most popularly used COTS processor in embedded system as, it is a low-cost, high performance and versatile processor[1],[2],[4],[6]. Many embedded system designers (e.g., [9], [13], and [14]) combine the ARM7TDMI (ARM7) processor with internal memory devices and a wide range of peripherals on a single chip to obtain a microcontroller [1]. The computational power of ARM7 is quite enough for the majority of embedded applications. For example, ARM7 can easily executable in all benchmarks in MiBench benchmark suite [1],[2],. ARM7 can also execute complex operating systems (e.g., Real-Time Executive for Multiprocessor Systems (RTEMS) [1], [2,] and Keil RTX [1]). For highly computation applications, the performance of ARM7 might not be adequate [1]. In this case, it should be noted that our proposed platform is not only dependent on ARM7 [1].

### A. Architectural Overview

This ARM7-based platform is used in most of the COTS processor, here we chose one of them ie. LPC214x controllers. As shown in the fig.1, this ARM7 microcontroller consist of inbuilt flash, ROM, and SRAM internal memory devices, universal asynchronous receiver-transmitter (UART), serial peripheral interface (SPI), analog-to-digital converter (ADC), universal serial bus (USB), real-time clock(RTC), Pulse width modulation controller(PWM),GPIO lines and external input pins.

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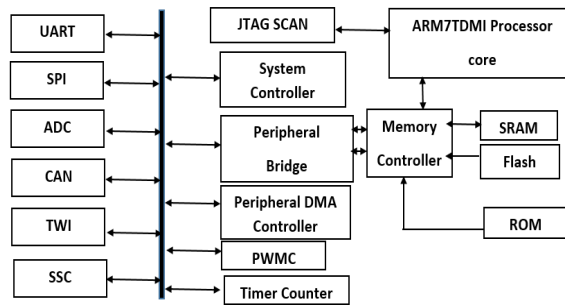


Fig. ARM-7 based microcontroller architecture [1]

## B. Platform Architecture

The architecture of hardware platform and physical implementation is shown in fig.2(a) and fig.2.(b) respectively . this platform consist of two LPC2148 microcontrollers connected via serial bus ie .UART1 . Max232 is used for the serial communication. ARM microcontroller 1 is and primary unit of our system. on this microcontroller we have implemented a “Smart library assistant device”. 4x4 Keyboard and 16x2 LCD display are used as a input and output device respectively. This device will show the location of book’s section. Example- If user will search for the books for Microcontrollers, device will show “SECTION 6”. As all related books for microcontroller are kept in “Section 6”. For the DPM techniques, each processor will independently choose its modes of operation via software clock controlling. For peripheral power down, a separate circuitry is designed using opto-coupler circuit as shown in fig. 2.(a). the AT89c51 processor core 3 (3) microcontroller is controlling the opto-coupler circuit for peripheral power down. In this system, we are controlling two peripherals ADC and RTC.

Implementation of fault tolerance is done on secondary unit. ARM microcontroller 2 is used as spare unit. This unit is also connected to PC for observation of fault tolerance and replacement of keyboard and display.

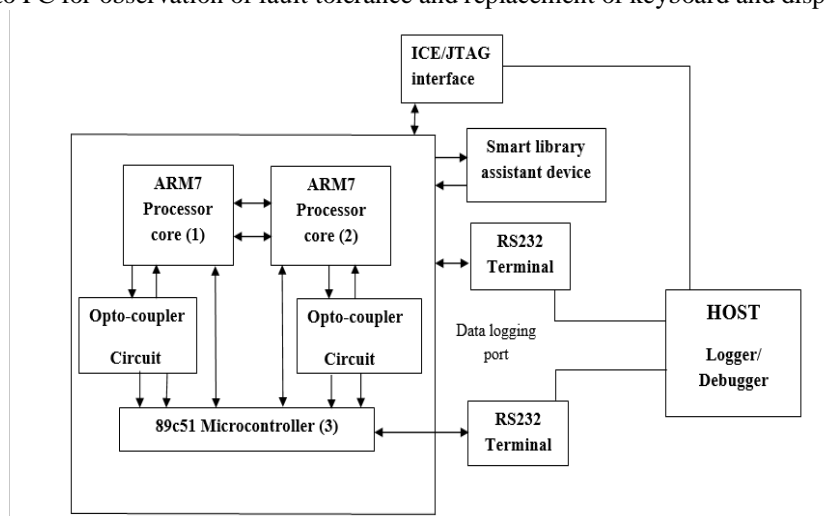


Fig. 2.(a) Hardware platform block diagram

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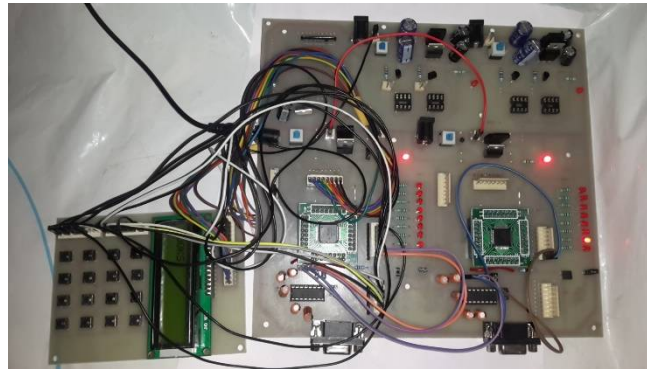


Fig.2.(b) Hardware platform implementation

### III. POWER MANAGEMENT UNIT

In any embedded system, high performance is needed only for a small fraction of time, while for the rest of time low-performance and low-power is allowed. The peak computing rate needed is much higher than average rate required.

#### A. DPM

DPM usually have only two operation states for systems component, namely *active* and *idle*. The processor power consumption can be reduced by switching off the processor clock when it enters to idle mode while waiting of an interrupt. In this technique, after completion of task each processor will enter itself in idle mode. Primary unit executes the task, as it will display the book's section. After completion of task it will switch itself into idle mode. Secondary unit will be always in idle mode unless fault occurs.

#### B. Peripheral power down

We are using hardware peripheral power down technique. In this system, externally system peripherals will be switched on and switched off. As we have two peripherals to control, ie. ADC and RTC. Microcontroller AT89C51 will receive the signal from ARM microcontrollers based on workload peripherals are operated. In this system, we are using a opto-coupler circuit as shown in fig.2(a).

### IV. FAULT TOLERANCE UNIT

Fault tolerance consists of fault detection and fault correction. In this system, hardware redundancy technique is used, as redundancy is simply the addition of information, resources, or time beyond what is required for normal system operation. However, we have chosen standby sparing hardware redundancy technique. There are two types of standby sparing techniques. If spare unit is continuously active and executing same task as primary unit is hot standby sparing, this system is prepared to take over any time. If spare unit is in idle mode, and fault has occurred then it is cold standby sparing technique. the proposed system is soft-real time, therefore cold standby sparing is applied.

The first step toward fault tolerance is error detection. The error detection mechanism is based on both software techniques (eg. Arithmetic codes [3], and program result checking [3]) and hardware techniques (eg. parity checking, watchdog timer, instruction counting, and signature checking [3]). In our system we are using program result checking error detection mechanism.

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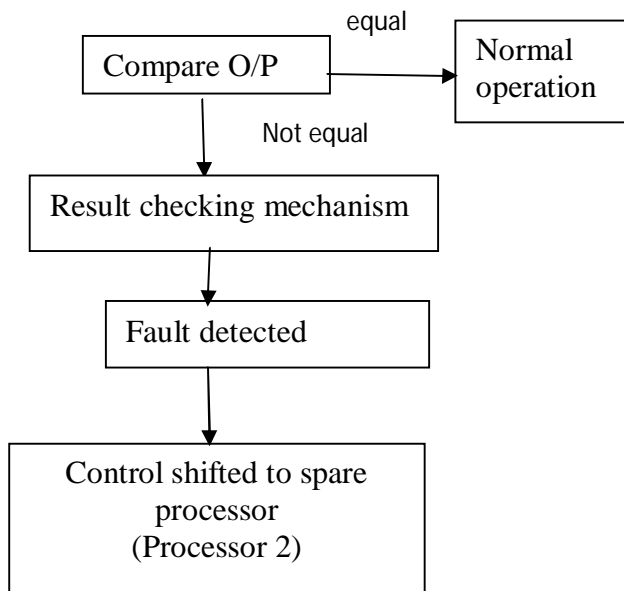


Fig.3 . Fault tolerance design flow

## V. EXPERIMENTAL RESULTS

The LPC2148 provides two reduced power mode: idle mode and Power down mode. Power consumption of ARM processor is given in following table -I

TABLE-I

### POWER SAVING MODES OF PROCESSORS

No of Processors	Active mode	power down mode
One processor	165mW	265mW
Two processors	330mW	103mW
Three processors	430mW	3900μW

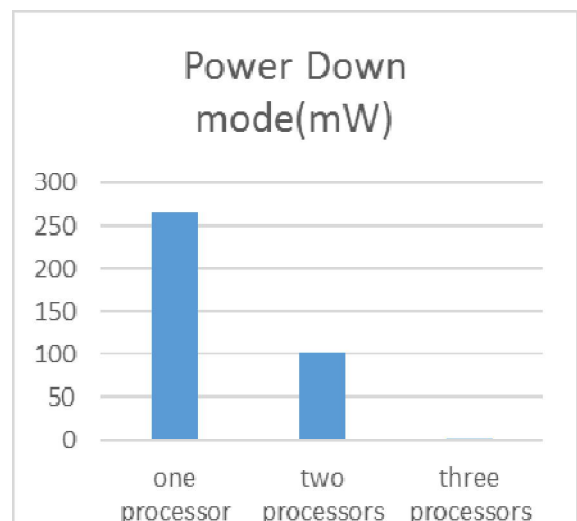


fig.4. Power consumption of the system based on Processors

The power consumption of processors are more than the peripherals, but peripherals also contributes in power

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consumption. In LPC2148 microcontroller, Power control register(PCON) special function register (SFR) is used to for selecting the operational modes. Also for 89C51 microcontroller, PCON is used for selecting modes. Peripheral power down can also be done by software method by using PCONP special function register.

The power consumption increases with application as I/O pins consumes most of the power. At run time of application, power consumption observed in the system is given in TABLE-II.

The power consumption increases with application as I/O pins consumes maximum of the power. At run time of application, power consumption observed in the system is specified in TABLE-II.

TABLE-II

### POWER CONSUMPTION SMART LIBRARY ASSISTANT DEVICE(WATT)

Components	Power Consumption
LCD Display	8.2mW
GPIO	4W
Processor 1	165mW
Total power	4.1732 W

The power consumption during fault tolerance is specified in TABLE-III

TABLE-III

### POWER CONSUMPTION DURING FAULT TOLERANCE(WATT)

Components	Power Consumption
UART0	0.5W
UART1	0.5W
Processor 2	165mW
Total power	1.16W

The above observation shows that the power consumption of system also depends on the workload, if work load is more power consumption is more. Also power consumption is more when I/O are busy. Power consumption during normal workload is observed to be 4.1732W, at fault-tolerant condition power consumption of the system is observed as 1.15 W.

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Power consumption of proposed system on the basis of workload is represented as given in fig.5

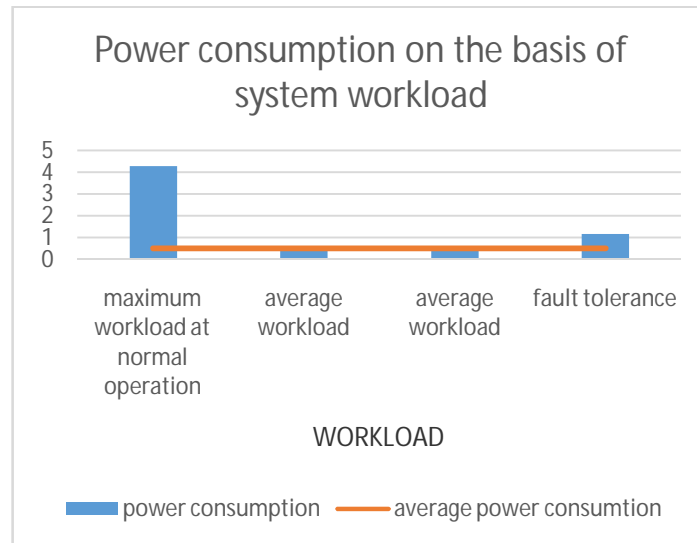


fig 5. Power consumption in the basis of workload

## VI. EXTENSION AND FUTURE WORK

The proposed hardware platform works as experimental setup for different research projects, various low power techniques and fault tolerance techniques. The platform can be used for following research work-

1. The low power hard real time system can be implemented by using this platform.
2. The different fault tolerance techniques can be implemented such as “2 out of “2 hardware redundancy with voter [1], [13], N- version programing [1][11] and many more.
3. The two microcontrollers are connected in such a way that they can interrupt, restart and turn on/ off each other [1].
4. Each of the microcontroller can access the internal parts of the other via JTAG [1], this will be helpful to implement fault detection mechanism that require comparing parts of a processor with their correspondents in the other one [1].
5. There are interconnections to transfer date, internal, states, and check points between the microcontrollers [1].

## VII. CONCLUSION

In this system, we propose a platform for power management techniques and fault tolerance techniques for multiprocessor embedded system. By using Peripheral power down and DPM techniques minimum power consumption can be achieved for “Smart library assistant device”. The platform is also equipped with power measurement unit, debugging unit and facilities for experimenting with different fault tolerance techniques. Although this platform is general and can be designed for any COTS devices and embedded processors.

## VIII. ACKNOWLEDGMENTS

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