

VLSI Implementation of Low Power Decompressor Using PRESTO Generator

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ABSTRACT: This paper deals with a low-power programmable (PRESTO) generator for creating pseudo-random test patterns with desired toggling levels and improved fault coverage versus the state-of-the-art built in self test (BIST) based pseudorandom test pattern generator. A PRESTO generator involves a linear finite state machine (linear feedback shift register or a ring generator) and an auxiliary circuit driving the required binary sequence to a phase shifter to obtain the desired test pattern. The auxiliary circuit comprising of various components creates an auxiliary output so as to enable/disable certain values in the input binary sequence to the Phase Shifter. This paper also discusses about the Low Power Decompressor application of PRESTO generator to derive the required test pattern at a better compact design, improved time delay and reduced power consumption. In the LP Decompressor, the output of the phase shifter is fed to a Transition Controller which reduces the switching transitions further reducing the power consumed. The above proposed application is simulated using Synopsys tool for HDL design and the results obtained are compared with existing technique.

KEYWORDS: Linear feedback shift register (LFSR), Built in self test (BIST), Pseudorandom test pattern generators (PRPGs), Low Power Decompressor (LP).

I. INTRODUCTION

The Test pattern generator produces test vectors that are applied to the tested circuit during pseudo-random testing of combinational circuits. The nature of the generator thus directly influences the fault coverage achieved the influence of the type of pseudo-random pattern generator on stuck-at fault coverage. Linear feedback shift registers (LFSRs) are mostly used as test pattern generators, and the generating polynomial is primitive to ensure the maximum period. We have shown that it is not necessary to use primitive polynomials, and moreover that their using is even undesirable in most cases. This fact is documented by statistical graphs. Built-in self-test enables the chip to test itself and to evaluate the circuit's response. Thus, the very complex and expensive external ATE (Automatic Test Equipment) may be completely omitted, or its complexity significantly reduced. Moreover, BIST enables an easy access to internal structures of the tested circuit, which are extremely hard to reach from outside. There have been proposed many BIST equipment design methods.

In most of the state-of-the-art methods some kind of a pseudorandom pattern generator (PRPG) is used to produce vectors to test the circuit. These vectors are applied to the circuit either as they are, or the vectors are modified by some additional circuitry in order to obtain better fault coverage. Then the circuit's response to these vectors is evaluated in a response analyser [4]. Usually, linear feedback shift registers (LFSRs) or cellular automata (CA) are used as PRPGs, for their simplicity. Patterns generated by simple LFSRs or CA often do not provide a satisfactory fault coverage. Thus, these patterns have to be modified somehow. One of the most known approaches is the weighted random pattern testing. Here the LFSR code words are modified by a weighting logic to produce a test with given probabilities of occurrence of 0's and 1's at the particular circuit under test (CUT) inputs [14]. Many papers dealing with the computation of the weights and the design of the weighting logic have been published.

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This paper is organized as follows, section 2 represents about existing methods are PRESTO generator and full operational PRESTO generator is explained with complete operation in detail. Section 3 represents low power de-compressor work in detail. Section 4 introduces proposed method low power de-compressor with transition controller. Section 5 simulated and experimental comparison results.

II. RELATED WORK

Fig.1 shows the basic structure of PRESTO Generator. An n-bit PRPG connected with a phase shifter with supply scan chains frames a part of the generator for creating the pseudorandom test patterns as shown in Fig1. A linear feedback shift register of 32-bit or a ring generator can execute a PRPG. More significantly, although, n hold latches are put between the PRPG and the phase shifter [13]. Every hold latch is exclusively controlled through a relating phase of an n-bit toggle control register. As long as its enable input information is stated, the given latch is transparent and then information goes from the PRPG to the phase shifter, and it is said to be in the toggle mode. When the latch is disabled, it catches and stores, for various clock cycles, the relating bit of PRPG, in this manner sustaining the phase shifter with a period of time. It is currently in the hold mode. It is important that every phase shifter yield is acquired by XOR-ing outputs of three distinctive hold latches [15]. As stated previously, the toggle control register operates the hold latches. Its substance contains 1s, where 1s demonstrate latches in the toggle mode, accordingly transparent for information approaching from the PRPG. Their portion decides a scan chain switching activity. The control register is reloaded once per pattern with the substance of an extra shift register. The enable signals infused into the shift register are created in a probabilistic manner by utilizing the first PRPG with a programmable arrangement of weights. The weights are resolved by four AND gates delivering 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate permits allowing probabilities beyond basic powers of 2.

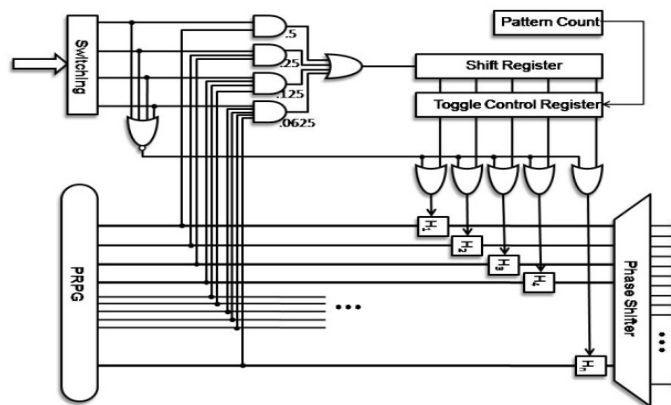


Fig. 1. Basic Architecture of PRESTO

A 4-bit Switching register is utilized to enable the AND gates and permits selecting a user defined level of switching activity. If the switching code is 0100, it will set to 1 and control register make 25% of hold latches to be enabled. An extra 4-input NOR gate distinguishes the switching code 0000, which is utilized to turn the LP functionality off [9]. It is significant that is working in the weighted random mode, the switching level selector selects the different probabilities and generate 1 as its carries. Therefore, generally a similar part of scan chains will remain in the Low power mode, however an arrangement of real low toggling chains will continue changing starting with one test pattern then onto the next. It will relate to a specific level of toggling in the scan chains.

PRPG is developed by 32-bit LFSR [10] and the polynomial equation $X^{32} + X^{22} + X^2 + X + 1$, for which we can generate random outputs. Power reduction is mainly depends on technology characteristic of gates employed [2]. LFSR is a shift register whose input is resulting of XOR gate some of its input. The output of flip-flops is loaded with seed value anything expects zero's which cause LFSR to produce all 0 patterns and when LFSR is clocked, PRPG generate 0's and 1's [5].

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A. ENHANCED VERSION OF PRESTO GENERATOR

Much higher adaptability in shaping low-toggling test patterns can be achieved by a deploying a scheme presented in Fig. 2. Basically, this approach breaks up a moving time of each test pattern into an arrangement of exchanging hold and toggle intervals. To move the generator forward and backward between these two states, we utilize a T-type flip-flop that switches at point there is a 1 on its information input. On the off chance that it is set to 0, the generator enters the hold time frame with all latches for a limited period of time and disabled despite of the control register content. This is proficient by putting AND gates on the control register outputs to permit solidifying of all phase shifter inputs. The T flip-flop is set to 1 then the latches enabled through the control register can send test information moving from the PRPG to the scan chains. Two extra parameters kept in 4-bit Hold and Toggle registers decide to what extent the whole generator remains either in the hold mode or in the toggle mode, separately. To end either mode, a 1 must happen on the T flip-flop input [8]. This weighted pseudorandom signal is delivered in a way like that of weighted logic used to strengthen the shift register.

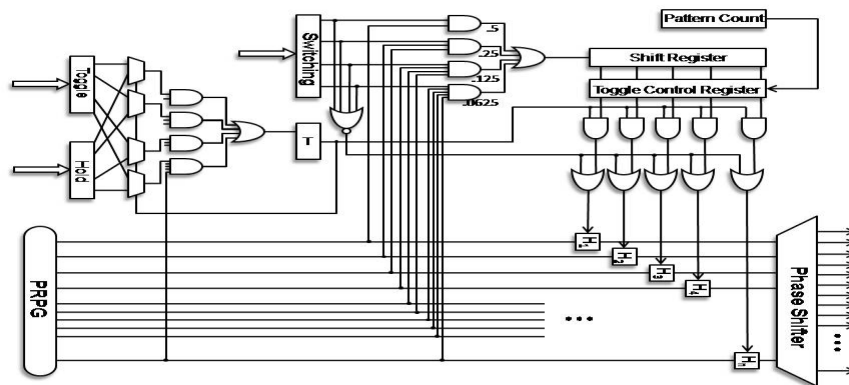


Fig. 2. Enhanced version of PRESTO Generator

The T flip-flop controls additionally four 2-input multiplexers directing information from the Toggle and Hold registers. It permits selecting an origin of control information that will be utilized as a part of the following cycle to conceivably change the operational method of the generator. For instance, when in the toggle mode, the information multiplexers watch the Toggle register. Once the weighted logic yields 1, the flip-flops toggles, and therefore all hold latches solidify in the last recorded state. They will stay in this state until another 1 happens on the weighted logic output. The random event of this occasion is presently identified with the substance of the Hold register, which decides when to end the hold mode [1].

III. PROPOSED ALGORITHM

The aim of the Low Decompressor is to disable both weighted common logic blocks (V and H) and to deploy control data instead as shown in Fig. 3. A multiplexer positioned in the front of the shift register select the content of the toggle and control register. The Toggle and control registers are employed to alternately preset a four-bit binary down counter, and to determine durations of the toggle and hold states. When this circuit reaches the zero value, it reasons a dedicated signal to go high to toggle the T flip-flop. The identical signal allows the counter to have the input data kept in Toggle or control register entered as the next state. Both the T flip-flop and the down counter want to be initialized for each test pattern. The initial value of the T flip flop decides whether or not the Decompressor will begin to operate both inside the hold mode or within the toggle mode, while the initial value of the counter referred to as offset, determines mode's duration [12]. T Flip-flop remains same as that of LP PRPG. It occurs two cases, first is the encoding procedure

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can completely disable the hold phase by loading hold register with correct code. If no hold it overrides the T flip-flop by using the additional OR gate. Now, it generates the test patterns from the phase shifter. 1st of all, the cryptography procedure might utterly disable the hold part (when all hold latches area unit blocked) by loading the Hold register with associate degree applicable code, as an example, 0000. If detected (No Hold signal within the figure), it overrides the output of the T flip-flop by exploitation an extra logic gate [11]. As a result, the whole take a look at pattern goes to be encoded among the toggle mode solely.

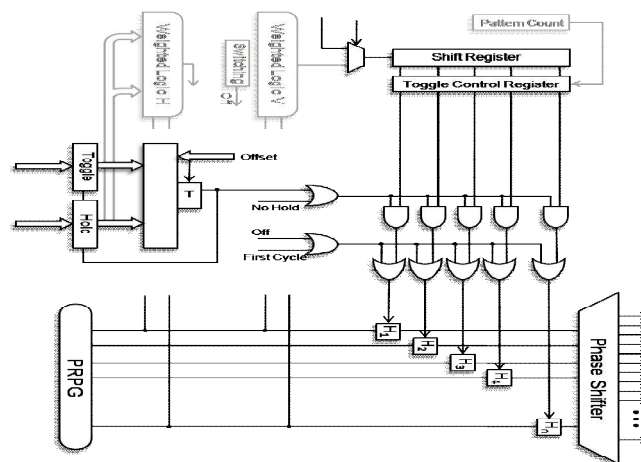


Fig. 3. Low Power Decompressor

Additionally, all hold latches got to be properly initialized [7]. Hence, an impression signal 1st cycle made at the tip of the ring generator data format part reloads all latches with the present content of this a part of the decompressor. Finally, external Ate channels (feeding the initial PRPG) permit one to implement a continual flow take a look at information decompression paradigm like the dynamic LFSR reseeding.

A. LOW POWER DECOMPRESSOR WITH TRANSITION CONTROLLER

In the proposed system, extra block transition controller is added in order to consume less power and produces less controlled transitions on phase shifter output is shown in fig 4. This adaptive technique reduces the power. During the shift mode the previous test patterns in scan flip-flops are given as feedback to the transition controller which is used to generate the test patterns such that switching is reduced [6]. Fig. 5 shows Transition Controller Block which is connected to the phase shifter output of Low Power Decompressor and test patterns are generated with better toggling rate from Multiple Input Signature Register of Transition Controller block.

The transition controller block as shown in Fig.5 includes multiplexer, a XNOR gate and D flip-flop. The output of XNOR gates connects as a multiplexer selects input the value of XNOR gate is 0 the D flip-flop holds previous value or it updated by a phase shifter output. Multiple input signature register (MISR) works depending on polynomial equation $X_{32} + X_{22} + X_2 + X_1 + 1$, for which we can generate random outputs. MISR consists of D flip flops, XOR gates

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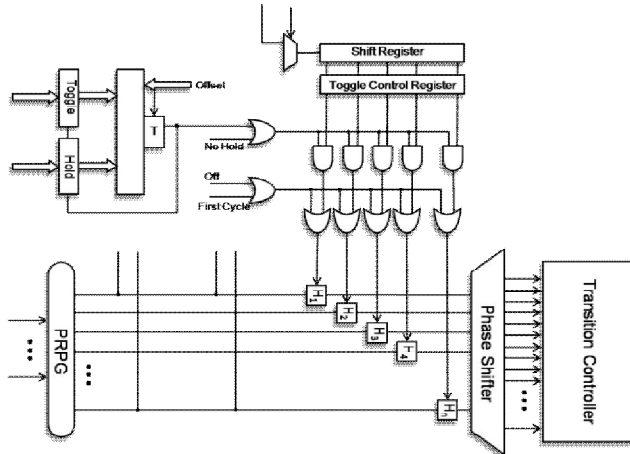


Fig. 4. Low Power Decompressor with Transition Controller

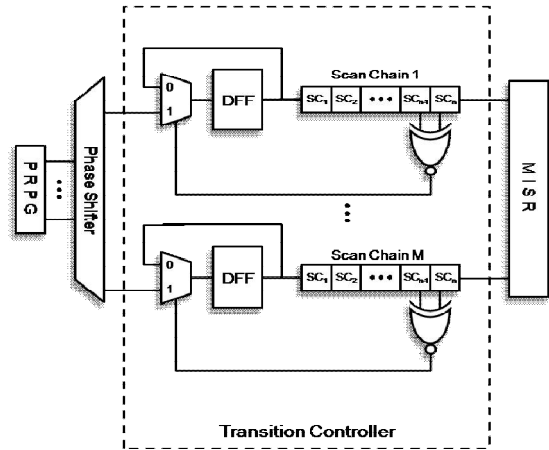


Fig. 5. Transition Controller

[3]. The coefficients of polynomial equation are given by XOR of output of previous flip flop and the input. Remaining coefficients are given by XOR of previous flip flop output and the MSB of MISR and it is again XOR-ed with input.

IV. SIMULATION RESULTS

The efficiency of the work is analysed using synopsis tools for both simulation and synthesis report.

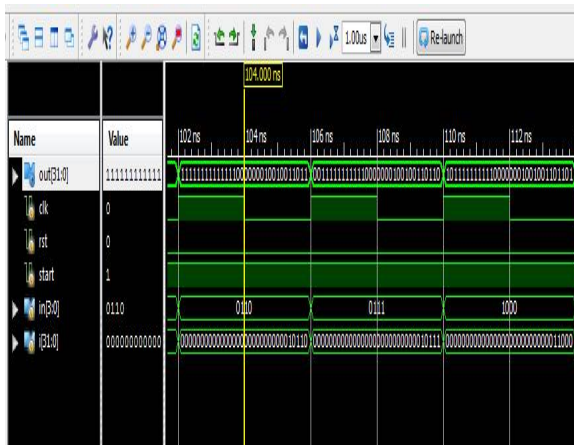


Fig. 6. Basic Architecture of PRESTO Generator

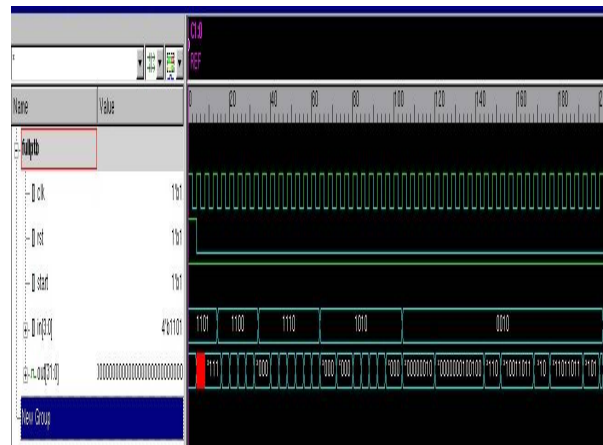


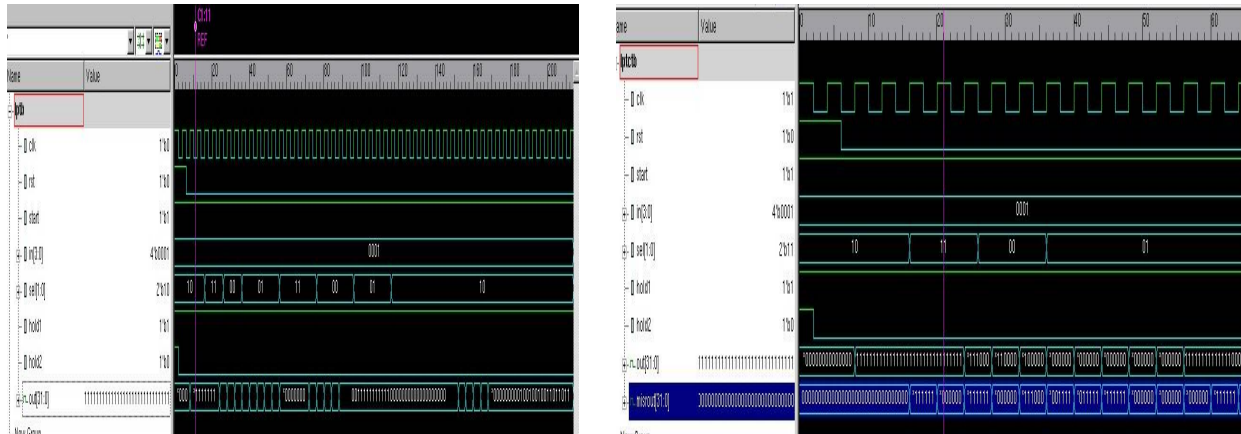
Fig. 7. Enhanced Version of PRESTO Generator

The simulation result in Fig. 6 shows that depending on the switching activity input corresponding to hold latches hold the output of LFSR and toggling rate decreases that shown in the waveform of Basic Architecture of PRESTO Generator. Fig. 7 shows that Enhanced Version of PRESTO Generator represents that in addition to switching activity, Toggle and Hold registers helped us to control the toggling activity of test patterns further.

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The simulation result in Fig. 8 shows that toggle and hold activity will be controlled for certain period of time which are independent of switching activity and produce the better toggling rate compare to Enhanced Version of PRESTO Generator and Fig. 9 shows that Transition Controller block added to Low Power Decompressor for better toggling is shown in waveform.

VLSI IMPLEMENTATION

S.NO	Test pattern generation & compression techniques	Area-Report	Timing- Report	Power consumption
1.	Basic PRESTO Generator	8199.703nm	16.80ns	70.41μw
2.	Enhanced PRESTO Generator	8453.424nm	19.83ns	51.37μw
3.	Low-power decompressor	7869.353nm	19.72ns	41.68μw
4.	Low-power decompressor with Transition controller	8078.536nm	19.70ns	30.40μw

The above tabular form represents Synthesis Report about the Area, Delay and Power Consumption for different architectures by Synopsis tool. Low Power Decompressor with Transition Controller gives better results.

V. CONCLUSION AND FUTURE WORK

In this paper PRESTO generator is designed using LFSR to decrease the toggling rate which results in low switching power, Area and timing. Low power decompressor and low power decompressor with transition controller were designed to reduce above parameters mentioned compare to PRESTO generator. Generated test patterns were applied to multiplexer to detect faults in the design. This LP PRPG is also capable of acting as a fully functional test data decompressor with the ability to control scan shift-in switching activity. Future, we can introduce for 64-bit and 128-bit for PRESTO generator for further reducing power dissipation.

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