

Efficient Implementation of Sum of Power of Two (SOPOT) Structure

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ABSTRACT: The proposed system uses a consumer wireless recording device to collect Electrooculography and employs new encoding or decoding paradigms to convey users intentions with eye movements including blinking and looking up. Discrete wavelet transform is used for decomposing the data segments into series of lower resolution components. In the SOPOT structure for efficient hardware implementation assuming all multipliers involved are constant. Multipliers are replaced with adders and shifters only which lead to multiplierless realization. The lifting structure is used to determine the algorithm. The purpose of decomposing the given shift by a series of fixed and larger shifts and a final stage of small variable shift is to avoid using programmable shifts with a larger shifting range, which may consume large hardware resources. To reduce the hardware complexity and power consumption of Electrooculography based human machine interface system a novel multiplierless implementation is developed.

KEYWORDS: SOPOT-Sum of Power of Two, Discrete wavelet transform

I. INTRODUCTION

The discrete wavelet transform (DWT) is a multi-resolution analysis tool with good resolution in the time and frequency domains. The DWT offers higher coding efficiency, compression ratio, and quality of image restoration than the traditional discrete cosine transform. As a result, the DWT is accepted in compression standards such as MPEG-4 and JPEG 2000. In numerical analysis and functional analysis, a discrete wavelet transform (DWT) is any wavelet transform for which the wavelets are discretely sampled. In any discretized wavelet transform, there are only a finite number of wavelet coefficients for each bounded rectangular region in the upper half plane. Still, each coefficient requires the evaluation of an integral. In special situations this numerical complexity can be avoided if the scaled and shifted wavelets form a multiresolution analysis. The main feature of DWT is multiscale representation of function. By using the wavelets, given function can be analysed at various levels of resolution. The DWT is also invertible and can be orthogonal.

In any discretised wavelet transform, there are only a finite number of wavelet coefficients for each bounded rectangular region in the upper half plane. Still, each coefficient requires the evaluation of an integral. In special situations this numerical complexity can be avoided if the scaled and shifted wavelets form a multiresolution analysis. The discrete wavelet transform has a huge number of applications in science, engineering, mathematics and computer science. Most notably, it is used for signal coding, to represent a discrete signal in a more redundant form, often as a preconditioning for data compression. Practical applications can also be found in signal processing of accelerations for gait analysis, in digital communications and many others.

It is shown that discrete wavelet transform (discrete in scale and shift, and continuous in time) is successfully implemented as analog filter bank in biomedical signal processing for design of low-power pacemakers and also in ultra-wide band (UWB) wireless communications. One famous example of lifting structured [4] FB commonly used in image compression is the 9/7 FB. Fig. 3 shows a general lifting structure, which is parameterized by two scaling

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 12, December 2016

constants C_0, C_1 and M lifting coefficients $p_m, m = 0, 1, \dots, M-1$. The z transform of the analysis filter pairs $[H_0(z), H_1(z)]$ and synthesis filter pairs $[F_0(z), F_1(z)]$ in the lifting structure can be written as

$$H_0(z) = C_0 H^{(M-2)}(z) \text{ and } H_1(z) = C_1 H^{(M-1)}(z) \text{ ---- (1); } F_0(z) = H_1(-z) \text{ and } F_1(z) = -H_0(-z) \text{ ---- (2)}$$

Where $H_0(z) = z^{-1} + p_0 Q(z)^2$ and $H^m(z) = z^{-2} H^{m-2}(z) + p_m Q(z)^2 H^{m-1}(z)$ with $Q(z) = (1+z^{-1})/2$ and $H^1(z) = 1$ for $m = 1, 2, \dots, M-1$.

II. RELATED WORK

This paper presents an efficient genetic approach to the design of digital finite impulse response (FIR) filters with coefficients constrained to be sums of power-of-two terms. To obtain such efficiency, i.e. a reduction of computational costs and an improvement in performance, a specific filter coefficient coding scheme has been studied and implemented. The resulting genetic algorithm (GA) is explained and compared experimentally with other state-of-the-art design techniques on several power-of-two FIR filter design cases.[1] It can be seen that the proposed genetic technique is able to attain results as good as or better than the other methods. Moreover it can be easily implemented on parallel hardware.

The fixed-coefficient filters can be implemented efficiently using sum-of-power-of-two (SOPOT) coefficients and the multiplier-block technique, which gives minimum adder realization. Apart from the multipliers required in the SRC, the digital IF can be implemented without any multiplications. While most multiplier-less filter design and realization methods address only the coefficient round-off problem by minimizing the number of SOPOT terms used, the proposed design methodology aims to minimize more realistic hardware[2] complexity measure, such as adder cells and registers, of the digital IF subject to a given spectral and accuracy specifications. The motivation is that the complexity is closely related to the target output accuracy, which is specified statistically by its total output noise power generated by rounding the intermediate data.

It is well known that if each coefficient value of a digital filter is a sum of signed power-of-two (SPT) terms, the filter can be implemented without using multipliers. In the past decade, several methods have been developed for the design of filters whose coefficient values are sums of SPT terms. Most of these methods are for the design of filters where all the coefficient values have the same number of SPT terms. It has also been demonstrated recently that significant advantage can be achieved if the coefficient values are allocated with different number of SPT terms while keeping the total number of SPT terms for the filter fixed. In this paper, we present a new method for allocating the number of SPT [7] terms to each coefficient value.

III. MOTIVATION

The motivation behind this project is based on a new single-channel EOG-HMI system with efficient hardware implementation is developed in this brief. In the proposed EOG-HMI, EOG signals are recorded from a commercial single-channel EEG/EOG[9] acquisition system, namely, Mind Wave Mobile Headset (Neuro Sky, CA, USA), and the user's intention is encoded by combinations of eye movements. The headset places only one dry electrode on the forehead of the user to record[11] mixed EEG/EOG activities and transmits signals to a computer or other hardware system via Bluetooth. Hence, the EOG-HMI equipped with the Mind-Wave Mobile Headset[8] is easy to use and has high mobility. Furthermore, this brief developed a new encoding/decoding paradigm and a hardware efficient system, which work[10] in tandem with the Mind Wave Mobile Headset in the EOG-HMI system. Since the headset used in our system places one dry electrode on the skin surface without any conductive gel in between and any fixed attachment, the noise level of EOG recorded by this headset appears to be relatively higher than that collected by conventional wet electrodes.

IV. CANONICAL SIGNED DIGIT

The canonical signed digit (CSD) representation is one of the existing signed digit (SD) representations with unique features which make it useful in certain DSP applications focusing on low-power, efficient-area and high-

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 12, December 2016

speed arithmetic [1]. The CSD code is a ternary number system with the digit set $\{1^- 0 1\}$, where 1^- stands for 1. Given a constant, the corresponding CSD representation is unique and has two main properties: (1) the number of nonzero digits is minimal, and (2) no two consecutive digits are both nonzero, that is, two nonzero digits are not adjacent. The first property implies a minimal Hamming weight, which leads to a reduction in the number of additions in arithmetic operations. The second property provides its uniqueness characteristic. However, if this property is relaxed, this representation is called the minimal signed digit (MSD) representation, which has as many non-zeros as the CSD representation, but which provides multiple representations for a constant. One sample example for canonical signed digit is $01111111 = 2^0 - 2^{-7} = 10000001 \Rightarrow 01101111 \rightarrow 01110001 \rightarrow 10010001 \Rightarrow k = 2^0 - 2^{-3} - 2^{-7}$

V. SUM OF POWER OF TWO (SOPOT)

An important advantage of lifting structure filter bank is perfect reconstruction. Two basic denoising functions, bandpass filtering and wavelet transform, involves a considerable number of multipliers, which are hardware and power intensive. But we are using implementing only Discrete Wavelet Transform. For efficient hardware implementation, take all multipliers involved as constant, and these can be expressed as SOPOT or canonical signed digit. The multipliers or coefficients are in the following SOPOT representation as shown in fig1

For each SOPOT term $a_k 2^{b_k}$, [1] the exact operation of the s-unit is controlled by a 7-bit control register sel_k , which specifies the sign of a_k in $sel_k(6)$, the polarity of shifting direction, i.e., the sign of b_k , in $sel_k(5)$, the number of rounds used to realize the smallest factor of 4, i.e., $|b_k|/4$, in $sel_k(4:2)$, and the remaining amount of shift, i.e., $|b_k| \bmod 4$, in $sel_k(1:0)$. hence, the overall coefficient λ in (3) can be computed by reusing one s-unit 1 times with the help of an accumulator.

The proposed SOPOT structure with 7 bit control bits fig.1 is given below. But for input mux there is no selection line until there's no selection line it won't select any line in it.

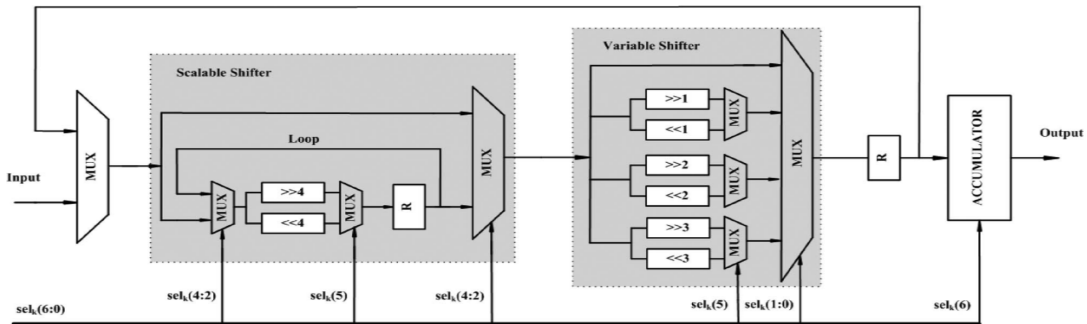


Fig 1. SOPOT Structure Unit

The below given Table 1 is for p_1 coefficient for each SOPOT terms have to define configuration for it. Table 1 shows the configurations of the second lifting coefficient p_1 of the lifting structured FB. Configurations for other SOPOT coefficients can be derived similarly.

Table 1 SOPOT structure

Coefficient	SOPOT terms	Configuration
P_1	-2^{-3}	1100011
	2^{-6}	0100011
	2^{-8}	0100010
	2^{-11}	1100011

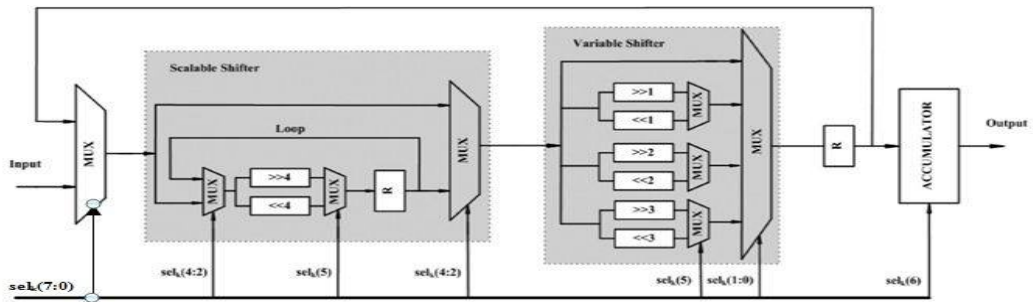
International Journal of Innovative Research in Science, Engineering and Technology

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VI. MODIFIED SOPOT STRUCTURE

The same coefficient is used in fig.2 but here the S unit is[1] controlled by 8 bit control register sel_k , which specifies the sign of a_k in $sel_k(6)$, the input is select with bit 7 as selection bit, the polarity of shifting direction, i.e., the sign of b_k , in $sel_k(5)$, the number of rounds used to realize the smallest factor of 4, i.e., $|b_k|/4$, in $sel_k(4..2)$, and the remaining amount of shift, i.e., $|b_k| \bmod 4$, in $sel_k(1..0)$. Hence, the overall coefficient λ in (3) can be computed by reusing one S-Unit L times with the help of an accumulator and input starts with zero shift. The same shift operation is used in this modified structure the SOPOT terms will be accumulated either in increasing order of their shifts (left and then right) so that only the incremental shift is required at each stage.



The modified SOPOT terms for coefficient p_1 and their configurations with 8 control bits is shown in Table 2. Table 2 shows the configurations of the second lifting coefficient p_1 of the lifting structured FB. Configurations for other SOPOT coefficients can be derived similarly.

Table 2
Modified SOPOT structure

Coefficient	SOPOT terms	Configuration
P1	-2^{-3}	01100011
	2^{-6}	10100011
	2^{-8}	10100010
	-2^{-11}	11100011

The given below Table 3 consists of coefficients and constants and each of their 9/7 filter bank with SOPOT representation respectively. Table 3 summarizes the SOPOT coefficients of the lifting structured FB, which are determined by the algorithm proposed in [2].

Table 3
SOPOT coefficients of the 9/7 filter banks

	9/7 Filter bank [4]	SOPOT representation
P_0	-3.17226868408289	$-2^{-2} + 2^0 - 2^{-2} + 2^{-4} + 2^{-6} - 2^{-11} + 2^{-13} - 2^{-15} + 2^{-18} - 2^{-20}$
P_1	-0.10596023714940	$-2^{-3} + 2^{-6} + 2^{-8} - 2^{-11}$
P_2	1.76582215102264	$2^1 - 2^{-2} + 2^{-6} + 2^{-12} - 2^{-14} + 2^{-16} - 2^{-20} - 2^{-22}$
P_3	0.88701370409649	$2^0 - 2^{-3} + 2^{-6} - 2^{-8} + 2^{-12} + 2^{-14} - 2^{-16} + 2^{-18} + 2^{-20} + 2^{-22}$
C_0	0.81289306611600	$2^0 - 2^{-2} + 2^{-4} + 2^{-11} - 2^{-13} + 2^{-15} - 2^{-18} + 2^{-23}$
C_1	0.61508705245638	$2^{-1} + 2^{-3} - 2^{-6} + 2^{-7} - 2^{-9} - 2^{-12} + 2^{-13} - 2^{-15} + 2^{-17} - 2^{-19}$

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VII. SIMULATION RESULTS

The simulation results given below fig 3 shows the output of SOPOT unit for each configuration and the total SOPOT term results in one coefficient value. The following results are for coefficient p1 .

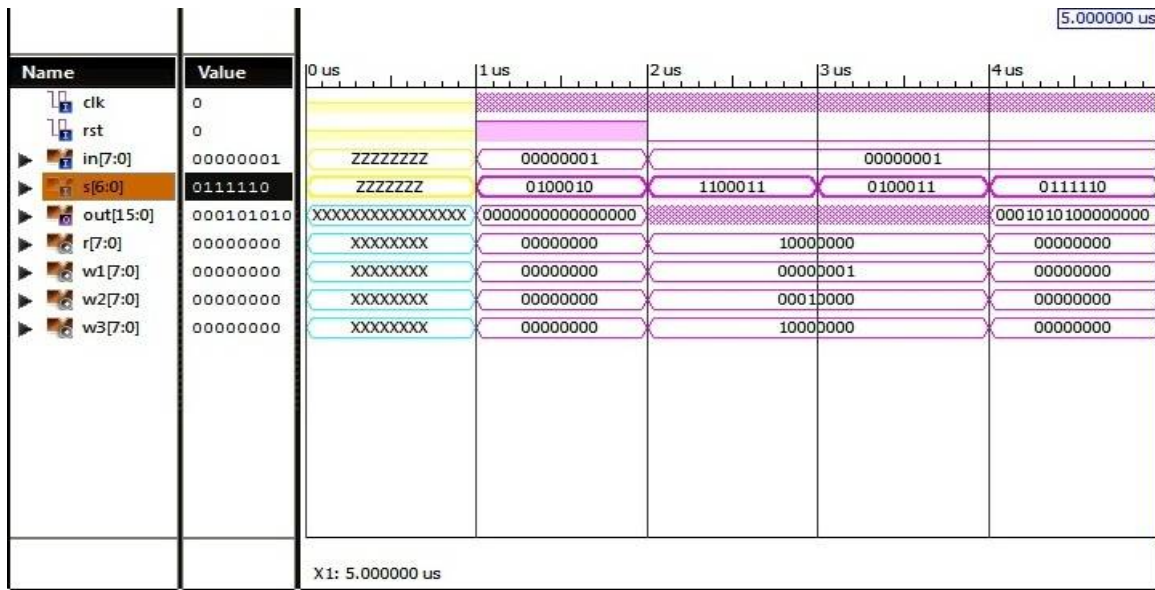


Fig.3 Output of SOPOT unit for coefficient p1

The following fig.4 is for one configuration each clock separated with 128 bit difference .

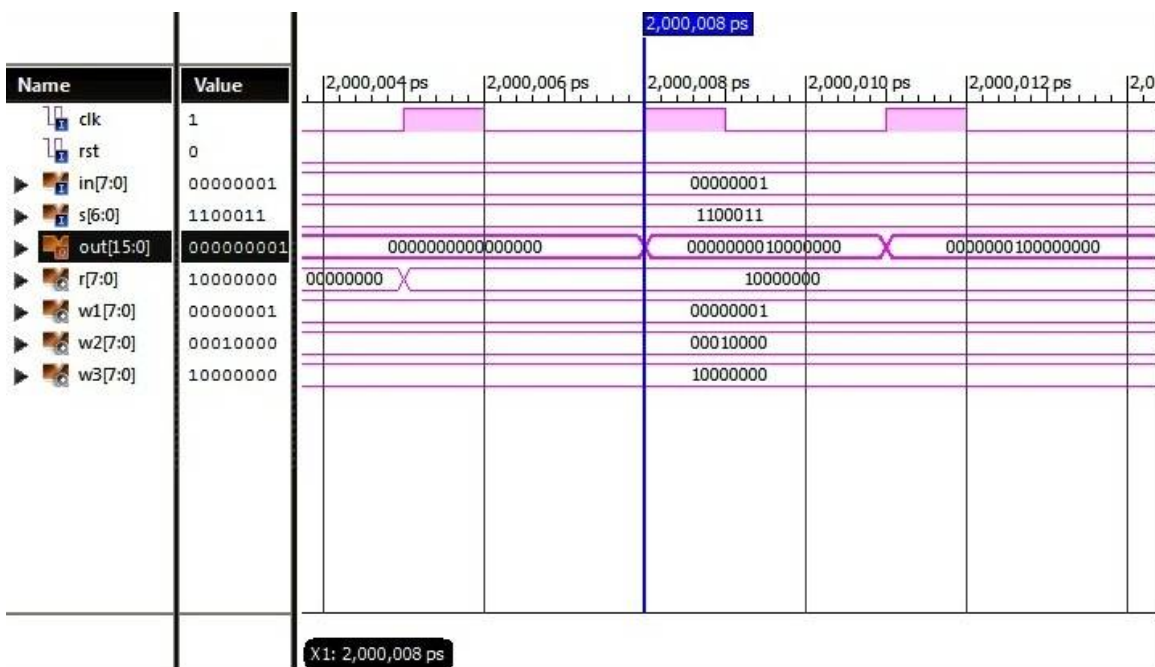


Fig.4 For the coefficient p1 with -2^{-3} as sopot term

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The following fig.5 shows the configuration of one of the SOPOT term i.e., the coefficient p1 with 2^{-6}

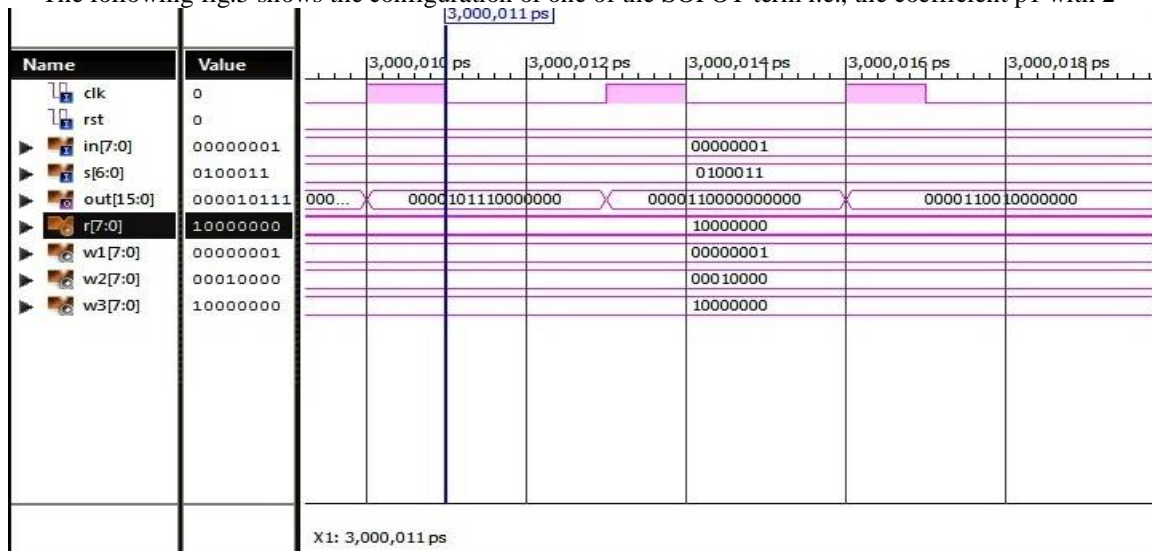


Fig.5 For the coefficient p1 with 2^{-6} as sopot term

DESIGN SUMMARY :

In this the percentage of utilization can be seen as how many number of flip flops ,number of slices it leads to power consumption, number of bounded IOBs. Even we can see project status in this design summary as shown in fig.6

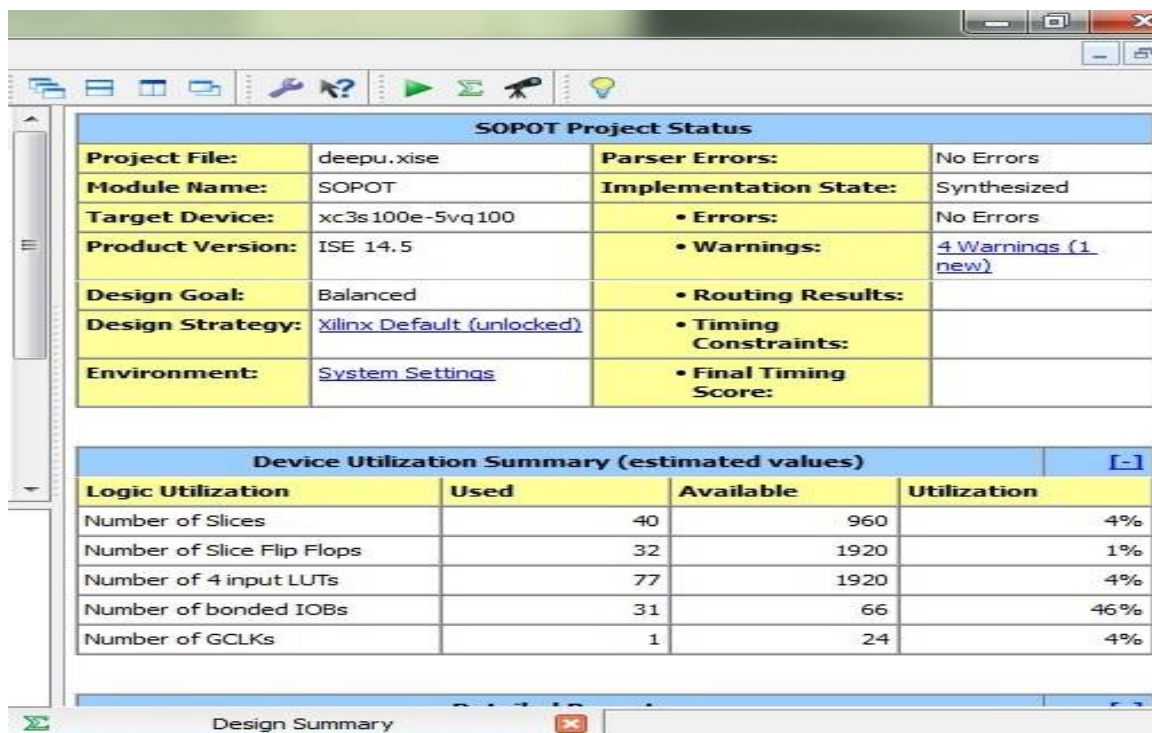


Fig.6 Design summary with logic utilization

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VII. CONCLUSION

The architecture and multiplierless implementation of a SOPOT representation have been presented. Experimental results show that the proposed SOPOT structure offers satisfactory performance in terms of classification accuracy, implementation complexity, and power consumption.

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