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A Novel Topology for Dual Unified Power Quality Conditioner

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ABSTRACT: This project presents a Novel topology for a dual unified power quality conditioner—iUPQC. The iUPQC is consists of two active filters, a series active filter and a shunt active filter (parallel active filter), used to eradicate harmonics and unbalances. Unlike from a conventional UPQC, the iUPQC has the series filter controlled as a sinusoidal current source and the shunt filter controlled as a sinusoidal voltage source. Hence, the pulse width modulation (PWM) controls of the iUPQC deal with a renowned frequency spectrum. This frequency spectrum is controlled using voltage and current sinusoidal references, unlike from the conventional UPQC that is controlled using nonsinusoidal references. In this project, the recommended design control, power flow analysis, and experimental results of the advanced prototype are presented.

KEYWORDS: Active filters, power line conditioning, control design, unified power quality conditioner.

I. INTRODUCTION

The practice of power quality conditioners in the distribution system network has enlarged during the past years due to the steady increase of nonlinear loads connected to the electrical grid. The current exhausted by nonlinear loads has a great harmonic content, varying the voltage at the utility gridand subsequently affecting the operation of critical loads.

Through using a unified power quality conditioner (UPQC), it is probable to ensure a controlled voltage for the loads, balanced and with low harmonic distortion and at the same time draining undistorted currents from the utility grid, even if the grid voltage and the load current have harmonic substances.TheUPQC contains of two active filters, the Series Active Filter (SAF) and the Shunt or Parallel Active Filter (PAF) [1], [2].

The Shunt filter is generally controlled as a non-sinusoidal current source, which is liable for compensating the harmonic current of the load;however the SAF is controlled as a non-sinusoidal voltage source, which is responsible for compensatingthe grid voltage. Both filters have a control reference with harmonic contents, and usually, these references might be attained through complex methods [4], [5], [14], [17], [21],[23].

Various works show a control technique to both PAF and SAFs which uses sinusoidal references without the necessity of harmonic extraction, in order to decrease the complexity of the reference generation of the UPQC.

An exciting alternative for power quality conditioners was proposed and it was called line voltage regulator/conditioner. This voltage regulatorinvolves of two single-phase current source inverters where the PAF is controlled by a voltage loop and the SAF is controlled by a current loop. In this way, both grid current and load voltage are sinusoidal, and therefore, their references are also sinusoidal.

Some authors have applied this concept, using voltage source inverters in uninterruptable power supplies and in UPQC [10], [25]. In [10], this concept is called "dualtopology of unified power quality conditioner" (iUPQC), and the control schemes use the p-q theory, requiring determination in real time of the positive sequence components of the voltages and the currents.

The aim of this paper is to suggest a simplified control technique for a dual three-phase topology of a unified power quality conditioner (iUPQC) to be used in the utility grid connection. The suggested control scheme is developed in

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ABCReference frame and allows the use of classical control theory without the requirement for coordinate transformers and digital control implementation. The references to both Series and PAFs are sinusoidal, dispensing the harmonic extraction of the grid current and load voltage.

II. DUAL UPQC

Classical UPQC arrangement is collected of a SAF andaPAF, as shown in Fig. 1. In this topology, the SAF works as voltage source in way to compensate the grid distortion, unbalances, and disturbances like sags, swells, and flicker.Consequently, the voltage compensated by the Series active filter is composed of a major content and the harmonics. ThePAF acts as a current source and it is responsible for reimbursing the displacement, unbalances,and harmonics of the load current, make sure a sinusoidal grid current.

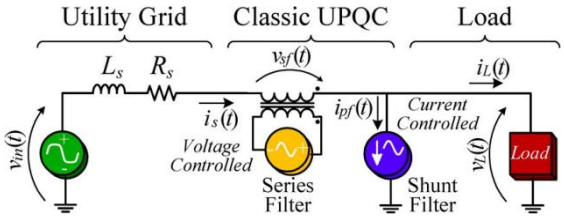

Fig. 1.Classical UPQC

The series filter construction to the utility grid is prepared through a transformer;however the shunt filter is ordinarily connected straight to the load, generally inlow-voltage grid applications. The classical UPQC has the resulting drawbacks: complex harmonic abstraction of the grid voltage and the load includingcomposite calculations, current voltageand references with harmonic contents demanding a high bandwidth control, and the leakage inductance of the series connection transformer disturbing the voltage compensation generatedby the series filter.

In order to reduce these drawbacks, the iUPQC is discovered in this project, and its structure is shown in Fig. 2.

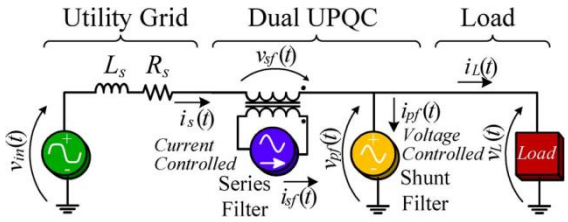

Fig.2. Dual UPQC (iUPQC)

The scheme of the iUPQC is muchrelated to the conventional UPQC, using an association of the PAF and SAF, differingonly from the way the shuntand seriesfilters are controlled.In the iUPQC, the SAF works as a current source, which inflictsa sinusoidal input current synchronized with the grid voltage.

The PAF acts as a voltage source which imposing a sinusoidal load voltage synchronized with the grid voltage. Like this, the iUPQC control uses sinusoidal references for both SAF and PAFs filters. This is a main point to noticeassociated to the conventional topology since the only request of sinusoidal reference generation is that it needto be synchronized with the grid voltage.

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The series active filter (SAF)worksas high impedance for the current harmonics and secondarilyrecompenses the harmonics, unbalances, and disturbances of the grid voltage meanwhile the connection transformer voltages are identical to the variance between the grid voltage and the loadvoltage. Correspondingly, the shunt active filter (PAF) secondarily compensates the unbalances, displacement, and harmonics of the grid current, providing a low-impedance lane for the harmonic load current.

III. POWER CIRCUIT

The power circuit of the existing iUPQC is fabricated with pair offour-wire three-phase converters coupled back to back and their particular output filters, as shown in Fig. 3. The three single-phase transformers are used to connect the SAFto the utility grid, whereas the PAF is joined directly to the load. Table I displays the specification of the iUPQC. The passive components are shown in Table II.

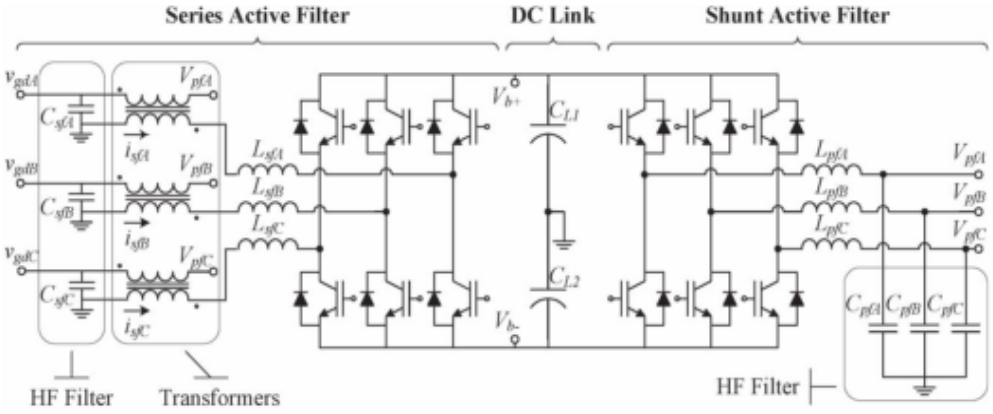

Fig.3. Power circuit of iUPQC

TABLE I
DESIGN SPECIFICATIONS OF THE iUPQC

Input line to line voltage	V_{in}= 220V
Output nomial Power	P_o= 2500VA
DC link voltage	V_b= 400V
Utility grid frequency	f_{grid}= 60Hz
Switching frequency of series and PAFs	f_s = 20kHz
Transformer ratio	n = 1

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TABLE II
COMPONENT SPECIFICATIONS OF THE POWER MODULE

Leakage Inductance of SAF coupling transformers	L*lg* = 2.33mH
Transformer ratio of the SAF coupling transformers	n = 1
SAF Inductances	L*sf*= 650μH
PAF Inductances	L*pf*=650μH
DC Link Capacitance	C*b* = 3mF

IV. OUTPUT PASSIVE FILTER DESIGN

The iUPQC circuit can be considered by a single-phase wiring diagram, as shown in Fig. 4.

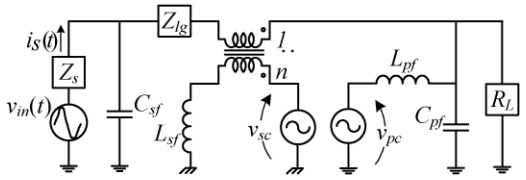

Fig.4. Single-phase wiring diagram of the dual UPQC

The utility grid impedance is signified by Zs= jωLs+ R s, while the coupling transformerleakage impedance is symbolized by Zlg = jωLlg+ Rlg, andthe voltage sources Vscand Vpcimply the equivalent structures of the series and shunt filters, which generate a waveformcomposed of the fundamental component and harmonics that originated from the commutation of the switches. These highfrequencies must be filtered by the output passive filters of theiUPQC, make sure sinusoidal grid currents and load voltages.

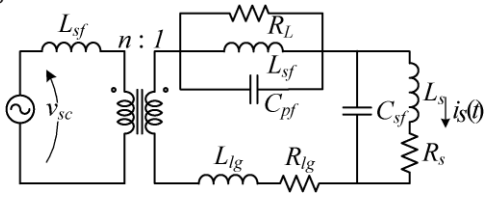

Fig.5. Equivalent circuit as viewed by SAF

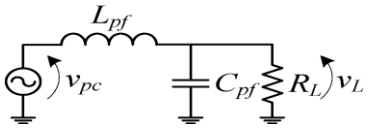

Fig.6. Equivalent circuit as viewed by PAF

Fig. 5 shows the equivalent circuit used for the SAF outputimpedance analysis, and Fig. 6 shows the equivalent circuitused for the PAF output impedance analysis. In order to shortenthe analysis of the PAF, the voltage source Vscand theinductance Lsf, which are series connected, were consideredas a current source.

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Noticing the equivalent circuits, we can claim that the PAFoutput impedance affects the frequency response of the SAF, while the SAF output impedance does not disturb the frequency response of the PAF. Hence, the output passive filter design of the iUPQC should be started with the PAF design trackedby the SAF design.The high-frequency filter transfer function of the PAF is derived by analysingthe circuit of Fig. 6 and is shown in

$$\frac{VL(s)}{Vpc} = \frac{1}{LpfCpf} \cdot \frac{1}{s^2 + s \cdot \frac{1}{CpfRl} + \frac{1}{LpfCpf}} \quad (1)$$

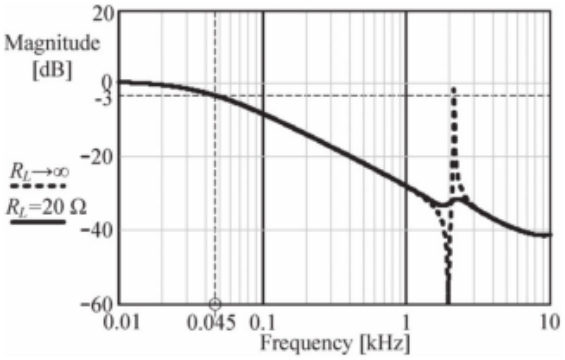

Fig.7. HF filter frequency response of the PAF

The inductor $L_{pf}$was defined by the power design, so thecapacitor C_{pf}will be defined according to the preferredcut-offfrequency of the filter. In this design, a 2.9-kHz cut-off frequencywas used, resulting in a value of 10μF for the C_{pf}filtercapacitor. Fig. 7 shows the PAF frequency response for theminimal load and no load.

The high-frequency filter transfer function of the SAF isderived by analysingthe circuit of Fig.5 and is shown in

$$\frac{is(s)}{vsc(s)} = \frac{n}{\{sLsf + n^2[sLlg + Rlg + \alpha + \beta] \cdot \gamma\}} \quad (2)$$

Where

$$\propto = \frac{sLpfRL}{s^2LpfCpfRL + sLsf + RL} \quad (3)$$

$$\beta = \frac{sLrd + Rrd}{s^2LsCsf + sCsfRs + 1} \quad (4)$$

$$\gamma = s^2Csf + sCsfRlg + 1 \quad (5)$$

As the inductor L_{sf}as defined by the power design, thecapacitor C_{sf}will be defined according to the desired cutofffrequency of the filter. In this design,a 45-Hz cut-off frequency.

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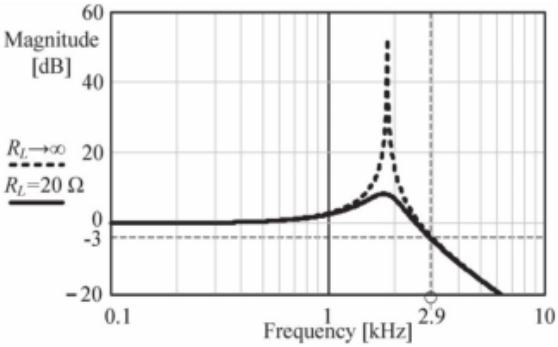

Fig.8. HF filter frequency response of the SAF

Fig.8shows the SAF frequency response for nominal load and nowas used, resulting in a value of 1μF for the C_{sf}.As the inductor $L_{sf}$was defined by the power design, thecapacitor C_{sf}will be defined according to the preferred cut-offfrequency of the filter. In this design a 45-Hz cut-off frequency. Fig.8 shows the SAF frequency response for nominal load and noload. It can be prominent that the filter response has a small cutofffrequency that can moderate the bandwidth of the SAF, decreasing its efficiency under operation with harmonic contents on thegrid voltage.

This characteristic of low-frequency attenuationis adverse and intrinsic to the structure due to the leakageimpedance of the coupling transformers.

V. PROPOSED CONTROL SCHEME

The proposed iUPQC control arrangement is an ABC reference structure based control, where the SAF and PAF are controlled in an independent way.

In the suggested control scheme, the power calculation andharmonic abstraction are not required since the harmonics, unbalances,disturbances, and displacement would be compensated.

The SAF has a current loop in order to make sure a sinusoidal grid current synchronized with the grid voltage. The PAF has a voltage loop to ensure a balanced controlled load voltage with small harmonic distortion. The SAF and PAF control loops areindependent from each other meanwhile they act independently in each active filter. The dc link voltage control is prepared in the SAF, where the voltage loop describes the amplitude reference for the current loop, in the same manner of the power factor converter control schemes. The sinusoidal references for both filter controls are generated by a digital signal processor (DSP),which make sure the grid voltage synchronism using a phase protected loop.

A.SAF Control

Fig. 9 shows the control block diagrams for the Series active filter (SAF). TheSAF control structure contains of two voltage loops and three identical grid currentloops. One voltage loop isliable for regulating the total dc link voltage, and the other is responsible for avoiding the unbalances between the dc link capacitors.The current loops are responsiblefor tracing the reference of each grid input phase in order tocontrol the grid currents individually.

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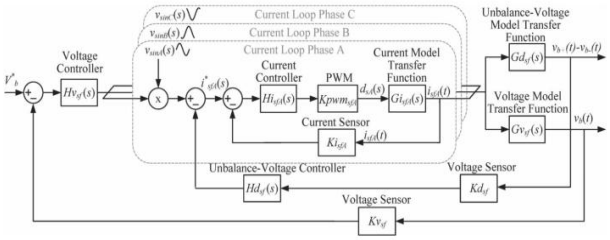

Fig.9. Control block diagram of the SAF controller

The total dc voltage regulator loop has a low-frequency responseand decides the reference amplitude for the currentloops. Hence, when the load increases, overcoming the inputgrid current, the dc link supplies transitorily the active power consumption, resulting in a decrease of its voltage. This voltage controller turns to increase the grid current reference, aiming to bring back the dc link voltage. In the similar way, when the load decreases, the voltage controller decreases the grid current reference to adjust the dc link voltage. Considering the threephase input current, sinusoidal and balanced, the voltage loop transfer function is attained through the method of power balance analysis. The three-phase four wire converter withneutral point can be represented by the circuit shown in Fig. 10,

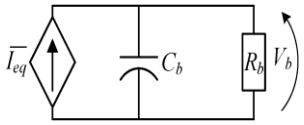

Fig.10. Equivalent circuit of the SAF voltage loop

Collected of a current source which is in parallel with the dc link impedance and whose current source signifies the average charge current of the dc link.

The resistor R_b is absent in the real circuit (R→8);it just represents instant active power consumption of the dc link. The term instant is related to the time of the switching period, since active power consumption of the dc linkis null for the utility grid voltage frequency. The average charge current of the dc link is given by

$$\overline{Ieq} = \frac{3}{2} \cdot \frac{n \cdot Vgdpk \cdot Isfpk}{Vb} \qquad (6)$$

The SAF peak current $I_{sfpk}$is considered the same for thethree phases due to balanced current. Through (6), the voltageloop transfer function is obtained and is represented by

$$Gvsf(s) = \frac{Vb(s)}{Isf(s)} = \frac{3}{2} \cdot n \cdot \frac{Vgdpk}{Vb} \cdot \frac{1}{\frac{1}{Rb} + sCb} \qquad (7)$$

Where
V_{gdpk}peak of the grid voltage;
V_b dc link voltage;
$R_b$load equivalent resistance;
$C_b$total dc link equivalent capacitance;
ntransformer ratio.
The open-loop transfer function ($OLTF_v$) is given by

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$$OLTFv(s) = Gvsf(s) \cdot \frac{Kvsf}{Kisf} \cdot Kmsf \qquad (8)$$

Where
K_{mfs}multiplier gain;
$K_v$voltage sensor gain;
K_{isf}current sensor gain;
The K_{mfs} gain is attained by considering the gain of the multiplier integrated circuit and the peak of the synchronizedsinusoidal signal generated by the DSP.

Pointing to regulate the total dc link voltage control, a proportional integral (PI)+pole controller was considered which ensures a crossover frequency of 4Hz and a phase margin of 45.Frequency response containing the open-loop transfer function (OLTFv), controllertransfer function (H_{vsf}), and compensated loop transfer function(OLTFv+ H_{vsf}).

The unbalanced-voltage control loop also has a low-frequency loop and performances on the dc level of the grid currentreference in order to keep the voltage balance in dc linkcapacitors. When a voltage unbalance occurs, this loop adds adc level to the references of the grid currents, aiming to balanceboth $C_{L1}$and C_{L2} voltages.

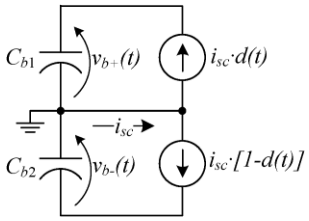

Fig.11. Equivalent circuit of the SAF unbalanced-voltage loop

The unbalanced-voltage loop transfer function is attainedthrough the analysis of the simplified circuit shown in Fig. 11.The four-wire converter permits the single-phase analysis, wheretwo current sources represent the current on the inverter switches. In Fig. 11, the current $I_{sc}(t)$ represents the currentthrough the neutral point, and d(t) represents the duty cycle.

Through the mesh analysis and by applying Laplace, theunbalanced-voltage loop transfer function is achieved andgiven by

$$Gdf(s) = \frac{Vb+(s) - Vb-(s)}{Isc(s)} = \frac{3}{2 \cdot s \cdot Cb} \qquad (9)$$

The open-loop transfer function ($OLTF_d$) is given by

$$OLTFd(s) = Gdsf(s) \cdot \frac{Kdsf}{Kisf} \qquad (10)$$

Where
K_{dsf}differential voltage sensor gain.

Aiming to abolish the variance dc link voltage, a PI+polecontroller was designed, which ensures a crossover frequencyof 0.5 Hz and a phase margin of 50.Frequency response includingthe open-loop transfer function ($OLTF_d$), controller transferfunction(H_{dsf}), and compensated loop transfer function($OLTF_d$+H_{dsf}).

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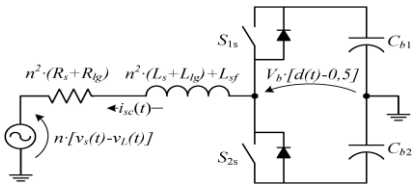

Fig.12. Single-phase equivalent circuit of SAF

The current control scheme contains of three equal current loops, except for the 120phase displacements from thereferences of each other. The current loops have a fast response to track the sinusoidal references, agreeing the decoupling analysis in relation to the voltage loop. The current loop transfer function is acquired through the analysis of the single-phase equivalent circuit shown in Fig. 12.

The voltage source represents the voltage on the coupling transformer. The dynamic model is obtained through the circuit analysis using average values associated to the switching period. Under these conditions, the voltages $V_s(t)$ and $V_L(t)$ are constants. Through small signal analysis and by using Laplace, thecurrent loop transfer function is given by

$$Gifs(s) = \frac{Isc(s)}{D(s)} = \frac{Vb}{sA1 + n^2 \cdot (Rs + Rlg)} \qquad (11)$$

Where

$$A1 = n^2 \cdot (Ls + Llg) + Lsf \qquad (12)$$

and

$L_s$series grid inductance;

R_sSeries grid resistance;

L_{lg}leakage inductance of the coupling transformer;

R_{lg}series resistance of the coupling transformer.

The open-loop transfer function ($OLTF_i$) is given by

$$OLTFi(s) = Gisf(s) \cdot Kpwmsf \cdot Kisf \qquad (13)$$

Where

K_{pwmsf}series filter pusle width modulation (PWM)Modulator gain.

The K_{pwmsf}gain is equal to the inverse peak value of thetriangular carrier.

Aiming to track the current reference, a PI+pole controller was designed, which ensures a crossover frequency of 5 kHz and a phase margin of 70.Frequency responsehaving the open-loop transfer function ($OLTF_i$), controller transfer function (H_{isf}), and compensated loop transfer function ($OLTF_i$+ H_{isf}).

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B. PAF Control

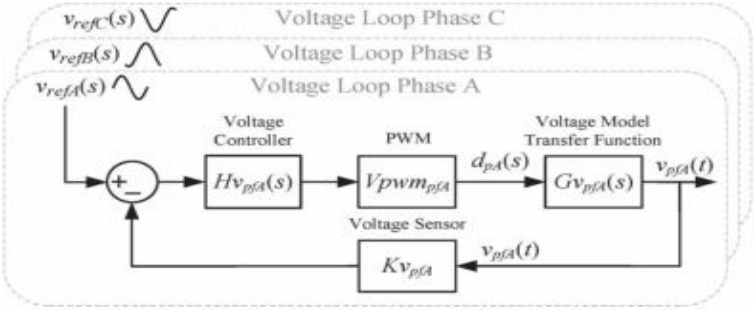

Fig.13. Control block diagram of the PAF voltage loop

Fig. 13 shows the control block diagram of the Parallel Active Filter (PAF) controller.The PAF control scheme is designed by three identical load voltage feedback loops, excluding for the 120^0 phase displacements from the references of each other. The voltage loops are liable for tracing the sinusoidal voltage reference for each load output phase in order to control the load voltages individually.

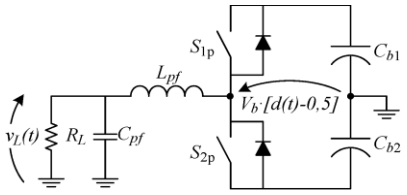

Fig.14. Single-phase equivalent circuit of PAF

The voltage loop transfer function is obtained through the analysis of the single-phase equivalent circuit shown in Fig. 14. The dynamic model is attained through the circuit analysis using average values related to the switching period. Through small signal analysis and by using Laplace,the voltage loop transfer function is given by

$$Gvpf(s) = \frac{Vb}{LpfCpf} \cdot \frac{1}{s^2 + s\left(\frac{1}{CpfRL}\right) + \frac{1}{LpfCpf}} \quad (14)$$

Where $G_{Vpf}(s)=V_L(s)/D(s)$.
The open-loop transfer function ($OLTF_{Vpf}$) is given by

$$OLTFv(s) = gvpf(s) \cdot KpwmpfKvpf \quad (15)$$

Where
K_{pwmpf}shunt filter PWM modulator gain.

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Aiming to trace the voltage reference, a proportional integral derivative (PID)+additional pole controller was designed, which make sure a crossover frequency of 4 kHz and a phase margin of 35. Frequency response containing the open-loop transfer function ($OLTF_{vpf}$), controller transfer function (H_{vpf}), and compensated loop transfer function ($OLTF_{vpf}$+ H_{vpf}).

In stable state, assuming a sinusoidal and balanced utility grid voltage and disregarding the dual UPQC losses, the apparent power of SAF S_{sf} and PAF S_{pf} regularized in relation to the apparent power of the load are given by (16) and (17).

$$\frac{|Ssf|}{|SL|} = \frac{\cos\varphi 1 \cdot \sqrt{(1-\frac{VL}{Vs})^2}}{\sqrt{1+TDHi^2}} \qquad (16)$$

$$\frac{|Spf|}{|SL|} = \sqrt{\frac{cos^2\varphi 1 \cdot \frac{VL}{VS} \cdot \left(\frac{VL}{VS}-2\right)}{1+TDHi^2}} + 1 \qquad (17)$$

Where cos(ϕ1) is the displacement factor and THDi is the total harmonic distortion of the output current.
These equations are attained through the analysis of the complex power of SAF $\dot{S}_{sf}$ and PAF $\dot{S}_{pf}$

$$\dot{S}sf = \left(\dot{V}s - \dot{V}L\right) \cdot \dot{I}^*s \qquad (18)$$

$$\dot{S}pf = SL - \dot{V}l \cdot \dot{I}^*s \qquad (19)$$

Increasing THD_i and decreasing cos(ϕ1) will decrease the ratio of $|S_{sf}/SL|$ and will increase the ratio of $|S_{pf}/SL|$.

This exploration indications that it is possible to design a SAF with power capacity lower than the minimal load power. By varying the transformers ratio, it is possible to use power switches with minor current capacity. On the other hand, PAF is constantly designed for nominal load power from the time when it has to process the total load reactive power.

VI. EXPERIMENTAL RESULTS

Experimental results for the proposed iUPQC. The passive filters were designed according to the specifications of Table I.

The Precharge system and the Precharge structure are an important and not trivial design step of the iUPQC due to the power flow characteristics of the system. During the start-up, the voltage supplied to the load cannot be distorted, and the iUPQC coupling in the circuit will not affect the load. The precharge method developed permits the start-up of the iUPQC without requirement of load power disconnection. The used precharge sequence is shown in Fig. 15. The precharge circuit has three contactors, namely, K_s,K_{p1},andK_{p2}, and one in-rush resistorR_{pc}. The switches $S_{w1}$and $S_{w2}$are used symbolically to showthe switching turn-on time. The $K_{p1}$and K_{p2}contactors are initially opened, while the $K_s$contactor is initially closed, and the switching of both active filters is primarily disabled.

The precharge sequence starts when the contactor K_{p1} is turned on, providing the charge of the dc link capacitors through antiparallel diodes present in the PAF power circuit. After 340 ms, the switching of the SAF $S_{w1}$is enabled, causing avoltage unbalance on the dc link during a short period of timedue to the stabilization time of the SAF unbalanced-voltage control loop. After 1 s, the K_s

Contactor is turned off, allowing the increase of the dc link voltage by SAF operation. After 10 ms, the switching of the PAF $S_{w2}$is enabled, starting theregulation of the load voltage. After 100 ms, the $K_{p2}$is turned on, finishing the precharge

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sequence. In order to match a harmonic distorted load current, a three phase rectifier with capacitive filter and two single-phase rectifiers with RL load connected to phases A and B, correspondingly, was used.

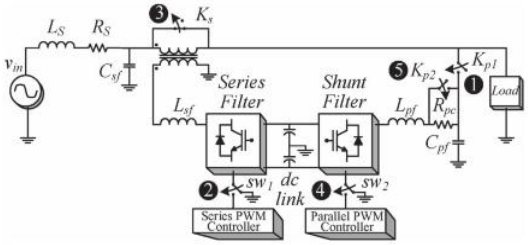

Fig.15. Precharge sequence of the iUPQC

In order to match a distorted grid voltage and to evaluate the harmonic compensation of the grid voltage, a FCATH 450-38-50 programmable ac power source manufactured by SUPPLIER Inc. was used. The power source supplies a threephase voltage source with 20% of the third harmonic in phaseA, 10% of the fifth harmonic in phase B, and 10% of the seventh harmonic in phase C.

Fig. 17 shows the currents through the PAF. The PAF indirectly supplies the load harmonic currents because the SAF only drains the fundamental current component from the source.

In a similar manner, Fig. 18 shows the voltages synthesized by the SAF. The SAF indirectly processes the harmonic grid voltages because the PAF imposes a synchronized sinusoidal voltage on the load.

In order to verify the dynamic response of the iUPQC, Fig. 20 shows the source and load voltages during a voltage interruption in phase A. Fig. 21 shows the source currents during a fault in phase A. It is possible to see that the source currents in the other phases have the amplitudes increased in order to keep the nominal power of the load.

Fig. 22 shows the load voltages and the load currentsduring a load step from 50% to 100%. The load voltages andthe load currents are shown in Fig. 23 during a load step from 100% to 50%.

Without Fault:

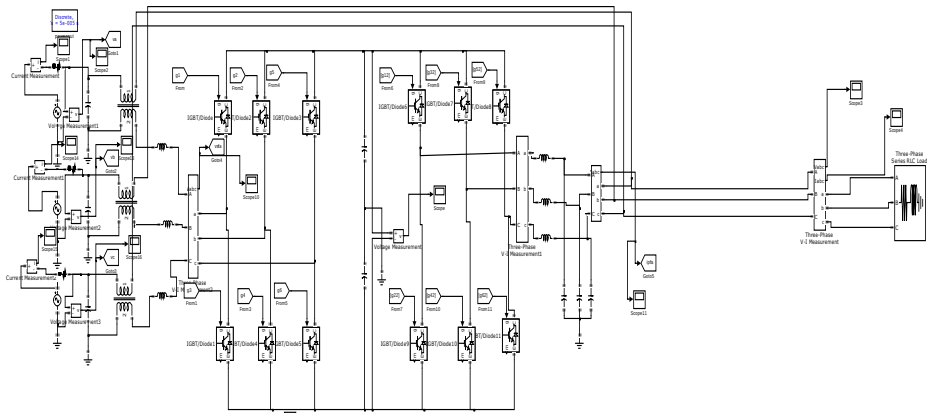

Fig.16. Simulink model without Fault

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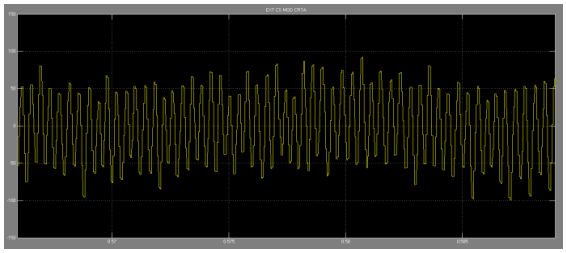
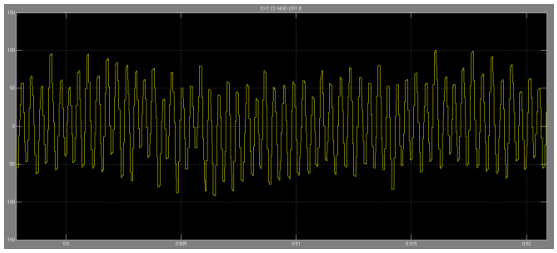
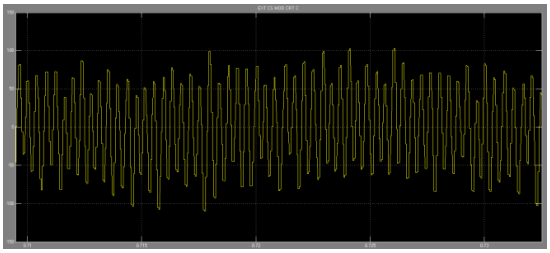


(a)

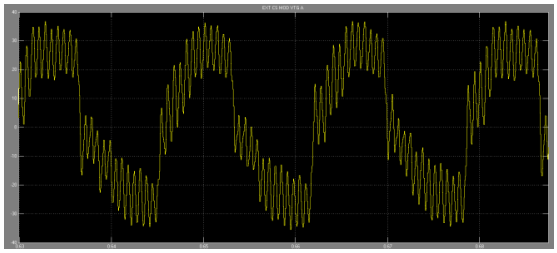


(b)

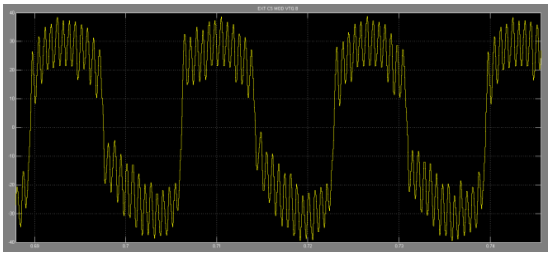


(c)

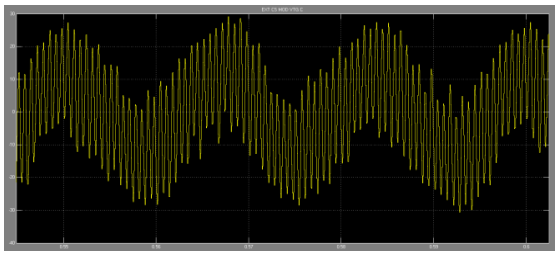
Fig.17. PAF currents, (a) Phase A, (b) Phase B, (c) Phase C



(a)



(b)



(c)

Fig.18. SAF voltages, (a) Phase A, (b) Phase B, (c) Phase C

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With Fault:

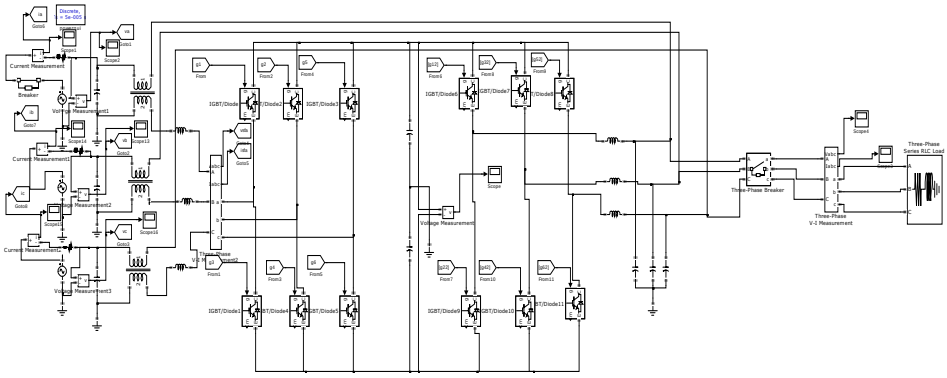
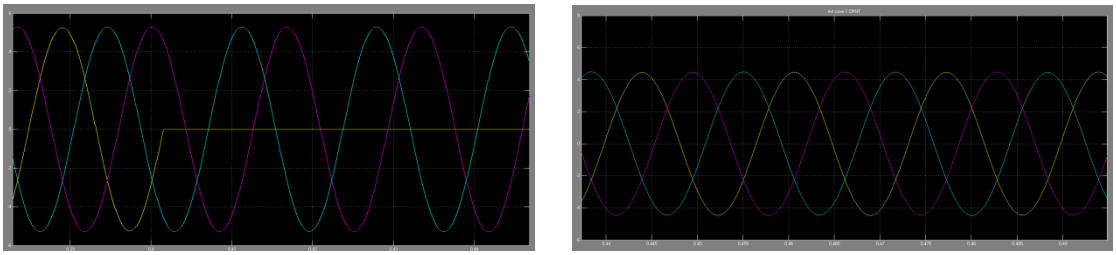
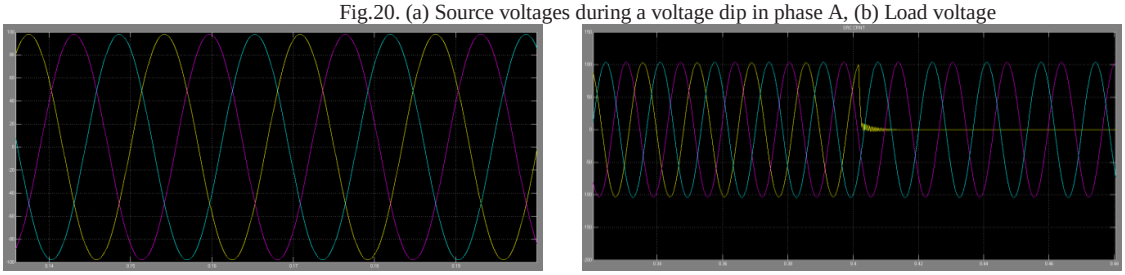


Fig.19. Simulink model with Fault at source in Phase A



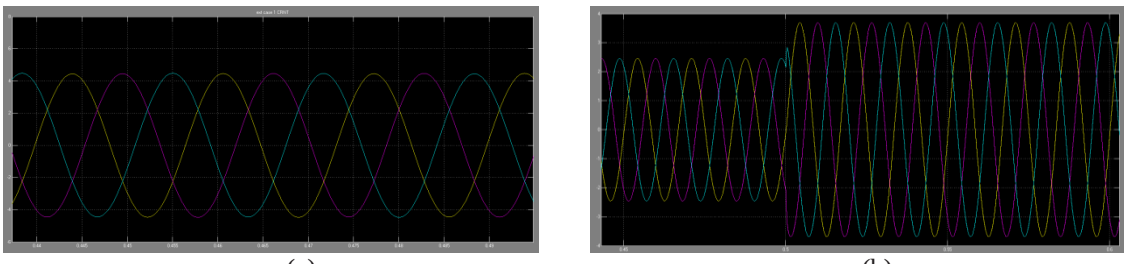
(a) (b)

Fig.20. (a) Source voltages during a voltage dip in phase A, (b) Load voltage



(a) (b)

Fig.21. (a) Load voltages, (b) Source currents during fault in phase A



(a) (b)

Fig.22. During a load step from 50% to 100%, (a) Load voltages and (b) Load currents

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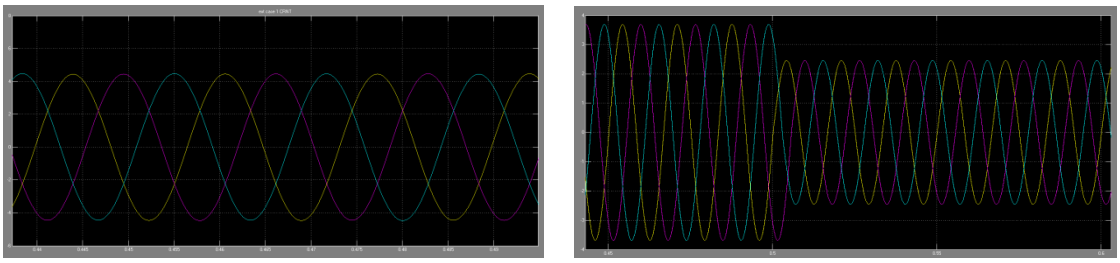

(a) (b)

Fig.23. During a load step from 100% to 50%, (a) Load voltage and (b) Load currents

VII.CONCLUSION

The results acquired through the iUPQC confirms that the recommendedABC reference mount control works very fine and thatit was capable to compensate the nonlinear load currents and similarlyensure the sinusoidal voltage for the load in all three phases. The control too had excessive performance during the load steps and voltage disorders at the source.

The main benefits of this proposed control in relativeto the other proposed systems were the consumption of sinusoidalreferences for both series and shunt active filtercontrols without the need for complex calculations or synchronizetransformations.

The iUPQC references do not require harmonic contents, and the only constraint is the synchronism with the grid voltage. Additional positive aspect of the iUPQC in low-voltage applications(Distribution system network) is the non-interference of the leakage impedance voltage of the series active filter (SAF) connection transformer in the load voltage compensation since the load voltage is directly controlled by the PAF. On the other hand, the leakage impedance affects in the current loop bandwidth, reducing its frequency response below distorted grid voltages.

The results confirm the proposed iUPQC control arrangement, evidencing that the power quality can be expressively better with a simple control method which uses only synchronized sinusoidal references.

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