

Analysis of THD in Asymmetrical Multilevel Inverter Using a Novel Topology

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ABSTRACT: Synchronous optimal pulse width modulation (SOP) allows low switching frequency modulation of construction electrical converter for medium-voltage high-power industrial ac drives while not compromising on total harmonic distortion (THD). The scope of experiment was to operate a 13-level cascade inverter of induction motor drive at an average device change frequency restricted to rated fundamental frequency by victimization SOP technique. To reduce the number of separate dc sources, a three-level diode clamped converter was used as a cell in the 13-level cascade inverter. Using SOP technique, optimal 13-level waveforms were obtained by offline optimization presumptuous steady-state operation of the induction machine. The switching angles for every semiconductor switch are then obtained from best 13-level waveforms primarily based on the criteria to attenuate the switching frequency similarly as unbalance in dc-link capacitor voltages.

KEYWORDS: Multilevel inverter, Medium-voltage ac drives, THD,

I. INTRODUCTION

Multilevel converters are a unit currently well-established and standard resolution for medium and high-voltage, high power applications. The advantages of structure converters over two-level converters are higher voltage operative capability with medium voltage semiconductor devices, improved output voltages with less harmonic distortion, reduced common-mode voltage, near curving input currents, smaller input and output filters, increased potency due to change of low change operation, reduced electromagnetic interference issues and doable fault-tolerant operation. In addition, the torque ripple also reduces as range of levels will increase in case of structure inverter fed ac drives. In high-power applications, the switching losses contribute to major portion of total device losses and thus low change frequency operation is necessary to realize higher potency. However, minimizing switching frequency will increase the harmonic distortion. Therefore, the challenge is to minimize the harmonic distortion while reducing the change frequency. Presently, the most popular topologies are unit diode-clamped or neutral-point-clamped (NPC), capacitor-clamped or flying capacitor (FC) and cascaded H-Bridge (CHB). The CHB topologies are most popular for higher-level converters due to demand of least number of elements and ease of management compared to other topologies. In addition, modularized circuit layout and packaging is also doable with CHB topology as a result of each level has similar structure. However, one major drawback of this topology is demand of multiple numbers of dc-sources, which is not possible in several applications. One of the methods for reducing the quantity of dc sources is to exchange H-Bridge cell with NPC or FC converters. However, an important issue with the topologies having agency or FC converters is voltage unbalance of dc-link capacitors that further adds to harmonic distortion of output voltage waveforms. An auxiliary capacitor-based balancing approach has been planned to equalize the dc-link capacitor voltages for agency five-level converter. Several low change frequency modulation techniques have been proposed for dynamical applications. A new modulation method for standard structure converter operative at elementary switching frequency whereas with success eliminating fifth harmonic.

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II. PROPOSED 13 LEVEL CASCADE INVERTER

Synchronous optimal pulse width modulation (SOP) technique is a rising technology to scale back switch frequency without compromising on harmonic distortion. Unlike SHE method, SOP takes into account all possible lower order harmonic components and determines switch angles thus as to keep the total harmonic distortion (THD) of output voltage or current waveforms within limits. SOP consists of Fourier series analysis of output voltage or current waveforms to model equations using switch angles as variables and their optimization to reduce distortion. All the calculations are computed offline assuming steady state operative conditions. SOP generates optimal switch pulse patterns of semiconductor devices in a multilevel electrical converter. Synchronized PWM is used in low-switching frequency applications where carrier signal at frequency (f_s) and sinusoidal management signal at frequency (f_l) are synchronized with every alternative, i.e., f_s / f_l is an integer in order to eliminate sub harmonic frequencies that square measure undesirable in many applications. Synchronized PWM results in lower number of switch instants per elementary amount and even a little variation in these switch angle values can have sizable influence on the harmonic distortion of output voltage. Optimization ways square measure urged to predetermine switching angles offline to scale back harmonic distortion. The recalculated switching angles square measure holds on and retrieved throughout real-time operation.

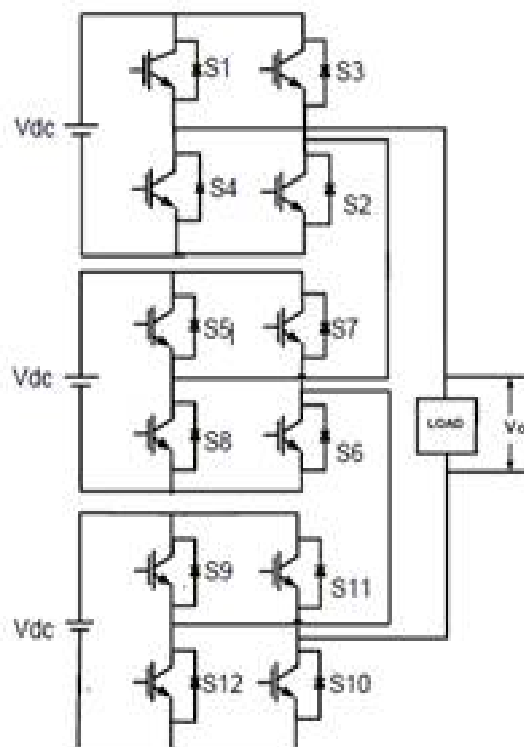


Figure 1: proposed circuit diagram

Asymmetrical dual bridge MLDCLI is one of the foremost necessary topology within the family of multilevel electrical converter (MLI). It requires least range of element compare to cascade H—bridge multilevel electrical converter and symmetrical twin bridge dc-link electrical converter. It consist two cell of H-bridge, first H-bridge work to increase the amount of the dc-link voltage and second H-bridge provide bi-directional power flow through the load. Each cell has designed to four switches Associate in Nursing an connected auxiliary switch is series with dc source, combination shunted through an opposed parallel diode. In this topology switch is used IGBT. DC voltage source area unit contemplate to be identical since all of them area unit batteries, solar cell, etc. it has two separated dc supply and totally

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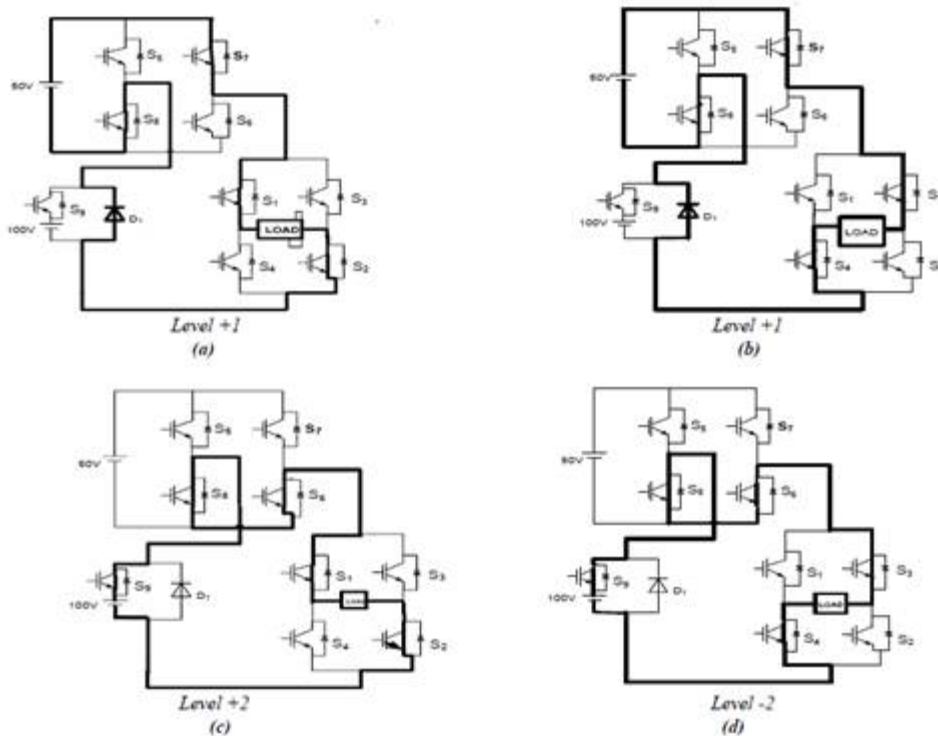
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different voltage. Asymmetrical seven level dual bridge dc-link multilevel electrical converter will operates in totally different modes witch area unit given. When switch S1, S2,S7 and S8 turned ON, an output voltage is V0 obtained with diode D1 operating as forward-bias. When switches S1, S2, S6, S8 and S9 are turned ON, an output voltage isV1 obtained with diode D1 working as reversed bias. When switch S1, S2, S7,S8 and S9 are turned ON, an output voltage is V0+V1 obtained with D1 operating as reversed-bias. When switch S1, S2, S6 and S8 are turned ON, an output voltage is “zero” obtained for “zero” level with diode D1 working as forward-bias. When switch S3, S4, S7andS8 are turned ON, an output voltage is -V0 obtained with diode D1 working as forward-bias. When switch S3, S4, S6,S8 and S9 are turned ON ,an output voltage is -V1 obtained with diode D1 operating as reversed-bias. When switch S3, S4, S7,S8 and S9 are turned ON, an output voltage is - (V0+V1) obtained with diode D1working as reversed-bias. For operation of seven level V0:V1= (50:100) V along with positive and negative cycle. The pair of switch S1 and S2 is used for positive half cycle, switch S3 and S2 is used for negative half cycle. If we take V0 = fifty = Vdc than V1= one hundred =2Vdc and V0+V1 = one hundred fifty =3Vdc.Cause of asymmetrical dc voltage source decreasing the switch losses, increasing the efficiency and eliminating the resultant effects of de-rating. Asymmetrical dual bridge dc-link structure electrical converter will be expressed victimization the relation $2(2n+1)+1$,where n is the range of voltage supply excluding V0.

III.OPERATING MODES

For convenience to explain the in operation modes for varied levels, the dc link structure are represented by mounted dc supply in the coming diagrams. The operation for each story of a 13 level inverter with V0:V1 = (50:100) V on with positive and negative [*fr1] cycles is explained pictorially through +3 level to -3 level. It will be seen from Figure nine. The try S1–S2 or pair S3–S4 in the H-bridge alternately is required to require extracting the primary level of the output voltage and goes through a similar sequence for other levels. The form of the output voltage shown in Figure ten clearly indicates the devices that conduct for the various levels of the output voltage.



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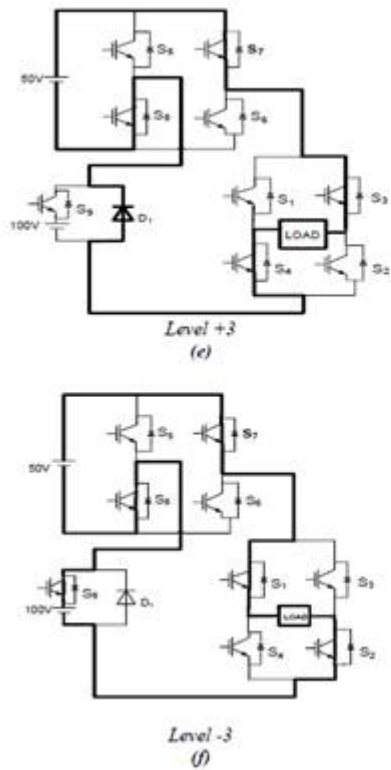


Figure 2 a,b,c,d,e,f: operating modes of proposed multilevel converter

IV. CONTROL AND MODULATION STRATEGIES

Phase opposition disposition pulse width modulation (POD PWM):-In POD PWM strategy all (N-1) carriers signal are same part to every different higher than the zero-axis with frequency and amplitude but carrier wave reduced than zero-axis is 180° out of phase with higher than zero-axis carrier wave shape.

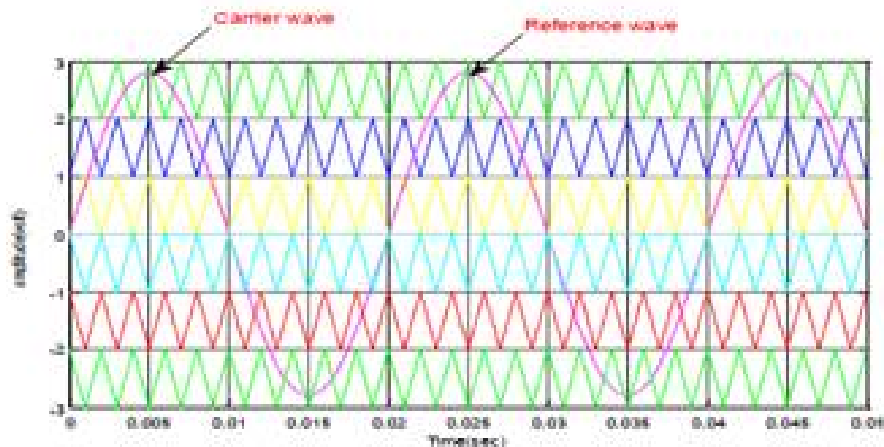


Figure 3: phase modulation techniques

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V.SIMULATION ANALYSIS AND RESULT

The proposed topology model of single-phase MLI. Table II shows its switching schemes and table I Comparison in terms of power components used for completely different level. The simulation parameters are as following $R=$ ten ohm, $L=$ 0.01mH and DC source V1 and V2 is 50V, 100V, respectively, carrier signal frequency is 4 kHz; doctor's degree area unit shown in Figure12.The harmonic spectrum is carried out by using the FFT analysis in MATLAB/simulink.

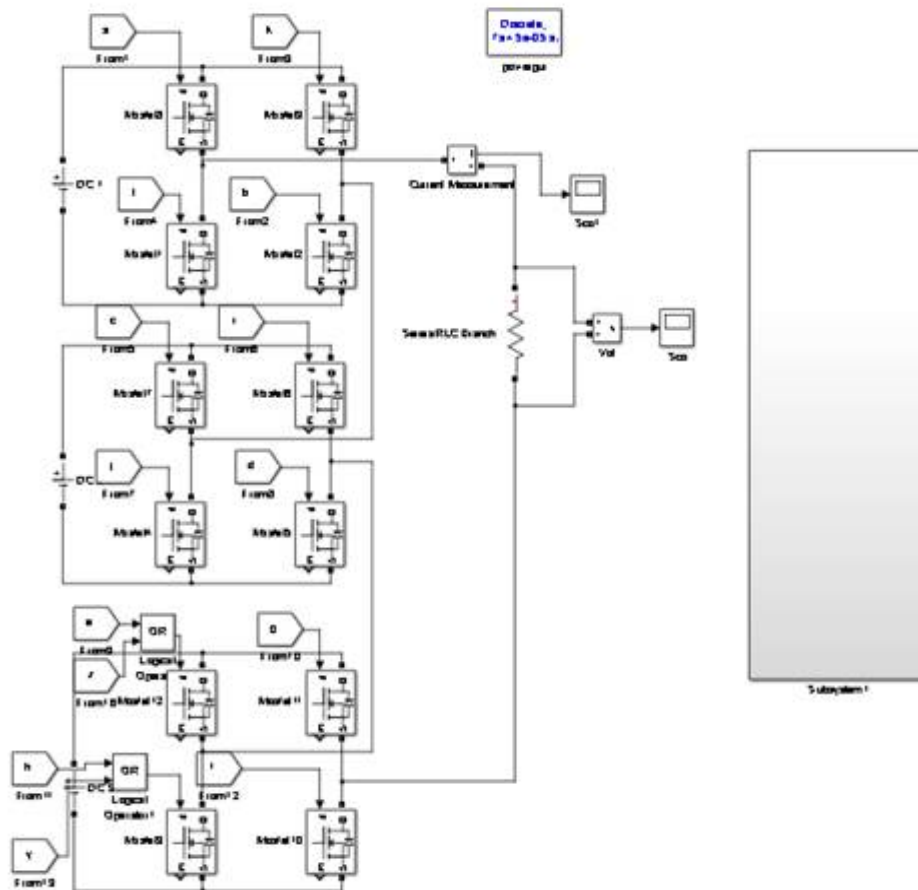


Figure 4:simulation circuit of proposed multilevel inverter

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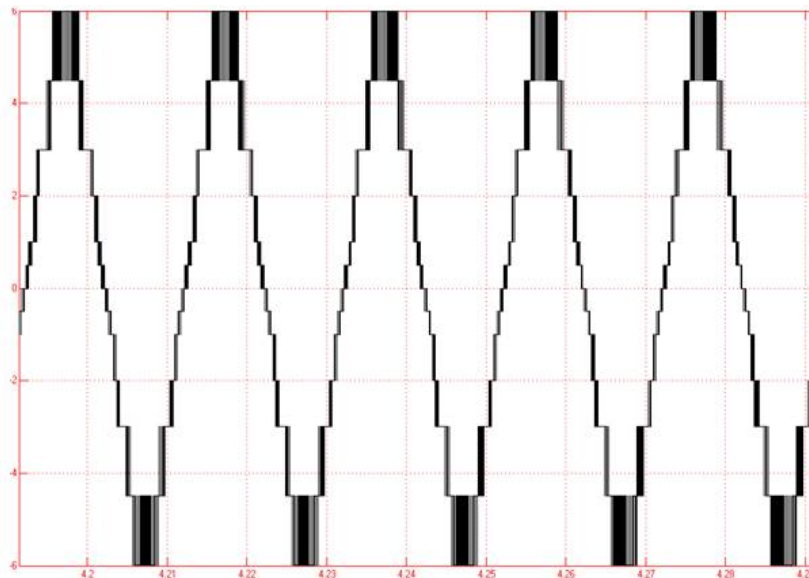


Figure 5: 13 level output waveform

VI.PROTOTYPE MODEL

The proposed technique has been implemented for controlling a 13-level cascade inverter feeding a 1.5-kW induction motor. One more necessary criterion whereas distribution changes angles is to attenuate the most device change frequency of every semiconductor device. the heartbeat range N determines the quantity of change transitions of the nine-level potential and every transition is being caused by a transition in one among four three level NPC inverters. The entire range of change transitions in turn decides the change frequency of conductor, so the pulse range ought to be divided equally among all the four three-level inverters.

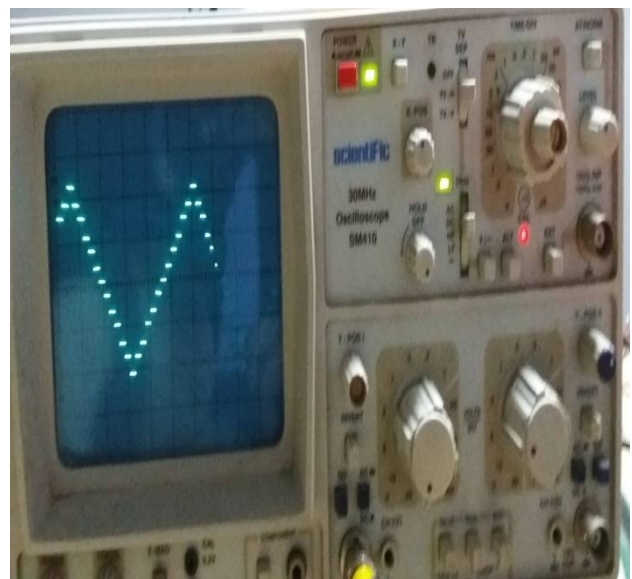
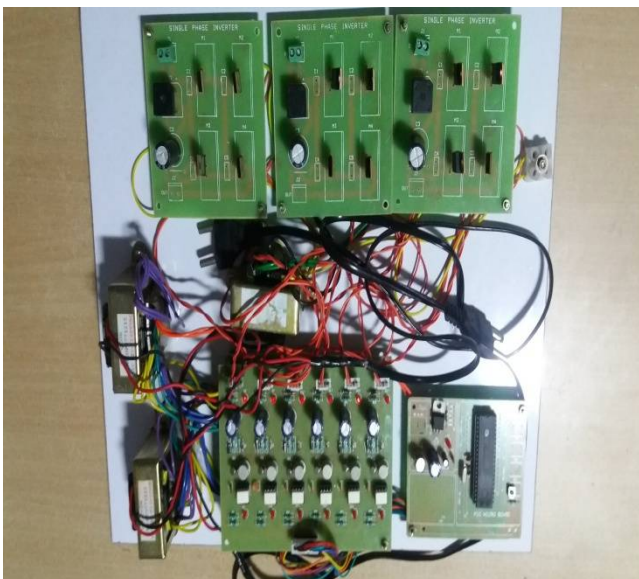


Figure 6a:hardware image

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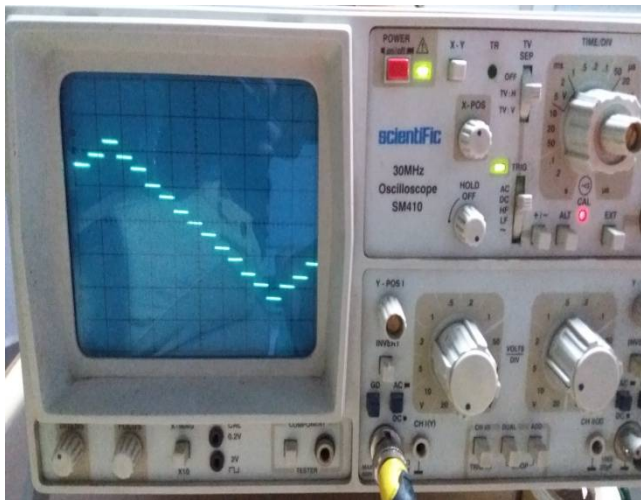


Figure 6c: 13 level sine wave

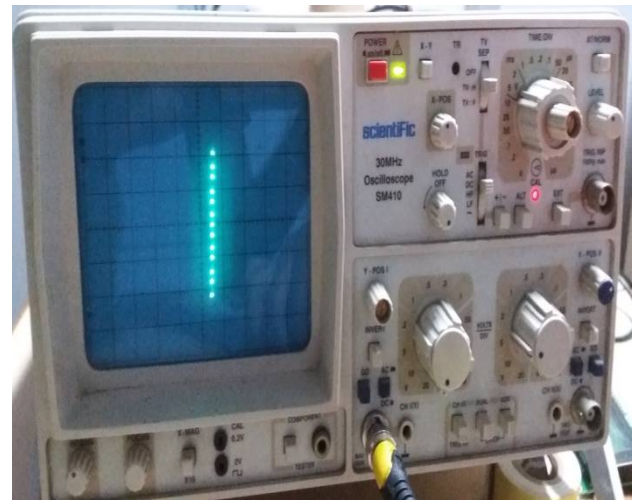


Figure 6d: 13 level

VII.CONCLUSION

An MLDCI structure fittingly designed mistreatment a twin bridge configuration has been offered with a read to reduce the quantity of power switches to synthesize Associate in nursing increasing level of output voltages. The topology has been prepared mistreatment Associate in nursing acceptable selection of voltage ratios between the constituent parts in the module. The acquirement of the desired results has been found to feature a feather to vindicate the technology revolution in progress. The higher quality of output voltage which will be taken out using the new structure can go a long approach in insinuating bigger horizons of power converter interfaces in the machine-driven world.

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