

An Efficient Carry Skip Adder Design for Fastest Addition

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ABSTRACT: Adders are the basic unit in arithmetic and logic units (ALUs). So increasing their speed and reducing their energy/power consumption is essential to increase the speed and reduce the power consumption of processors. In this paper, we present a carry skip adder structure (CSKA) with higher speed yet lower energy consumption. In the conventional CSKA (Conv-CSKA) the skip logic is using multiplexers. But in the proposed CSKA structure use AND-OR-Inverter (AOI) and OR-AND Inverter (OAI) compound logic gates for the skip logic. In addition, the proposed CSKA uses Common Boolean Logic (CBL) based half adder and full adder. The structure may be realized with both fixed stage size (FSS) and variable stage size (VSS). Whereas the variable stage size CSKA is more efficient in terms of power delay product (PDP). Also propose a hybrid variable latency extension of proposed CSKA structure.

KEYWORDS: Carry skip adder (CSKA), AND-OR-Inverter (AOI), OR-AND-Inverter (OAI), skip logic, power delay product (PDP), hybrid variable latency adders.

I. INTRODUCTION

Adders are the most essential logic block with in a digital system such as arithmetic and logic units (ALUs) [1]. In addition, adders are used in multipliers, dividers, and memory addressing units. Therefore, increasing the performance of the adders in terms of speed and power helps to improve the performance of the entire system. Extensive researches are continuous to be focused on to improve the power and delay performance of the adders. This is because adders are the critical elements in most circuits including digital signal processors (DSP) and microprocessors data path units. But it is very difficult to achieve lower delay at low power/energy consumptions.

There are many adder families with different speed, area usage and power consumptions. The different adder families are ripple carry adder (RCA), carry select adder (CSLA), carry skip adder (CSKA), and parallel prefix adders (PPAs). The RCA is constructed by simply cascading full adders (FAs) in series. Each FA is used to add two binary digits at any stage of the RCA. The carry output of one stage is fed to the carry input of the next stage directly. RCA is the simplest parallel adder with small area and power consumption. The main disadvantage of RCA is the worst critical path delay. The CSLA compute the alternative results in parallel and select the correct result using hierarchical techniques. In CSLA the sum and carry outputs are calculated for both carry input zero and one. After delivering the correct carry input multiplexer is used to choose desired output with the correct carry input as select line for the multiplexer. CSLA has higher speed than RCA with the cost of larger power consumption and area usage. The PPAs which are derived from carry look ahead adders are more flexible and used to speed up the binary addition [2]. There are different types of PPAs such as Brent-Kung adder, Kogge-Stone adder, Sklansky adder, Han-Carlson adder etc. The structural complexity of these adders is limiting their frequent usage.

The CSKA consist of simple RCA with multiplexer skip logic [3]. Because of this simplest structure the CSKA has lower power consumption and area usage compared with other adder families. The critical path delay of the CSKA is smaller than the RCA with similar area and power consumption. The power delay product (PDP) of the CSKA is

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equivalent to the CSLA and PPA structures [4]. But the CSKA has comparatively lower speed and hence it is not used for high speed applications.

In this paper, proposes attractive CSKA structures that considerably lower PDP than the Conventional and the existing concatenation incrementation CSKA. The proposed structure increases the speed of the CSKA by maintaining low power consumption and the area usage characteristics of the CSKA. Finally, proposes a hybrid variable latency CSKA structure. This structure also has the lower PDP than the existing one.

The remaining of this paper is organized as follows. Section II discusses the existing concatenation incrementation CSKA (CI-CSKA). In Section III, describes the proposed CSKA structure and its advantages over the conventional and existing one. Section IV discusses the hybrid variable latency adder structure. Evaluating the performance of the proposed structure with the Conventional and existing CSKA in Section V. In Section VI shown the simulation results and finally conclusions are listed in Section VI.

II. CONCATENATION INCREMENTATION CARRY SKIP ADDER

Three-stage CI-CSKA structure is shown in Fig.1. In the CI-CSKA structure shown, the multiplexer skip logic in Conv-CSKA is replaced with AND-OR-Inverter (AOI) and OR-AND-Inverter (OAI) compound gates as skip logic. The structure uses alternate AOI and OAI skip logic. This is because, the output carry generated from AOI compound gate skip logic are in complemented form to utilize the carry output directly to the next stage use OAI compound gate skip logic. This avoid additional inverter gate in the critical path. The other major difference in the CI-CSKA structure is that, the input carry to the RCA block expect the first block set to zero. Only carry input C_i is given to the first RCA block. Hence each stage calculates the intermediate result simultaneously. When the first block calculate the sum bits with input carry C_i the other RCA block calculate the intermediate results and the carry output of corresponding RCA block.

The intermediate results obtained are fed to the corresponding incrementation block, as shown in Fig.1. The internal structure of incrementation block is shown in Fig.2. The incrementation block shown consist chain of half adders (HAs). The skip logic determine the carry output, $C_{o,i}$ by taking the intermediate result of the stage, carry output of previous stage and the carry output of the RCA block in the stage.

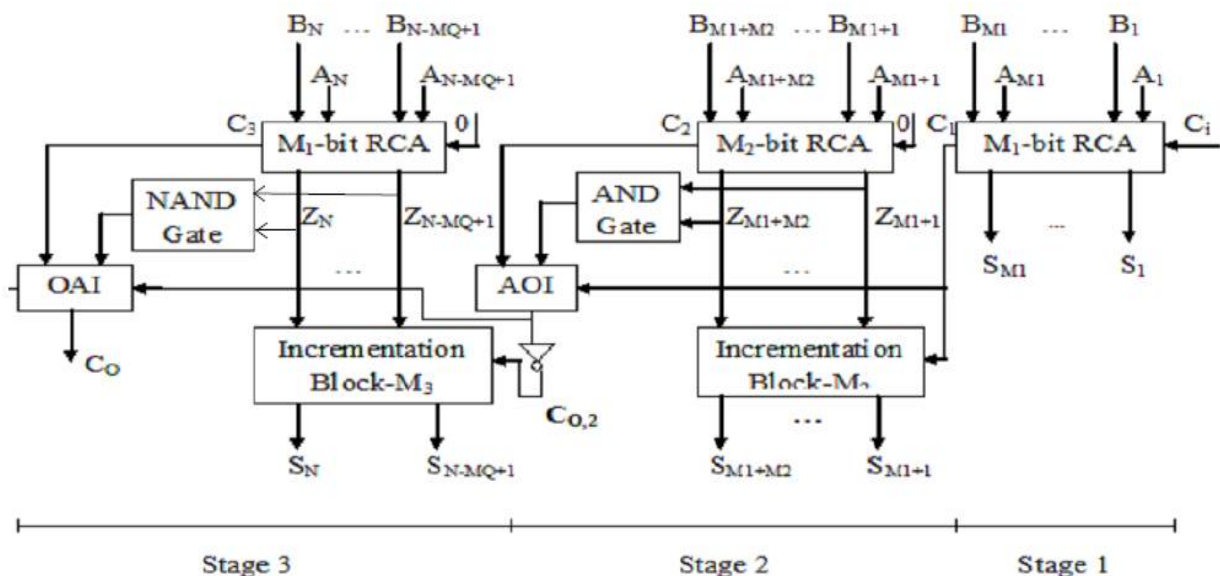


Fig.1. Three-stage CI-CSKA structure

The existing CI-CSKA structure considerably increases the speed compared with the conventional one. But this structure causes increase the power. The PDP of the CI-CSKA structure is much lower than the Conventional adder.

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The CI-CSKA structure is implemented for both FSS and VSS. Similar to Conv-CSKA the proposed CSKA VSS structure has the lesser delay compared to the FSS [5]. The stage sizes for the Conv-CSKA and CI-CSKA for VSS design as [3].

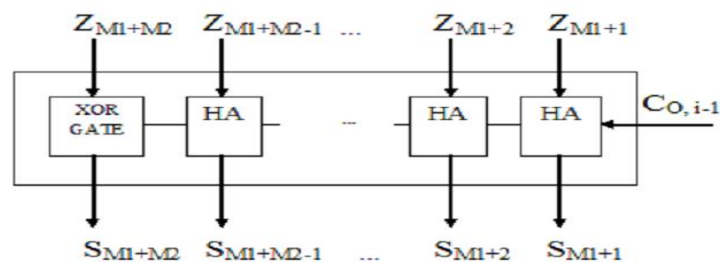


Fig.2. Internal structure of the incrementation block

III. PROPOSED CONCATENATION INCREMENTATION CARRY SKIP ADDER

The proposed CI-CSKA use Common Boolean Logic (CBL) based half adders (HAs) and full adder (FAs). In the existing CI-CSKA structure has more power consumption than the Conv-CSKA. The proposed structure decrease the power compared with the existing one. The proposed structure has power near to the conventional one. The proposed CI-CSKA has higher speed than the existing CI-CSKA. Which means the PDP of the proposed CI-CSKA is much less than the existing one. The CBL HAs and FAs are designed by analysing the truth table. The CBL based HA is shown in fig.3. For the case of HAs when input $B=0$ the sum output $S=A$, carry output $C_0=0$ and $B=1$, $S= \sim A$, $C_0=A$ this concept is used to design CBL HA [6]. The CBL HA use two 2:1 multiplexer one for the sum and the other for the carry output both with input B as select line as shown in fig.3.

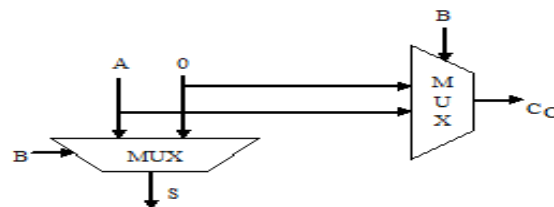


Fig.3. Common Boolean Logic based half adder

The CBL based FA is shown in fig.4. For the case of FAs when the carry input $C_i=0$ the sum output $S=A \oplus B$, carry output $C_0=A \& B$ and $C_i=1$, $S= \sim (A \oplus B)$, $C_0=A+B$ this concept is used to design the CBL FA [6]. The CBL FA is also designed using 2:1 multiplexer with carry input C_i as select input as shown in the fig.4. The proposed CI-CSKA structure is implemented for both FSS and VSS.

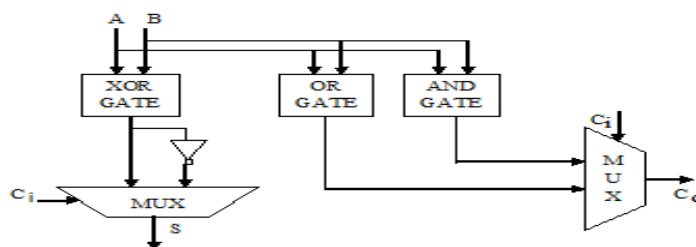


Fig.4. Common Boolean Logic based full adder

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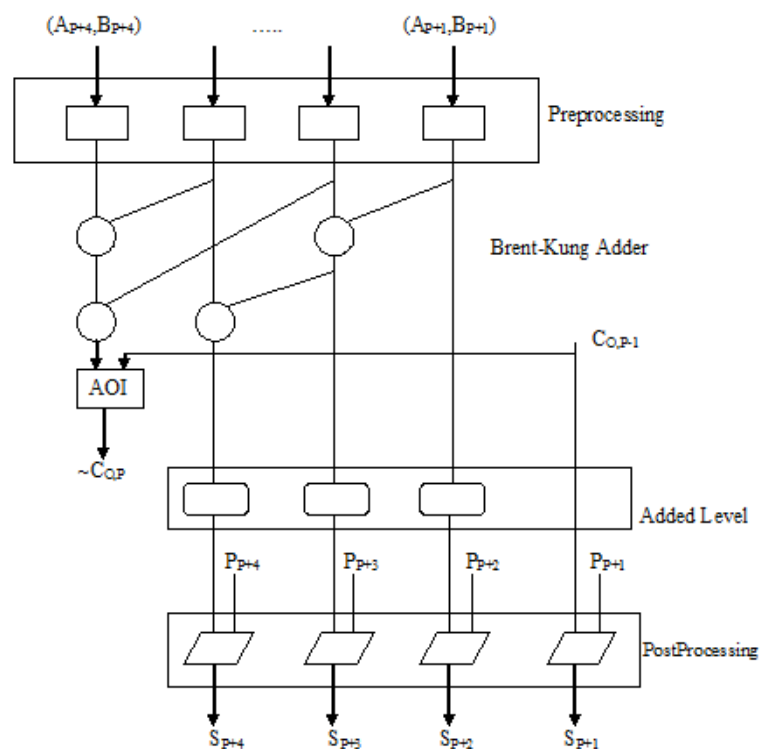
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IV. HYBRID VARIABLE LATENCY CARRY SKIP ADDER

The hybrid variable latency adder combines the PPA with the CI-CSKA hence the name hybrid [3]. The structure of hybrid latency CSKA is same as the CI-CSKA structure shown in Fig.1. with only one difference the nucleus stage is using PPA. This adder has variable latency path [7], it requires only one clock cycle when the off critical path is activated and two clock cycles when critical path is activated to complete the addition process. Predictor circuit is used to determine the number of clock cycles required for the addition [8]. In the proposed hybrid variable latency CSKA the predictor output is the propagate signal P_{MP+1} of PPA.

There are three main stages for the PPA, preprocessing stage parallel prefix network stage and finally postprocessing stage [10]. The preprocessing stage compute the generate (G_i) and propagate (P_i) next stage is the parallel prefix network. This stage calculate, the larger carry $G_{4:1}$ of the prefix network and $P_{4:1}$ which is the product of all propagate signals of the inputs. The $P_{4:1}$ propagate signal is used as the predictor signal. If $P_{4:1}$ is one, carry $C_{O,p-1}$ should skip this stage predicting that some critical path are activated. When $P_{4:1}$ is zero, $C_{O,p}$ is equal to $G_{4:1}$ without activating the critical path. Before the postprocessing stage, intermediate carries which are the functions of $C_{O, p-1}$ and intermediate signals are computed. Finally, in the postprocessing stage the outputs of the stage are calculated.

The nucleus stage of the existing and proposed hybrid variable latency carry skip adder is shown in Fig.5. In the existing hybrid variable latency CSKA uses Brent-Kung parallel prefix network. The Brent Kung adder require less area compared with other PPAs with less wiring congetion. Also it has less wiring capacitance, and simple and regular layout [9]. But the disadvantage is higher delay. In the proposed structure uses Kogge-Stone parallel prefix network. Kogge-Stone adder is the fastest adder in the PPA family with increase in area. The PDP of proposed hybrid adder is much smaller than the existing one.

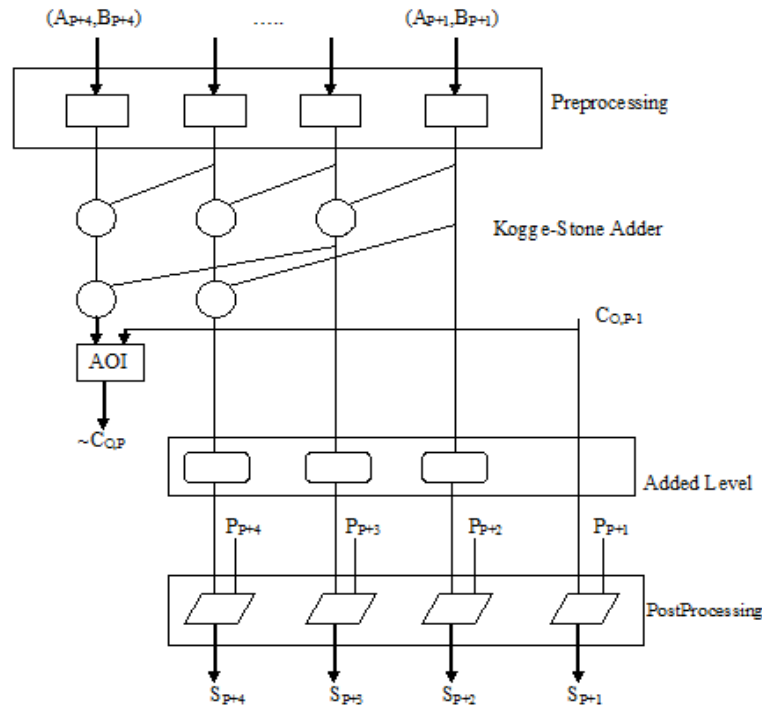


(a)

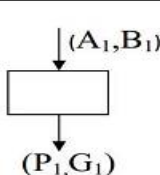
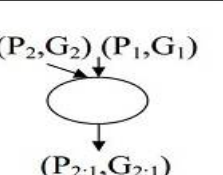
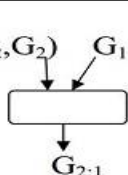
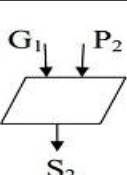
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(b)

Block Details			
			
$P_1 = A_1 \oplus B_1$ $G_1 = A_1 \cdot B_1$	$P_{2:1} = P_2 \cdot P_1$ $G_{2:1} = G_2 + P_2 \cdot G_1$	$G_{2:1} = G_2 + P_2 \cdot G_1$	$S_2 = G_1 \oplus P_2$

(c)

Fig.5. (a) Existing Brent-Kung based nucleus stage of hybrid variable latency CSKA structure (b) Proposed Kogge-Sone based nucleus stage of hybrid variable latency CSKA structure (c) Block details

V. PERFORMANCE ANALYSIS

Analysing the performance of the Conv-CSKA, CI-CSKA, proposed CI-CSKA in terms of power, delay and PDP are shown in the table. The CI-CSKA FSS and VSS structures have lower delay than the conventional FSS and VSS structures with slight increase in the power. The PDP of CI-CSKA is much lower than the Conv-CSKA for both cases. The proposed CI-CSKA structure reduces the power compared with the existing one with increase in the speed. The PDP is also smaller than the existing CI-CSKA. Finally, the existing hybrid variable latency CSKA has lower power consumption than other structures with delay similar to the existing CI-CSKA FSS structure. The proposed hybrid variable latency CSKA further increases the speed with slight increase in the power. The PDP of proposed hybrid variable latency carry skip adder is less than the existing structure

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TABLE I. ADDER COMPARISON

Adder Structure	Delay(ns)	Power(mw)	PDP
FSS-Conv-CSKA	63.711	163	10384.893
FSS-CI-CSKA	39.150	168	6577.2
FSS-Proposed CI-CSKA	38.043	165	6277.095
VSS-Conv-CSKA	53.463	160	8554.08
VSS-CI-CSKA	36.102	168	6065.136
VSS-Proposed CI-CSKA	35.715	165	5892.975
Hybrid CSKA	40.020	167	6683.34
Proposed Hybrid CSKA	38.950	168	6543.6

VI. SIMULATION RESULTS

Simulation results of Conv-CSKA, proposed CI-CSKA and proposed hybrid latency CSKA are shown below. Simulations are done using Xilinx ISE 9.1i using verilog code. The operating frequencies of all the structures are chosen to 100HZ. The p₇ output in the hybrid variable latency CSKA indicates the number of clock cycles required to the addition operation.

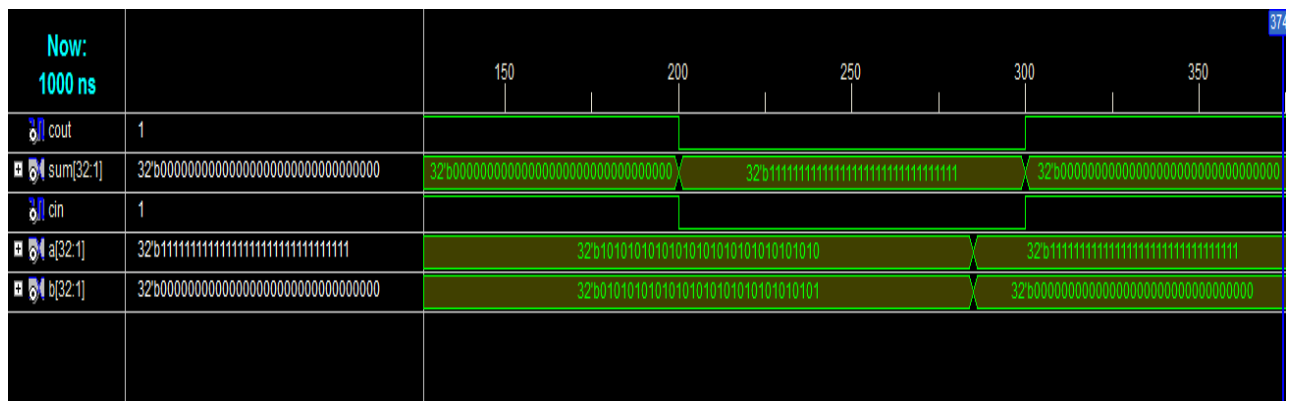


Fig.6. Simulation result of Conv-CSKA

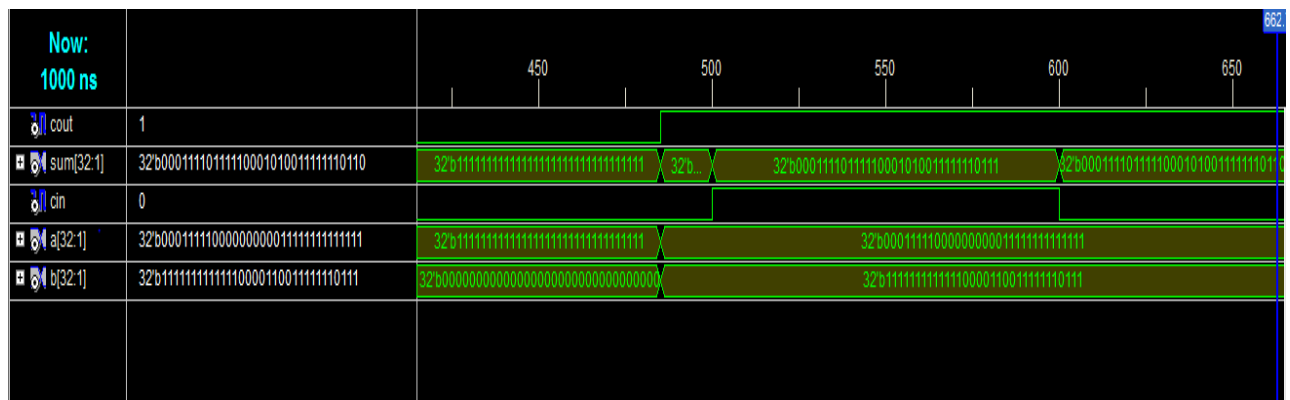


Fig.7. Simulation result of proposed CI-CSKA

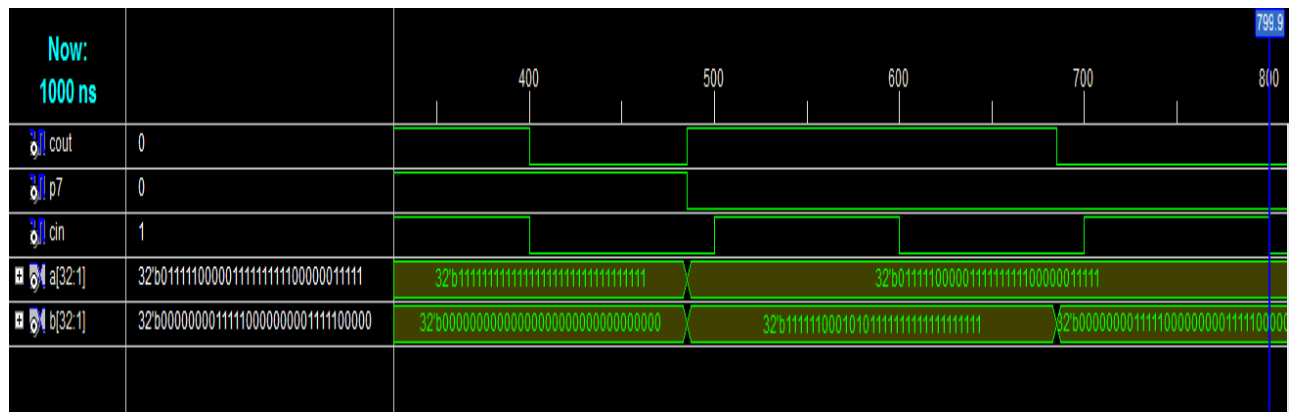


Fig.8. Simulation result of hybrid variable latency CSKA

VII. CONCLUSION

This paper presents, a static CMOS CSKA with higher speed with lower power/energy consumption. The Conv-CSKA has small area usage and low power consumption compared with other parallel adder the only disadvantage is the lower speed hence it is not used for high speed applications. The CI-CSKA structure overcomes this disadvantage with higher speed. In addition, this structure has lower PDP. This structure has the disadvantage of higher power than the Conv-CSKA. The proposed CSKA structure reduces the power of existing system with power similar to Conv-CSKA. The proposed structure also increases the speed and the PDP of proposed CI-CSKA is lower than the existing one. The existing hybrid variable latency CSKA has power lower than other existing structure with slight decrease in the speed. The proposed hybrid variable latency CSKA increases the speed with a small increase in the power. The PDP of the proposed hybrid variable CSKA is lower than the existing hybrid structure.

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