

Design of CMOS 8-bit Comparator with Efficient VLSI Design Constraints

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ABSTRACT: We present a Comparator with less Transistor count and low power by having less Active number of Transistors. There are less number of Transistors in series such that by default Speed can be better. Total number of transistor count for N-bit is $(N-1)*20+6+6+4$. The idea is to provide new way of Circuit Designing in Transistor level by without even forming the equations. CMOS logic style which is being dominant in Industry is being considered for designing the Circuit which has the Prime Disadvantage of occupying more Area and this corresponds to number of Transistors at the Circuit level. Total number of cells required for the Design are also very less such that it will be helpful for the Layout, though a manual or Automated Layout. Circuit which we have designed also has uniform structure. Circuit was designed by using S-EDIT tool for Schematic entry and T-SPICE for Simulation of TANNER EDA tool.

KEYWORDS: 10T BlockEven , 10T BlockOdd, Comparator, CMOS.

I. INTRODUCTION

Low density parity check (Ldpc) was designed by gallager in 1962[1]. Implementation of ldpc decoder has efficient Speed constraint but other constraints of VLSI. comparator is important module in decoder. C-H HUANG developed priority encoder based on logic and module which has efficient Speed and power but at expense of Area[2]. S-W CHENG employed Mux based Design and their design is designed at gate level and total number of levels are less which will improve the Performance [3]. J-Y KIM and H-J YOO proposed a design used dynamic logic which can lead to lack of full-output voltage swing and this might be inefficient when the Technology is scaled down[4].

Add-Compare-Select block will be performing three different operations like Addition, Comparison and Multiplexing, here asynchronous logic is being employed without under the control of the clock[5]. Static Cmos will be having power rails and thus they have good noise immunity when compared to Dynamic logic[6]. If we want to design High performance circuit there should be more Parallelism[7].

Any expression can be directly translated into equivalent transistor level CMOS Circuit [8]. Geetanjali Sharma comparator is based on gate level circuit designing which might not give the maximum [9]. Saleh Abdel Hafeez proposed high speed comparator at expense of Area but used transmission gates logic which does not have any power rails and leads to a less noise immunity[10].

VLSI has a trade-off among the design constraints like Area, Power and Speed so any two constraints in general will be kept in mind and making sure that low priority constraint is not that neglected. Here we are not interested in universal gate based design instead we want to propose design which can be extendable to N-bit.

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II. RELATED WORK

Comparator with High Speed as well as less Power consumption but More Area was being proposed they have less number of levels lead to high Speed and when Output is known, portion of the Circuit which is not needed to calculate the output will be deactivated leading to less Switching activity which in turn less Power consumption their design is Static and they have used basic CMOS cells and their Maximum Fan-in is 5, Maximum Fan-out is 4 and Maximum Transistor count is 20 and we can identify whether $A > B$ or $A < B$ or $A = B$ and total Active number of Transistors for 64-bit is 944 [10].

Comparator with High Speed as well as less Area was being proposed they have less number of levels lead to high Speed, design required basic logic gates and Multiplexers and their Maximum Fan-in is 3, Maximum Fan-out is 2 and Maximum Transistor count is 12 and we can identify whether $A \geq B$ or $A < B$ and total Active number of Transistors for 64-bit is 778 [03].

Proposed Comparator has Low Area and design is Static and we have used our defined CMOS cells and their Maximum Fan-in is 4, Maximum Fan-out is 2 and Maximum Transistor count is 10 and we can identify whether $A > B$ or $A < B$ or $A = B$ and total Active number of Transistors for 64-bit is 638, Obviously less number of Active Transistors means less will be the Power Consumption .

III. MAGNITUDE COMPARATOR

Comparator is going to compare 8 bits of A (A_7 to A_0) and 8 bits of B (B_7 to B_0) and decides whether $ALTB(A < B)$ or $AGTB(A > B)$ or $AEB(A = B)$. Conventional Digital CMOS cells are not utilized in the Design .we need to know what are all the conditions for $ALTB(A < B)$ to become true, if ($A_7 < B_7$) then $ALTB(A < B)$ should be true and 6T Block which has one not gate and one two input nand gate has been designed and nand gate has one output.

Now let us see the second condition that is if ($A_6 < B_6$) and if ($A_7 > B_7$) is false then $ALTB(A < B)$ should be true, so we have designed another 6T Block for knowing the status of ($A_7 > B_7$) and 10T BlockEven for ($A < B$) and this block has one output. Now the first condition for ($A > B$) which is ($A_7 > B_7$) already available and the second condition that is if ($A_6 > B_6$) and if ($A_7 < B_7$) is false and we have this status from 6T Block then $AGTB(A > B)$ should be true, and 10T BlockEven for ($A > B$) has been designed and this block has one output.

Now let us see the third condition for $ALTB(A < B)$ that is if ($A_5 < B_5$) and if 2-bit Greater then output is false then $ALTB(A < B)$ should be true and for this 10T BlockOdd is designed. Now let us see the third condition for $AGTB(A > B)$ that is if ($A_5 > B_5$) and if 2-bit less then output is false then $AGTB(A > B)$ should be true and for this 10T BlockOdd is designed.

Now let us see the fourth condition that is if ($A_4 < B_4$) and if 3-bit greater then output is false then $ALTB(A < B)$ should be true, so we have designed another 10T BlockEven for this requirement. Now let us see the fourth condition that is if ($A_4 > B_4$) and if 3-bit less then output is false then $AGTB(A > B)$ should be true, so we have designed another 10T BlockEven for this requirement

Now let us see the fifth condition that is if ($A_3 < B_3$) and if 4-bit greater then output is false then $ALTB(A < B)$ should be true, so we have designed another 10T BlockOdd for this requirement. Now let us see the fifth condition that is if ($A_3 > B_3$) and if 4-bit less then output is false then $AGTB(A > B)$ should be true, so we have designed another 10T BlockOdd for this requirement

Now let us see the sixth condition that is if ($A_2 < B_2$) and if 5-bit greater then output is false then $ALTB(A < B)$ should be true, so we have designed another 10T BlockEven for this requirement. Now let us see the sixth condition that is if

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($A_2 > B_2$) and if 5-bit less then output is false then $AGTB(A > B)$ should be true, so we have designed another 10T BlockEven for this requirement

Now let us see the seventh condition that is if ($A_1 < B_1$) and if 6-bit greater then output is false then $ALTB(A < B)$ should be true, so we have designed another 10T BlockOdd for this requirement. Now let us see the seventh condition that is if ($A_1 > B_1$) and if 6-bit less then output is false then $AGTB(A > B)$ should be true, so we have designed another 10T BlockOdd for this requirement

Now let us see the last condition that is if ($A_0 < B_0$) and if 7-bit greater then output is false then $ALTB(A < B)$ should be true, so we have designed another 10T BlockEven for this requirement. Now let us see the last condition that is if ($A_0 > B_0$) and if 7-bit less then output is false then $AGTB(A > B)$ should be true, so we have designed another 10T BlockEven for this requirement.

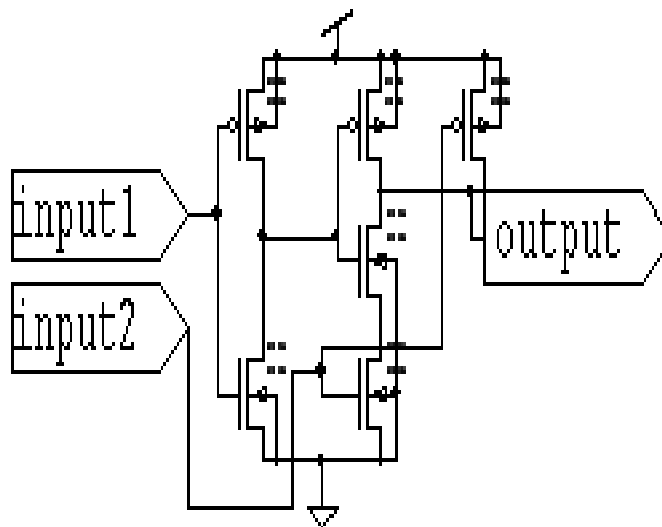


Fig.1 6TBlock

Fig1 is an 6Transistor Block Circuit which is required to know the less then($<$) and greater then($>$) Status at MSB stage, this Status is required at MSB-1 Stage of $ALB(A < B)$ and $AGB(A > B)$ and it requires 6 number of Transistors and this is one of the conditions and in fact the first condition which implies that when $A_7 > B_7$ no need to know the values of remaining inputs $AGB(A > B)$ Output will be True and same is the case for $A_7 < B_7$.

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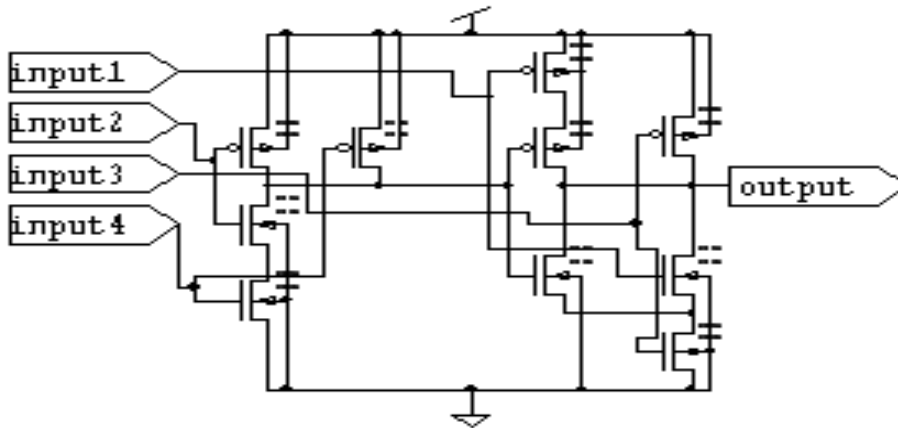


Fig.2 10TBlock(Even) Circuit

Fig2 is an 10Transistor BlockEven Circuit which is needed to get the Output of ALB(A<B) and AGB(A>B) at every EVEN bit position of the Primary inputs and it needs 10 number of Transistors. Input1 and Input2 corresponds to present bit positions and input3 and input4 corresponds to previous Status of ALB(A<B) and AGB(A>B) when used for ALB(A<B) and AGB(A>B) and ALB(A<B) when used for AGB(A>B) and this Block gives True output.

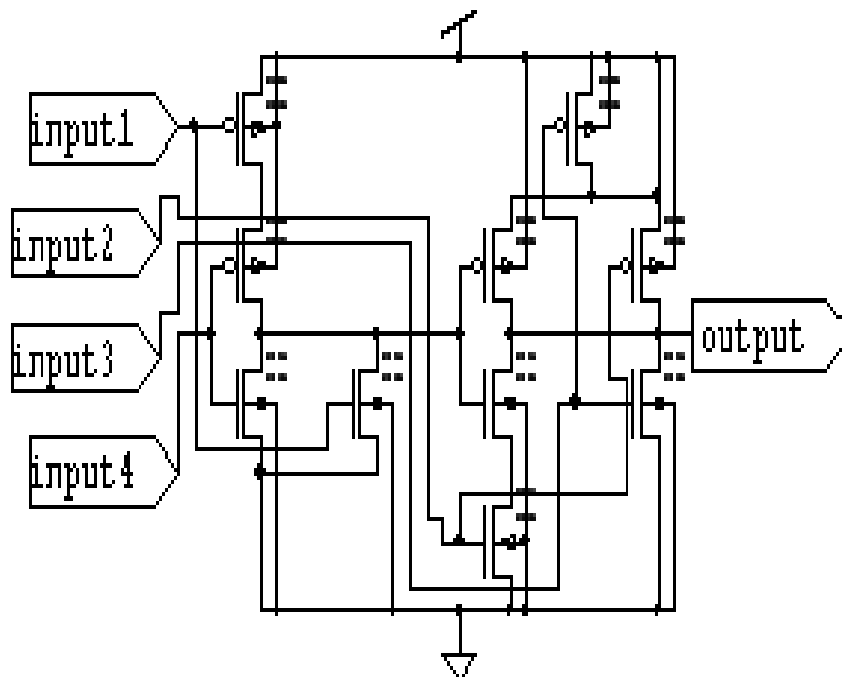


Fig.3 10TBlock(Odd)Circuit

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Fig3 is an 10T BlockOdd Circuit which is needed to get the output of ALB(A<B) and AGB(A>B) at every odd bit position of the Primary inputs and it takes 10 number of Transistors. Input1 and Input2 corresponds to present bit positions and input3 and input4 corresponds to previous Status of ALB(A<B) and AGB(A>B) when used for ALB(A<B) and AGB(A>B) and ALB(A<B) when used for AGB(A>B) and this Block gives False output.

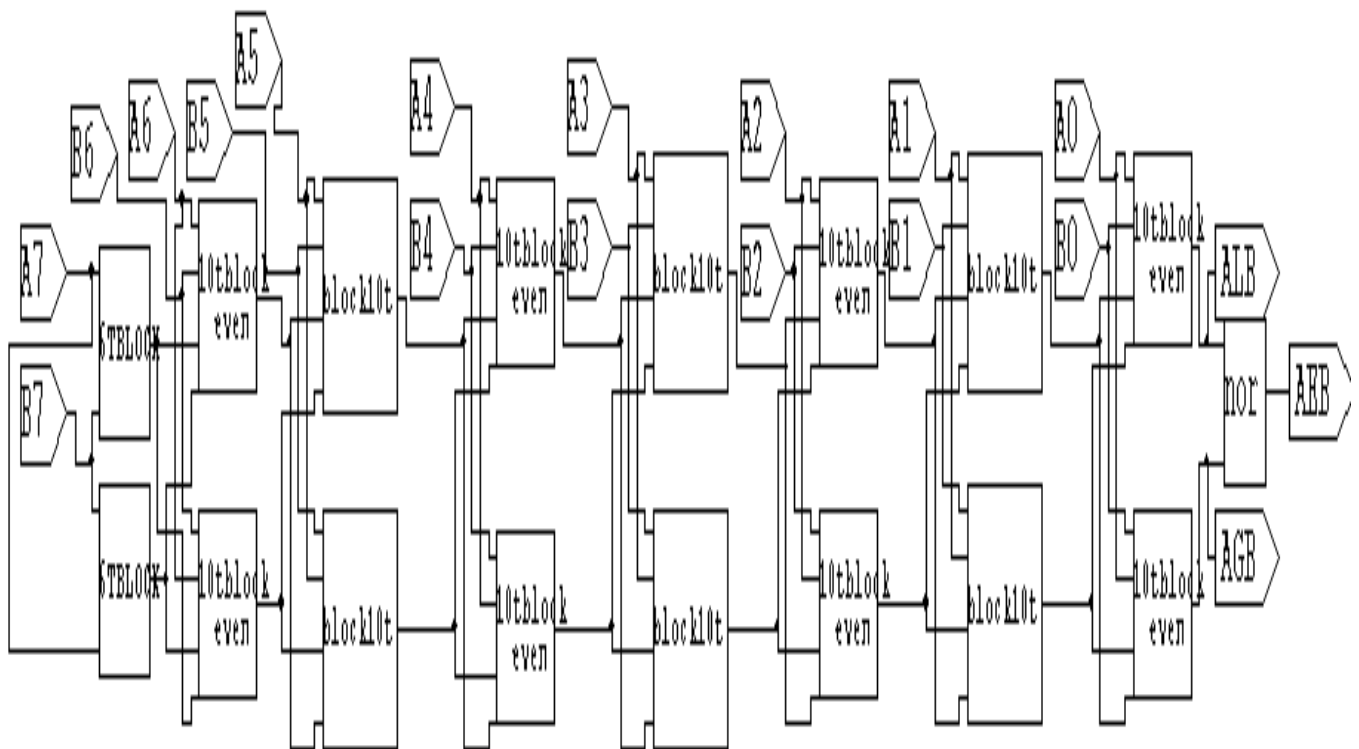


Fig. 4 Schematic of 156 transistor Comparator cell

Fig4 is schematic for 8-bit comparator Circuit which needs Two 6T Blocks, eight 10T Block evens, and six 10T Block Odds and one Nor gate, total Transistor count is $((2*6)+(8*10)+(6*10)+(1*4))$ equals to 156. This Schematic has Transition of 01010101 and the last one corresponds to final output, if Designed for Odd(7) bit Comparator then 1010101 Transition has to be maintained to save many number of inverters.

IV. STATIC CMOS

STATIC CMOS has the advantage of having very less Static power dissipation and static refers to for every input applied there will be possible path to activate the output, which is unlike in DYNAMIC logic which needs pre-charging and then only Evaluation phase can begin. Floor planning is very much essential as it will affect the chip Area required and we might need to go for Standard cell based Design in which the height of every cell is fixed and how much that can be depends on the cell which needed maximum height and this will be beneficial when the cells have to be merged. Since we have designed the circuit by only STATIC CMOS we can merge the cells more comfortably as it has Pull-up and Pull-down networks and these have equal number of Transistors. Transistors placed in series are going to increase the delay we can enhance speed by transistor sizing or by introducing buffer in which we need to sacrifice Area.

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V. PERFORMANCE ANALYSIS

8-bit magnitude comparator has been designed by using STATIC CMOS logic style. The comparator which we designed using STATIC CMOS logic style has less number of transistor count. Our design is extendable to N-bit, from MSB-{1,3,5,7} and so on 10T Blockeven is used and from MSB-{2,4,6} and so on 10T Blockodd is used. Total number of transistor count for N-bit is $(N-1)*20+6+6+4$.

TABLE1 COMPARISON OF AREA IN THREE DESIGNS

64-bit	Design in Reference3	Design in reference10	Design in this paper
(number of transistors)	1556	2976	1276

Table1 shows the comparison between S.W Cheng, Saleh Abdel Hafeez and the proposed Comparator. 1700 transistors were reduced when compared to Saleh Abdel Hafeez for 64-bit, almost in a equal proportion transistor count reduction will be there for N-bit and 280 transistors were reduced in comparison with S.W.Cheng, and count was less due to their logic can only identify '<' and '>=' conditions which in contrast '<', '>' and '=' can be identified in others mentioned in Table.

VI. CONCLUSION

Area is one of the important design constraint as it is proportional to the cost of the design. Since our design has less number of transistors total number of active transistors will be less and it is like only 50% of total transistors will be active, so only 638 transistors will be active for 64-bit. In Saleh Abdel Hafeez comparator only 32% of the total transistors are active but 944 are the active transistors for 64-bit. In equal proportion active transistor count will be there for our proposed design as well as in Saleh Abdel Hafeez design for N-bit.

we are able to design the comparator by using less number of transistors even though Static CMOS needs more number of transistors It shows an 64-bit comparator of the proposed technique only needs 1276 transistors, the technique which we presented can be easily extendable up to N-bit and some Design Techniques to be implemented to ensure that Delay is better

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