

# **BLDC Motor Speed Control and PFC Using Isolated Zeta Converter**

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**ABSTRACT:** A BLDC drive with power factor correction (PFC) for a wide range of speed control and the analysis, design and implementation of an AC-DC isolated Zeta converter in discontinuous current mode (DCM) of operation used for power quality improvement at AC mains. A PFC based isolated Zeta converter operating in discontinuous conduction mode (DCM) is used for controlling the DC link voltage of the voltage source inverter(VSI) with inherent PFC at AC mains using single voltage sensor. The drive is implemented to achieve power factor at AC mains for a wide range of speed control and supply voltage fluctuations. A MATLAB/ Simulink environment is used to simulate the developed model to achieve a wide range of speed control with high PF (Power Factor) and improved PQ (Power Quality) at the supply and the hardware is implemented on PCB.

**KEYWORDS:** Power factor correction (PFC), Brush less Dc Motor (BLDC), Isolated ZETA Converter, Power Quality (PQ)

## **I. INTRODUCTION**

PFC converters are widely used for improving the power quality at AC mains. Different configurations of non-isolated and isolated PFC converter have been reported in the literature for quality is achieved, with power quality indices within limits of IEC 61000-3-2 standard, the power quality at AC mains [1-3]. The cost of these PFC converters are decided by the sensing requirements and depends upon the mode of operation of the PFC converter. There are two modes of operation, Continuous conduction mode (CCM) and discontinuous conduction mode (DCM). If the converter is operating in CCM offers low stress on PFC converter switches but requires sensing of supply voltage, DC link voltage and supply current, which is a costly option in terms of cost of sensors. However, PFC converter operating in DCM requires single voltage sensor for DC link voltage control and inherent power factor correction is achieved at AC mains; but, at the cost of high stress on PFC converter switches [2]. Discontinuous mode of operation is limited to low power applications. A BLDC find applications in household appliances, medical equipment, robotics and automation, transportation and industrial tools. The BLDC motor is a three-phase synchronous motor with three-phase concentrated windings on the stator and permanent magnets on the rotor. It requires a three-phase voltage source inverter (VSI) for achieving an electronic commutation of BLDC motor based on the rotor position as sensed by Hall effects position sensors. A diode bridge rectifier (DBR) with a high value of smoothening capacitor is generally used for feeding the BLDC motor. It draws a distorted supply current from ac mains due to uncontrolled charging and discharging of the dc link capacitor. Such type of supply current is highly distorted in nature and has a very high total harmonic distortion (THD) in the order of 65% -70% which further leads to a poor factor (PF) in the order of 0.72 at ac mains. Such power quality indices are not acceptable within the limits of international power quality standards such as IEC 61000-3-2 [4-6]. A constant DC link voltage is maintained at the DC link capacitor of VSI and PWM based switching is used for the speed control of BLDC motor. This offers high switching losses in the VSI due to high switching frequency of PWM signals and high cost associated due to large number of sensors. Different configuration such as buck, boost and buck-boost, Cuk, SEPIC converter for a PFC based BLDC motor drive using a single-phase PFC converter has been reported in [7-10]. A PFC based Cuk converter feeding BLDC motor has been proposed in [7]. This configuration uses a variable voltage control of VSI for speed control of BLDC motor and hence operates the VSI in fundamental switching frequency for reduced switching losses. For a CCM mode of operation of PFC Cuk converter, this requires three sensors for voltage control with PFC at AC mains. This configuration is mainly suited for high power applications.

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Vol. 6, Issue 4, April 2017

Non-isolated bridgeless converters have been proposed in [8-10] for feeding BLDC motor but have high number of component count. Moreover, these configurations can't be used in many applications requiring a galvanic isolation for safety issues.

## II. SYSTEM CONFIGURATION

In Fig. 2.1 shows the PFC Isolated-Zeta converter fed BLDC drive. A single-phase supply is used to feed a DBR followed by a filter and an isolated -Zeta converter. The filter is designed to avoid any switching ripple in the DBR and the supply system. An isolated -Zeta converter is designed to operate in DCM to act as an inherent power factor corrector. This combination of DBR and PFC converter is used to feed a BLDC drive via a three-phase VSI. The DC link voltage of the VSI is controlled by varying the duty ratio of the PWM pulses of PFC converter switch. However, VSI is operated in a low frequency switching to achieve an electronic commutation of BLDC for reduced switching losses. A single voltage sensor is used at the front-end converter for the control of DC link voltage for speed control of BLDC.

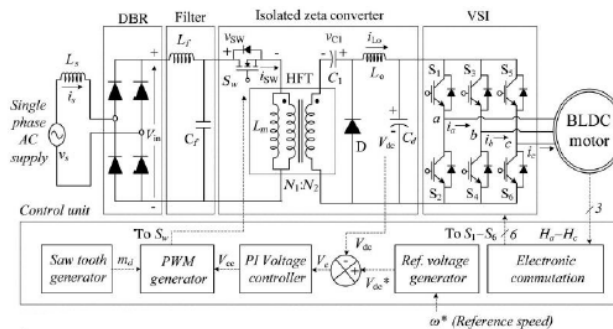


Figure 2.1: PFC based Isolated - Zeta converter fed BLDC drive

Mode-1

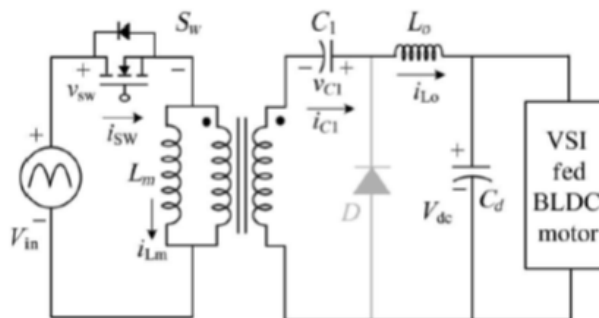


Figure 2.2: Operation of isolated PFC zeta converter, mode-1

When switch ( $S_w$ ) is turned on, a current in magnetizing inductance ( $L_m$ ) of high frequency transformer (HFT) increases as shown in Fig. 2.2 The intermediate capacitor ( $C_1$ ) supplies energy to an output inductor ( $L_0$ ) and the DC link capacitor ( $C_d$ ). Hence, voltage across intermediate capacitor ( $V_{c1}$ ) reduces and the current in output inductor ( $i_{L0}$ ) and DC link voltage ( $V_{dc}$ ) are increased.

Mode-2

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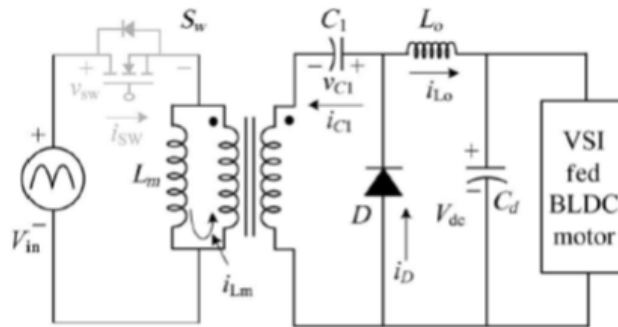


Figure 2.3: Operation of isolated PFC zeta converter, mode-2

When switch ( $S_w$ ) is turned off, the current in magnetizing inductance ( $L_m$ ) of HFT and output inductor ( $L_o$ ) starts reducing. This energy of HFT is transferred to the intermediate capacitor ( $C_1$ ) and therefore voltage across it increases. Diode ( $D$ ) conducts in this mode of operation and the DC link voltage ( $V_{dc}$ ) increases.

Mode-3

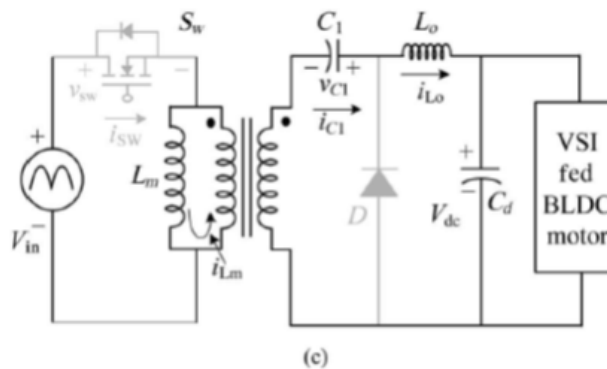


Figure 2.2: Operation of isolated PFC zeta converter, mode-3

This mode is DCM such that the energy of HFT is completely discharged as shown in Fig. 2.4. The intermediate capacitor ( $C_1$ ) and the DC link capacitor ( $C_d$ ) supply the energy to the output inductor ( $L_o$ ) and the load, respectively. Hence, the DC link voltage ( $V_{dc}$ ) and intermediate capacitors voltage ( $V_{C1}$ ) are reduced and the output inductor current increases in this mode of operation.

### III. DESIGN OF ISOLATED PFC ZETA CONVERTER

An isolated PFC Zeta converter is designed to operate in discontinuous conduction mode (DCM) such that the current flowing in magnetizing inductance of HFT ( $L_m$ ) becomes discontinuous in a switching period. A PFC converter of 250 W ( $P_{max}$ ) is designed for the selected BLDC. For a wide range of speed control, the DC link voltage is controlled from a low value of 50V ( $V_{dc\_min}$ ) to a rated voltage of 130 V ( $V_{dc\_max}$ ) with supply voltage variation from 170 V ( $V_{smin}$ ) to 270 V ( $V_{smax}$ ).

The input voltage,  $V_S$  applied to the PFC converter as:

$$V_S(t) = V_m \sin(\omega_L t) = 220\sqrt{2} \sin(314t) \text{ V} \quad (1)$$

Where ( $V_m$ ) is peak input voltage (i.e.  $\sqrt{2} * V_s$ ) and

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Vol. 6, Issue 4, April 2017

( $\omega_L = 2\pi f$ ) where  $f$  is the line frequency, i.e., 50 Hz.

Since the speed of the BLDC motor is controlled by varying the dc link voltage of the VSI, therefore, the instantaneous power  $P_i$  at any dc link voltage ( $V_{dc}$ ) is taken as linear function of  $V_{dc}$ .

Where  $R_L$  represents the emulated load resistance,  $f_s$  is the switching frequency (which is taken as 20 kHz), and  $P_i$  is the instantaneous power. The critical value of magnetizing inductance ( $L_{mc}$ ) is calculated for maximum current corresponding to lowest possible value of supply voltage, i.e., 170 V ( $V_s$  min) using (6) as:

$$L_{mc} = \frac{R_L \{1 - D_a\}^2}{2D_a f_s \{N_2/N_1\}^2} = \left( \frac{V_{dc}^2}{P_i} \right) \frac{\{1 - D_a\}^2}{2D_a f_s \{N_2/N_1\}^2}$$

$$= \frac{(67.6)}{2 \times 0.5195 \times 20000 \times \{5\}^2} = 3.65 \text{ mH} \quad (2)$$

Hence, to achieve a DCM, the value of magnetizing inductance of HFT ( $L_m$ ) is selected lower than  $L_{mc}$ . Therefore, the value of  $L_m$  is selected around 1/10th of  $L_{mc}$ , i.e., 360  $\mu$ H to achieve a discontinuous current conduction.

This output inductor is designed for rated dc link voltage of 130 V ( $V_{dc \text{ max}}$ ) for a minimum value of duty ratio ( $D_b$ ) corresponding to a peak of maximum supply voltage of  $270\sqrt{2}$  ( $\sqrt{V_s \text{ max}}$ ) as:

$$L_o = \frac{R_L \{1 - D_b\}}{f_s (kI_o)} = \frac{130 \{1 - 0.4050\}}{20000 \times (0.4 \times 1.35)} = 6.445 \text{ mH} \quad (3)$$

Where ' $\kappa$ ' represents the percentage ripple of the output inductor current which is taken as 40% of output inductor current ( $k$ ). Output inductor of 6.6mH is selected.

The intermediate capacitor ( $C_1$ ) is calculated at maximum value of dc link voltage ( $V_{dc}$ ) as:

$$C_1 = \frac{V_{dc \text{ max}} D_b (t)}{\eta \{ \sqrt{2} V_s \text{ max} + V_{dc \text{ max}} \} f_s \{ V_{dc \text{ max}}^2 \}}$$

$$C_1 = \frac{130 \times 0.4050}{0.1 \times \{ 270\sqrt{2} + 130 \} \times 20000 \left( \frac{250}{130^2} \right)} = 760.35 \text{ nF} \quad (4)$$

Where  $\eta$  is the permitted ripple voltage across intermediate capacitor and is taken as 10% of  $V_{C1}$ . Hence, an intermediate capacitor of 750 nF is selected for the application.

The value of dc link capacitor ( $C_d$ ) is calculated as:

The worst case design occurs for the minimum value of dc link voltage, i.e., 12 V ( $V_{dc \text{ min}}$ ) and is expressed as:

$$C_d = \left( \frac{P_{\text{min}}}{V_{dc \text{ min}}} \right) \frac{1}{2\omega (\eta V_{dc \text{ min}})}$$

$$= \left( \frac{96}{50} \right) \frac{1}{2 \times 314 \times (0.03 \times 50)} = 2038.36 \mu\text{F} \quad (5)$$

Therefore, the dc link capacitor ( $C_d$ ) with a nearest possible value of 2200  $\mu$ F is selected for this application. A low-pass LC filter is used to avoid the reflection of higher order harmonics in supply system. The maximum value of filter capacitance ( $C_{\text{max}}$ ) is given as:

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Vol. 6, Issue 4, April 2017

$$C_{max} = \frac{I_{Fpeak}}{\omega_L V_m} \tan(\theta) = \left( \frac{P_{max} \sqrt{2}/V_s}{\omega_L \sqrt{2} V_s} \right)$$

$$= \frac{250 \times \sqrt{2}/220}{314 \times 220 \times \sqrt{2}} \tan(1^\circ) = 303.21 \text{ nF} \quad (6)$$

Where ‘θ’ is the displacement angle between the fundamental component of supply voltage and supply current which is taken as 1°. Thus, a filter capacitor  $C_f$  of 330 nF is selected. The value of filter inductor is designed by considering the source impedance ( $L_s$ ) of 3% of the base impedance

$$L_f = L_{req} + L_s \Rightarrow L_{req} = L_f - L_s$$

$$L_{req} = \frac{1}{4f_c^2 \pi^2 C_f} - 0.03 \left( \frac{1}{\omega_L} \right) \left( \frac{V_s^2}{P_D} \right)$$

$$= \frac{1}{3245} - 0.03 \left( \frac{1}{314} \right) \left( \frac{220^2}{250} \right) = 5.94 \text{ mH} \quad (7)$$

Where  $f_c$  is the cutoff frequency which is selected such that  $f_L < f_c < f_s$ . Therefore,  $f_c$  is taken as  $f_s/10$ . This LC filter with inductance  $L_f$  and capacitance  $C_f$  is selected as 6 mH and 330 nF, respectively.

Control of isolated pfc zeta converter-fed **BLDC** motor drive:

The control of the proposed PFC-based BLDC motor drive is divided into two categories: control of PFC converter for dc link voltage control and control of three-phase VSI for electronic commutation of BLDC motor.

A voltage-follower approach is used for the control of isolated zeta converter operating in DCM. This control scheme consists of a reference voltage generator, voltage error generator, voltage controller, and a PWM generator. A “reference voltage generator” generates a reference voltage  $V_{dc}^*$  by multiplying the reference speed ( $\omega^*$ ) with the motor’s voltage constant ( $K_v$ ) as:

$$V_{dc}^* = K_v \omega^* \quad (8)$$

The “voltage error generator” compares this reference dc link voltage ( $V_{dc}^*$ ) with the sensed dc link voltage ( $V_{dc}$ ) to generate an error voltage ( $V_e$ ) given as:

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k) \quad (9)$$

$$\begin{cases} \text{if } m_d < V_{ct} \text{ then } S_w = \text{"ON"} \\ \text{if } m_d > V_{ct} \text{ then } S_w = \text{"OFF"} \end{cases} \quad (10)$$

Where ( $S_w$ ) represents the gate signal to PFC converter switch. A rate limiter is also introduced for limiting the stator currents of the BLDC motor during step change in dc link voltage for speed control. This rate limiter limits the rate of change of duty ratio of PWM pulses which is to be given to the PFC converter switch. The rising and falling slew rates of the rate limiter are selected to limit the peak current within twice the rated current of BLDC motor.

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Vol. 6, Issue 4, April 2017

## IV. SIMULATION AND RESULT ANALYSIS

The performance of the BLDC motor drive is simulated in MATLAB/SIMULINK environment using the Sim-Power-System toolbox. The performance evaluation of the BLDC drive is categorized in terms of the performance of the BLDC motor and isolated zeta converter. The parameters associated with the BLDC motor such as speed (N), electromagnetic torque ( $T_e$ ) are analyzed for the proper functioning of the BLDC motor. Parameters such as supply voltage ( $V_s$ ), supply current ( $i_s$ ), dc link voltage ( $V_{dc}$ ), of the PFC isolated zeta converter are analyzed to demonstrate its proper functioning.

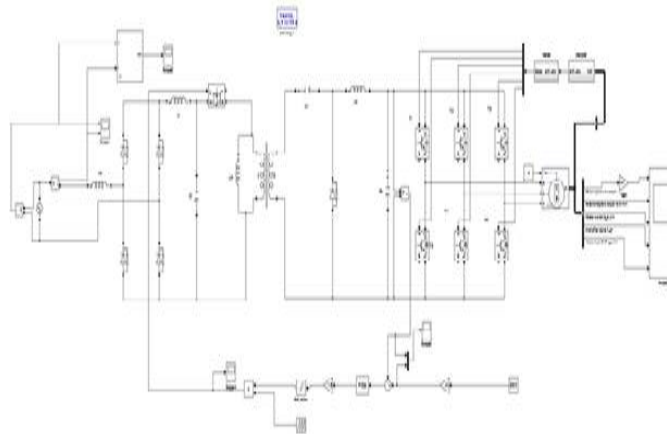


Figure.4.1- Simulation schematic

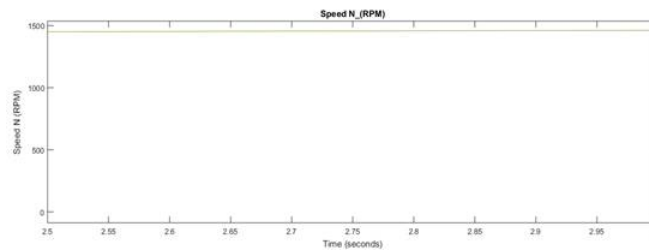


Figure.4.2-simulated waveform of rotor speed (N)

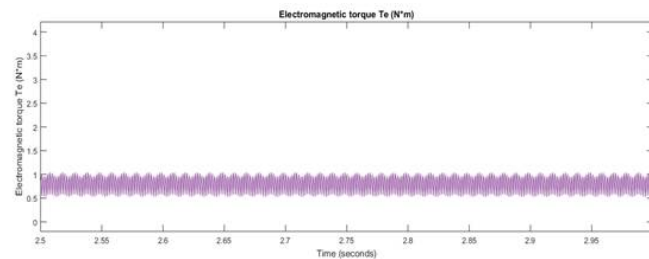


Figure.4.2-simulated waveform of Electromagnetic torque ( $T_e$ )

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Vol. 6, Issue 4, April 2017

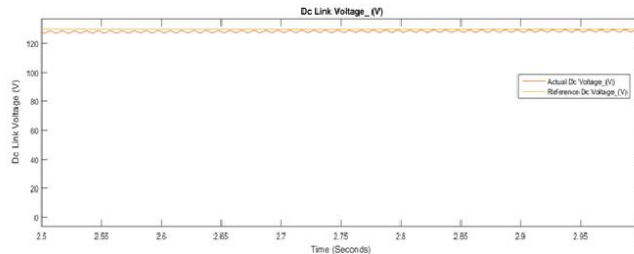


Figure.4.3-Simulated waveform of dc link voltage 130V

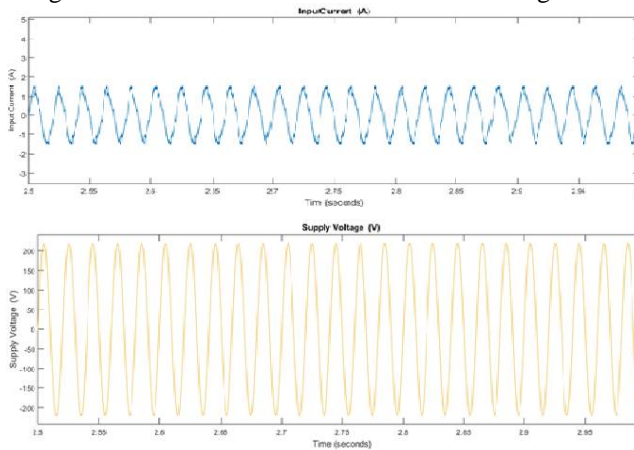


Figure.4.4- (a) Input supply current (b) supply voltage

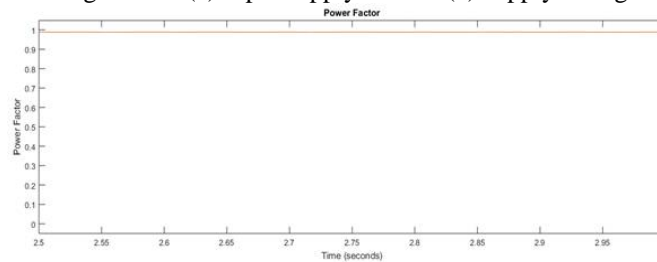


Figure.4.5- Power Factor

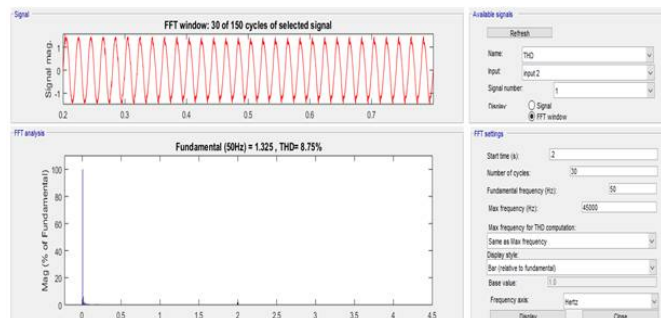


Figure.4.6- Harmonic spectrum of supply current

Harmonic spectrum of the supply current at rated speed is shown in Fig: 4. THD of the current is obtained as 8.75% which is below the limit given in IEC 61000-3-2 standard.

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Vol. 6, Issue 4, April 2017

## V.HARDWARE RESULT

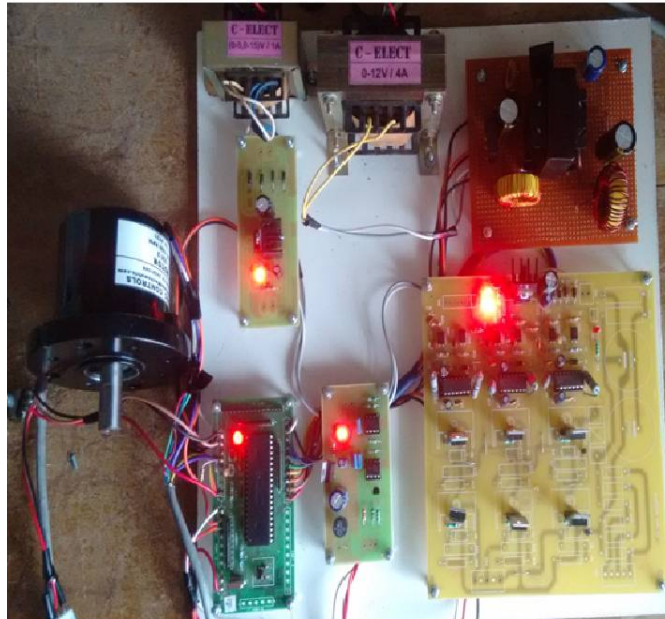


Figure 5.1- Experimental setup

Performance of proposed drive is validated on a developed prototype of BLDC motor drive. A PIC processor is used for the development of proposed drive. An opto-isolation is used between PIC processor and gate driver of VSI and PFC switches. Hall signal filtering and power circuitries are also developed for Hall effect position sensors. Test results of proposed BLDC motor drive are discussed as follows:

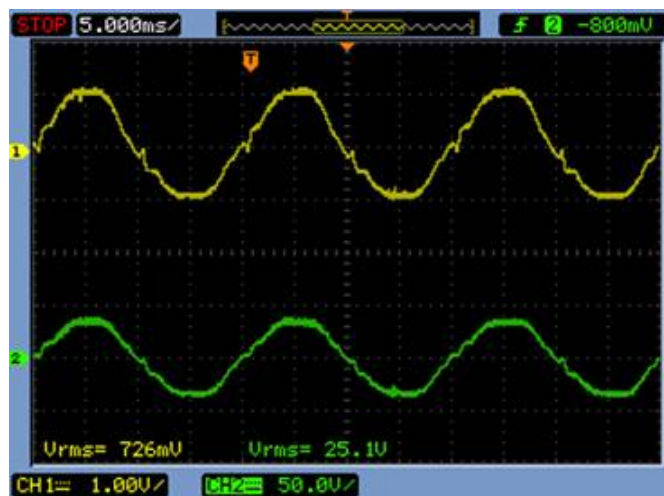


Figure.5.2- supply voltage and current

Fig. 5.2- shows test results of BLDC motor drive operating with supply voltage as 24 V and dc link voltages of 24 V and 12 V corresponding to the speed of BLDC motor as 1440 and 530 rpm, respectively. As shown in these figures, the



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Vol. 6, Issue 4, April 2017

dc link voltage is maintained at desired reference value. Moreover, magnitude and frequency of the stator current demonstrate the operation BLDC motor at different speeds. A sinusoidal supply current in phase with supply voltage is obtained which shows a near unity power factor at both the values of dc link voltages.

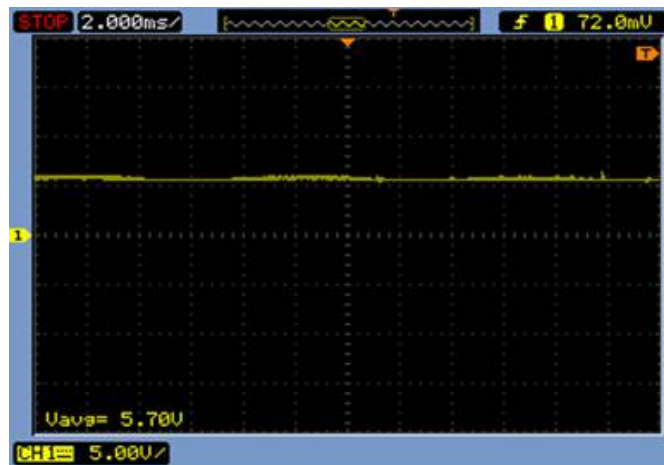


Figure.5.3- Dc link voltage

The voltage of PFC converter switch and its enlarged waveform are shown in Fig. 5.4 (a) and (b), respectively. A peak voltage and current stresses of 25 V is observed as shown in Fig. 5.4 (b), which are acceptable for a PFC converter of 70 W operating in DCM

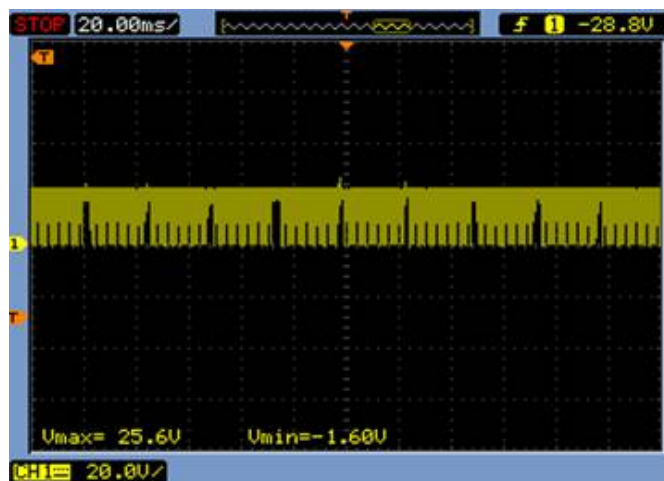


Figure.5.4- (a) switch voltage

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Vol. 6, Issue 4, April 2017

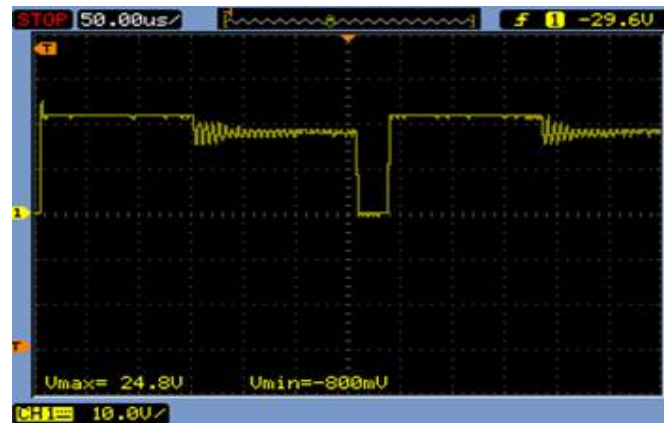


Figure.5.4 (b) Enlarged waveform of switch voltage

## VI.CONCLUSION

The BLDC drive provides acceptable power quality, high efficiency and thus it is suitable for adjustable speed drive applications in residential appliances, such as refrigeration and air conditioning. The motor speed control is achieved by controlling the voltage at dc bus and operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor for reducing the switching losses in VSI. The front-end DBR with isolated Zeta converter has been operated in DCM for achieving an inherent power factor correction at ac mains. A prototype of proposed drive has been implemented with satisfactory test results for its operation at wide range of supply voltages. THD of input supply current is 8.75 %. Hence power quality indices obtained are found to be satisfactory and within the acceptable limits by IEC 61000-3-2.

## APPENDIX

**BLDC Motor Specifications:** No of Poles: 4, Rated Dc bus voltage ( $V_{dc}$ ):130 V, Rated Speed ( $\omega_r$ ) :1500 rpm, Rated torque ( $T_{rated}$ ): 1.2 Nm, Rated Power ( $P_{rated}$ ):188 W, Voltage Constant ( $K_v$ ): 57.59 V (Peak –Peak)/Krpm, Torque Constant ( $K_t$ ): 0.55 Nm/A (Peak –Peak), Stator Winding's per Phase resistance ( $R_{ph}$ ): 4.32  $\Omega$ , Stator Winding's per phase inductance ( $L_{ph}$ ):8 mH, Moment of inertia ( $J$ ): 1.8Kg-cm<sup>2</sup>.

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