

# The Flexible DSP Accelerator Architecture using Error Tolerant Adder

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**ABSTRACT:** In the digital signal processing (DSP) domain, Hardware acceleration is proved an extremely promising implementation strategy. Instead of adopting a monolithic application-specific integrated circuit design approach, a novel accelerator architecture comprising flexible arithmetic components that support the execution of a large set of operation templates found in DSP kernels is introduced. One of its major peculiarity is to enable computations to be aggressively performed with carry-save (CS) formatted data. Incorporation of Error Tolerant Adder is another speciality. Advanced arithmetic design concepts, i.e., recoding techniques, and more enhanced arithmetic components are utilized enabling CS optimizations to be performed in a larger scope than in previous approaches.

**KEYWORDS:** Arithmetic optimizations, carry-save (CS) form, datapath synthesis, Error Tolerant Adder, flexible accelerator, operation chaining.

## I.INTRODUCTION

Nowadays, intensive Digital Signal Processing (DSP) functions are required to be performed by the embedded systems. The incorporation of heterogeneity through specialized hardware accelerators improves performance and reduces energy consumption. Previously, application-specific integrated circuits, domain specific reconfigurable accelerators, Flexible DSP accelerators using carry-save arithmetic were used for this purpose.

The requirement of high performance with less power consumption and reduced area always leads to new researches and innovations. All these requirements are satisfied in this project. In the previous flexible DSP accelerator, fast operation chaining is achieved. But, it has high power consumption and area. So energy saving and small size are major consideration. Improved performance can also be achieved with this new accelerator.

The invention of a hardware accelerator for DSP systems can change the digital world itself. To make a flexible accelerator with reduced energy consumption and area is the major objective of this project. As the name implies, the accelerator should be flexible, that is, it should perform all the required arithmetic operations. It should not be application specific. For any application, this accelerator should be useful. For that purpose, Carry-save adder, Booth multiplier, Error Tolerant Adder are incorporated in the basic computational unit, which is known as Flexible arithmetic component which is optimum in both arithmetic and architectural level.

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## II. RELATED WORK

In the early stages, application-specific integrated circuits (ASICs) form the ideal acceleration solution in terms of performance and power, but their inflexibility leads to increased silicon complexity, as multiple instantiated ASICs are needed to accelerate various kernels. Many researchers have proposed the use of domain-specific coarse-grained reconfigurable accelerators in order to increase ASICs' flexibility without significantly compromising their performance.

High-performance flexible datapaths have been proposed to efficiently map primitive or chained operations found in the initial data-flow graph (DFG) of a kernel. The templates of complex chained operations are either extracted directly from the kernel's DFG or specified in a predefined behavioral template library. Design decisions on the accelerator's datapath highly impact its efficiency. Existing works on coarse-grained reconfigurable datapaths mainly exploit architecture-level optimizations, e.g., increased instruction-level parallelism (ILP). The domain-specific architecture generation algorithms vary the type and number of computation units achieving a customized design structure. Recently, aggressive operation chaining is adopted to enable the computation of entire subexpressions using multiple ALUs with heterogeneous arithmetic features.

The aforementioned reconfigurable architectures exclude arithmetic optimizations during the architectural synthesis and consider them only at the internal circuit structure of primitive components, e.g., adders, during the logic synthesis. However, research activities have shown that the arithmetic optimizations at higher abstraction levels than the structural circuit one significantly impact on the datapath performance. The timing-driven optimizations based on carry-save (CS) arithmetic were performed at the post-Register Transfer Level (RTL) design stage. The common subexpression elimination in CS computations is used to optimize linear DSP circuits. There developed some transformation techniques on the application's DFG to maximize the use of CS arithmetic prior the actual datapath synthesis. The aforementioned CS optimization approaches target inflexible datapath, i.e., ASIC, implementations. Recently, a flexible architecture combining the ILP and pipelining techniques with the CS-aware operation chaining is introduced. However, all the aforementioned solutions feature an inherent limitation, i.e., CS optimization is bounded to merging only additions/subtractions. A CS to binary conversion is inserted before each operation that differs from addition/subtraction, e.g., multiplication, thus, allocating multiple CS to binary conversions that heavily degrades performance due to time-consuming carry propagations.

The existing accelerator architecture comprises flexible computational units (FCUs), which enable the execution of a large set of operation templates found in DSP kernels. It has a flexible datapath architecture that exploits CS optimized templates of chained operations. Each FCU can be configured to any of the different operation templates. The FCU enables intratemplate operation chaining by fusing the additions performed before/after the multiplication. It has good performance with large area and energy consumption.

## III. ERROR TOLERANT ADDER

The ETA method is introduced because of its high speed performance. There are many different types of fast adder like carry skip adder (CSK), carry-select adder (CSL) and carry-look-ahead adder (CLA) has been developed and also there are many low-power adder design techniques that have been proposed. To provide balance between speed and power consumption, error tolerant design techniques have a solution for this problem (i.e., trade off's between speed and power consumption). For that reason, addition arithmetic i.e., Error tolerant adder ETA is used here. For example consider two 16-bit input operands at first, split the input operand into two parts: accurate part and inaccurate part but length of each part need not necessary to be equal. However, higher order bits are considered as an accurate part and lower order bits are considered as an inaccurate part. The addition process starts from the middle toward the two opposite direction simultaneously.



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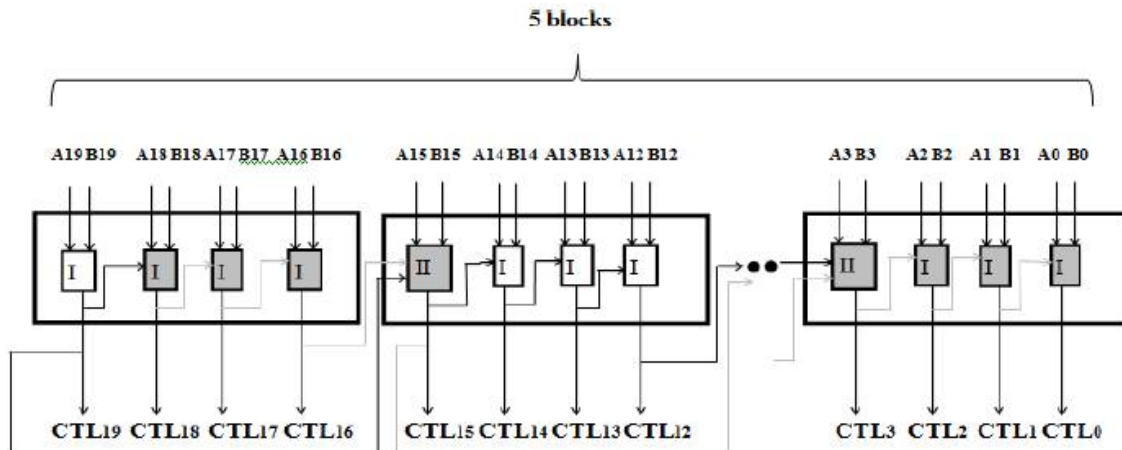


Fig. 2 Control block of overall architecture

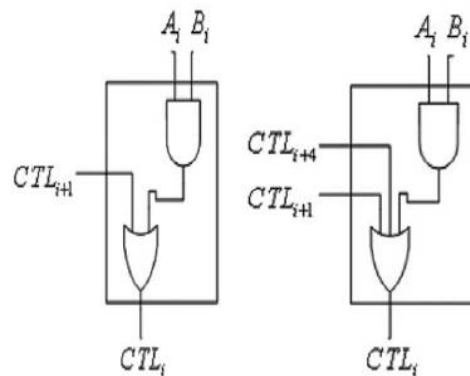


Fig.3 Schematic implementation of CSGS of Type 1 & 2

The control signal generated by the leftmost cell of each group is connected to the input of the leftmost cell in the next group. Shaded portion in Fig. 2 represent the worst case propagation path. The extra connections allow the propagated high control signal to jump from one group to another instead of passing through all cells.

## IV. CARRY-SAVE ARITHMETIC

CS representation has been widely used to design fast arithmetic circuits due to its inherent advantage of eliminating the large carry-propagation chains. CS arithmetic optimizations rearrange the application's DFG and reveal multiple input additive operations (i.e., chained additions in the initial DFG), which can be mapped onto CS compressors. The goal is to maximize the range that a CS computation is performed within the DFG. However, whenever a multiplication node is interleaved in the DFG, either a CS to binary conversion is invoked or the DFG is transformed using the distributive property. Thus, the aforementioned CS optimization approaches have limited impact on DFGs dominated by multiplications, e.g., filtering DSP applications.

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Here, the aforementioned limitations are tackled by exploiting the CS to modified Booth (MB) recoding each time a multiplication needs to be performed within a CS-optimized datapath. Thus, the computations throughout the multiplications are processed using CS arithmetic and the operations in the targeted datapath are carried out without using any intermediate carry-propagate adder for CS to binary conversion, thus improving performance.

## V. PROPOSED FLEXIBLE ACCELERATOR

The proposed flexible accelerator architecture is shown in Fig. 4. Each FAC operates directly on CS operands and produces data in the same form for direct reuse of intermediate results. Each FAC operates on 16-bit operands. Such a bit-length is adequate for the most DSP datapaths, but the architectural concept of the FAC can be straightforwardly adapted for smaller or larger bit-lengths. The number of FACs is determined at design time based on the ILP and area constraints imposed by the designer.

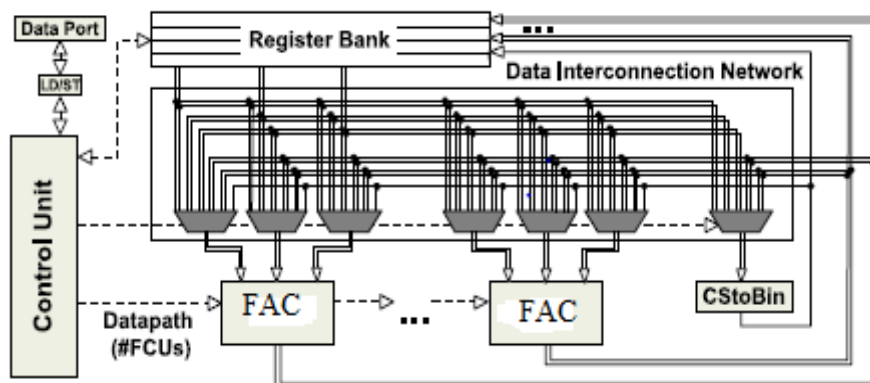


Fig.4 Abstract of the flexible datapath

The CStoBin module is a ripple-carry adder and converts the CS form to the two's complement one. The register bank consists of scratch registers and is used for storing intermediate results and sharing operands among the FACs. Different DSP kernels (i.e., different register allocation and data communication patterns per kernel) can be mapped onto the proposed architecture using post-RTL datapath interconnection sharing techniques. The control unit drives the overall architecture (i.e., communication between the data port and the register bank, configuration words of the FACs and selection signals for the multiplexers) in each clock cycle.

The structure of the FAC has been designed to enable high-performance flexible operation chaining based on a library of operation templates. Each FAC can be configured to any of the different operation templates. The proposed FAC enables intratemplate operation chaining by fusing the additions performed before/after the multiplication and performs any partial operation template of the following complex operations:

$$W^* = A \times (X^* + Y^*) + K^* \quad \text{————— (1)}$$

$$W^* = A \times K^* + (X^* + Y^*) \quad \text{————— (2)}$$

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The following relation holds for all CS data:  $X^* = \{XC, XS\} = XC + XS$ . The operand  $A$  is a two's complement number. The alternative execution paths in each FCU are specified after properly setting the control signals of the multiplexers MUX1 and MUX2. The multiplexer MUX0 outputs  $Y^*$  when  $CL0 = 0$  (i.e.,  $X^* + Y^*$  is carried out) or  $Y^*$  when  $X^* - Y^*$  is required and  $CL0 = 1$ . The two's complement 4:2 CS adder produces the  $N^* = X^* + Y^*$  when the input carry equals 0 or the  $N^* = X^* - Y^*$  when the input carry equals 1. The MUX1 determines if  $N^*$  (1) or  $K^*$  (2) is multiplied with or divided by  $A$ . The MUX2 specifies if  $K^*$  (1) or  $N^*$  (2) is added with the multiplication product. The multiplexer MUX3 accepts the output of MUX2 and its 1's complement and outputs the former one when an addition with the multiplication product is required (i.e.,  $CL3 = 0$ ) or the later one when a subtraction is carried out (i.e.,  $CL3 = 1$ ). The 1-bit ace for the subtraction is added in the Error Tolerant Adder. These are the operations that can be carried out by the proposed FAC.

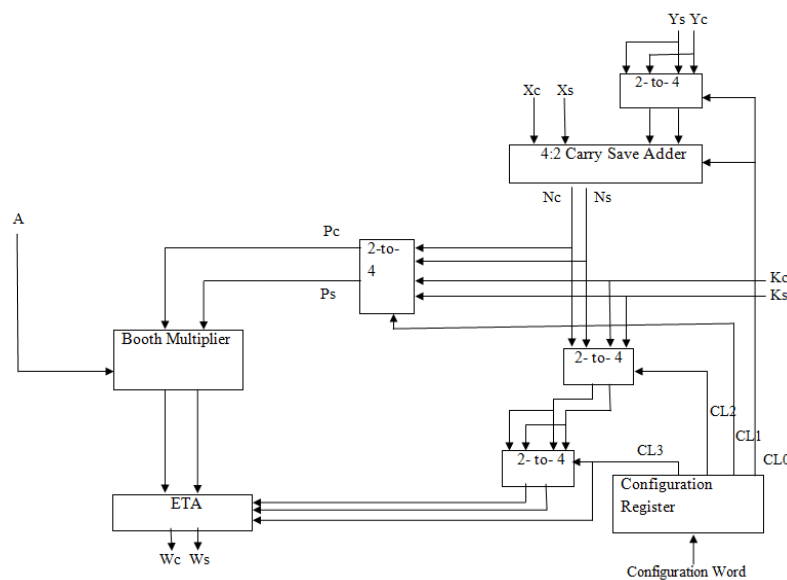


Fig.5 FAC

The multiplier comprises a CS-to-MB module, which adopts a recently proposed technique to recode the 17-bit  $P^*$  in its respective MB digits with minimal carry propagation. The multiplier's product consists of 17 bits. The multiplier includes a compensation method for reducing the error imposed at the product's accuracy by the truncation technique. However, since all the FAC inputs consist of 16 bits and provided that there are no overflows, the 16 most significant bits of the 17-bit  $W^*$  (i.e., the output of the ETA, and thus, of the FAC) are inserted in the appropriate FAC when requested.

## VII. EXPERIMENTAL RESULT

In this Flexible DSP Accelerator, better performance with reduced energy consumption and area can be achieved. Better performance implies both faster operation and the combination of addition, subtraction and multiplication operations. Less power is consumed by the new accelerator. Area is also reduced. The improvement in these three main factors makes this accelerator favourable.



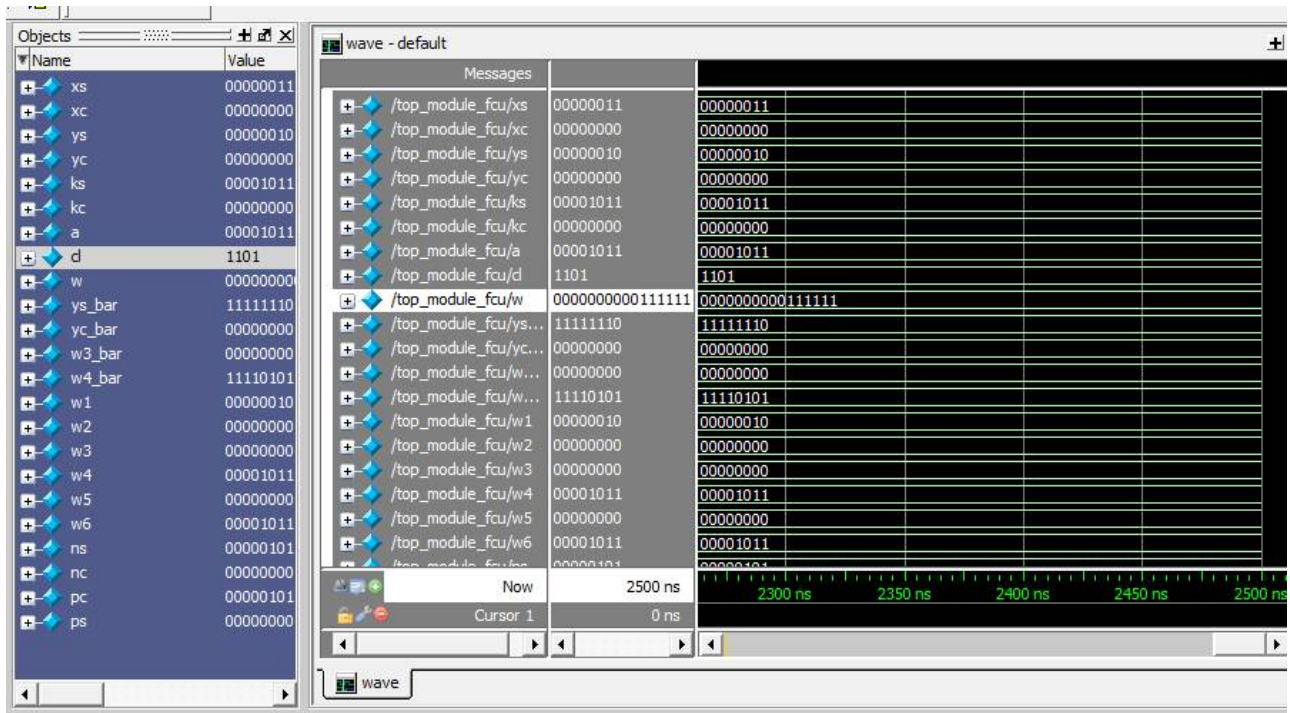


Fig.4.1 Simulation result of the designed Flexible DSP accelerator

The accelerator proposed in this project is an optimum solution when considering power, delay and area. It can change the digital systems to a more comfortable zone, with small size, reduced energy consumption and faster operations. Incorporating a divider in the FAC makes the accelerator a better one. It will improve the performance, but may lead to large area. Anyway, it improves the performance of digital systems. Replacing components in the FAC may help it to handle more no.of bits which also improves the system performance.

## VIII. CONCLUSION

A flexible accelerator architecture that exploits the incorporation of CS arithmetic optimizations to enable fast chaining of additive, multiplicative and division operations is introduced. It improves the performance of DSP systems. The proposed flexible accelerator architecture is able to operate on both conventional two's complement and CS-formatted data operands, thus enabling high degrees of computational density to be achieved. The Error Tolerant Adder improves the performance. Theoretical and experimental analyses have shown that the proposed solution forms an efficient design tradeoff point delivering optimized latency /area and energy implementations.

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