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Design and Analysis of DRAM Cell Using Transmission Gate

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ABSTRACT: Memories play an essential role in design of any electronics design; there are two types of memories used in modern day i.e. Read Only Memory (ROM) and Random Access Memory (RAM). In the proposed system analysis of DRAM cell by using transmission gate has been shown. In proposed circuit transmission gate is used as access transistor. This circuit offers improved process variation and improved read stability which makes it a promising choice for on chip memory for next generation microprocessor.

KEYWORDS: Read Only Memory (ROM), Random Access Memory (RAM), microprocessor.

I. INTRODUCTION

Dynamic random access memory plays very important role in the world of microprocessor. DRAM offers very high density & low cost, due to this DRAM is used by advanced processors for on chip data & program memory. In today's generation trade off is in low power consumption, low leakage current, low cost & compactness, but design complexity is increased due to reduction in size. Leakage power and delay are most important factors which affects the performance of DRAM cell. In new generation microprocessors, on chip memories provides high system performance utilizing a significant portion of entire die space. On chip caches based on SRAM cells which are scaled down very well with technology as technology nano-scaling promises increasing transistor density & increasing performance in microprocessors. However, stability, performance & leakage power are major issues in scaling process of SRAM cell; we can avoid scaling limitations of SRAM cell by designing a new circuit.

Dynamic memories give better solution, as it provides good data storage structure in the process core. DRAM is volatile memory, which holds instructions temporarily required by CPU for performing the task. DRAM cell is constructed by using transistor and capacitor, where capacitor is used to produce 1 or 0. As capacitor is used in DRAM cell, information stored in capacitor degraded constantly, because of this DRAM cell need to be refreshed periodically which leads to the power consumption. The design of conventional 3T DRAM cell decreases the power consumption and access delay but it doesn't provide good stability. We proposed a DRAM cell using transmission gate to improve the stability and compare their performance with 3T DRAM cell. The rest of this paper organized as: in Section II we discuss the different systems, Section III describes structure of DRAM cell using Transmission gate, in section IV simulation results are given. Conclusion is presented in section V.

II. RELATED WORK

Sameya Firdous and T Nagaraju [1] present a method for design a variability aware SRAM cell. The proposed architecture of the TG8T SRAM cell is analogous to the standard 6T SRAM Cell. The proposed architecture of the TG8T SRAM cell is analogous to the standard 6T SRAM cell; the only exception is that they possess full transmission gates which replace an access pass transistor. Transmission gate is used to further reduced leakage current penetrating in the 8T SRAM cell. Comparative analysis is performed by using transmission gate. The simulation result of proposed system shows the leakage current of TG8T SRAM cell is improved as compared to conventional 6T SRAM cell.

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Priyanka Kushwah et al. [2] proposed system, in which analysis of DRAM logic compatible 3T cell has been shown. DRAM is basically an array of memory cells, each cell consist of transistor and capacitor to store single bit data. This is named as dynamic RAM because of its leakage phenomenon which degrades the charge stored in memory cell with time that is it requires periodic refreshment in order to retain data. In this section DRAM cell with three transistors is described. Fig. 1 shows the structure of 3T DRAM cell, here three transistors and one capacitor is used. Transistor M2 is used as access transistor to store information data. Transistor M1 and M3 are used as switches, each switch is turn ON or OFF according to write and read operation respectively

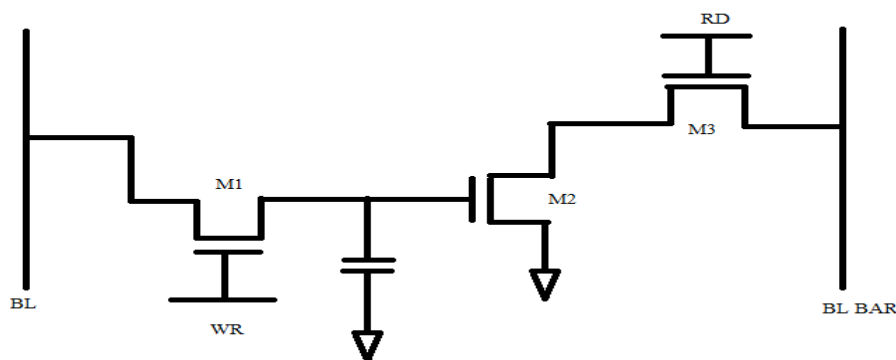


Fig. 1 shows the structure of 3T DRAM cell [1].

Vamsi J. and B. Rambabu [3] presents a 4T DRAM element for faster digital system applications, which deals with analysis of average power consumption of dram cell designs for the nanometer scale memories. The major contributor of power in DRAM is the off state leakage current, improving the power efficiency, average power consumption of the overall system. This proposed system is designed 3T DRAM cell and 4T DRAM cells by using TANNER EDA tool and their average power consumption are compared. Average power consumption, write access time, read access time and retention time of 4T, 3T DRAM cell are simulated and compared on 32 nm technology. Table 1 shows the power dissipation and delay time of 1T,2T,3T AND 4T DRAM for read and write operation.

Table 1 Power Dissipation and Delay Time of 1T, 2T, 3T AND 4T DRAM for Read and Write Operation [3].

DRAM	WRITE OPEERATION		READ OPERATION	
	Power (mw)	Delay (ns)	Power (mw)	Delay (ns)
1T	29 mw	6.9 ns	41.6 mw	9.2 ns
2T	31.2 mw	6.9 ns	61.1 mw	10.1 ns
3T	44.8 mw	5.8 ns	52.6 mw	6.1 ns
4T	58.6 mw	10.6 ns	71.6 mw	13.2 ns

S. Raju and K. Jeevan Reddy [4] present design and implementation of 8x8 DRAM memory array using 45nm technology. These proposed systems provide design of 8x8 DRAM memory array. This proposed system i.e. the 8x8 DRAM memory has been designed, implemented & analyzed in gpdk045 technology library using cadence tool. This system analyzes the average power consumption, write access time, read access time and retention time of 3T1D DRAM cell. This proposed array consumes 50.33uW power to write and read 1&0 at 1.1V power supply and gradually decreases with decreasing power supply.

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III. PROPOSED STRUCTURE

This section describes the proposed structure of DRAM cell using transmission gate. The main objective behind design of this cell is to provide write stability & to improve the performance. Fig 3 shows the schematic of DRAM cell using transmission gate. Here transmission gate is used as switch.

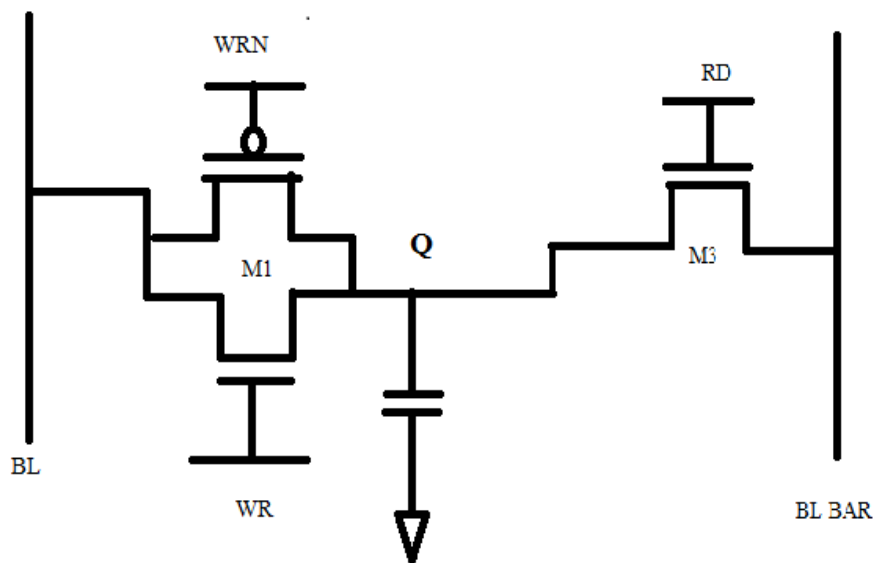


Fig 3 The schematic of DRAM cell using transmission gate

There are basically two operations i.e. read and write operation. During write operation, both the bit lines are at opposite voltages, that means if bit line BL is at high voltage then BLB at low voltage and vice versa. When WR becomes high and WRN becomes low this enables transmission gate and the charge on BL is stored in capacitor and data writes on output port Q.

During read operation the RD should be high; this enables the transistor M3, both bit line behaves as output, one of bit line starts discharging and that instant data is going to be read.

IV. SIMULATION RESULTS

The main objective of this work is to improve read stability of memory cell and to meet all challenges in designing of memory cell at nanoscale technology. All simulation have been performed on Tanner EDA tool version 13.0 using 22nm technology with input ranging from 0.4v to 1v.

a. POWER CONSUMPTION

Whenever the PMOS and NMOS transistors are in OFF state, the CMOS inverter is in stable state. No current flows through the power supply to ground. However, small amount of current flow through the OFF state transistor and it gives rise to, leakage power consumption, as shown in equation 1.

$$P=I_L \times VDD$$

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Sr. No.	Applied Voltage	Power Consumption	Discharge of Capacitance
1	0.4v	438.94pf	24.26mv
2	0.6v	340.07pf	20mv
3	0.8v	290.24pf	10mv
4	1v	128.65pf	10mv

b. READ STABILITY

Proposed system provides improved

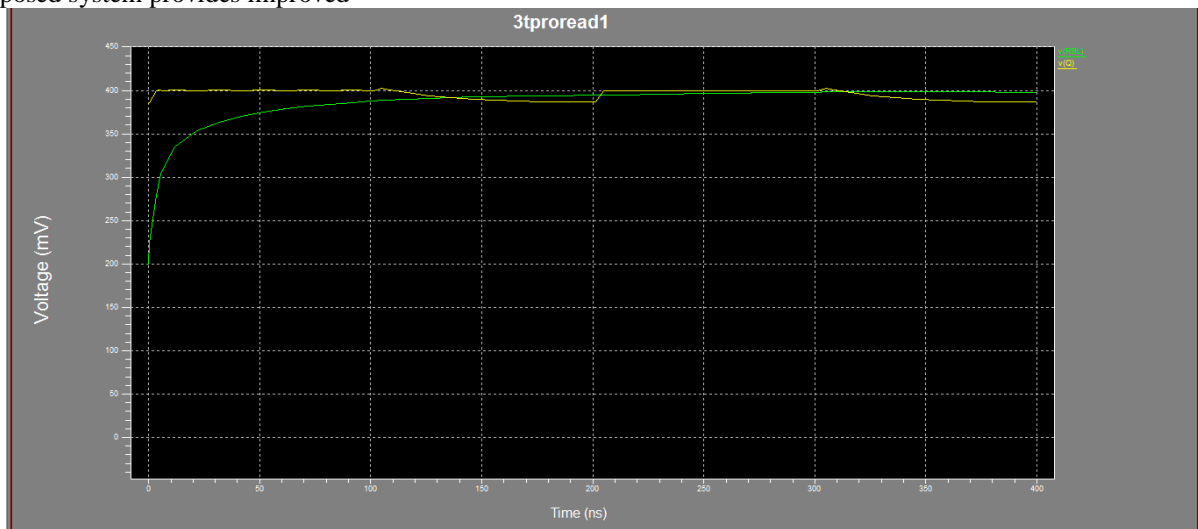


Fig.4 Read 1 of Proposed System.

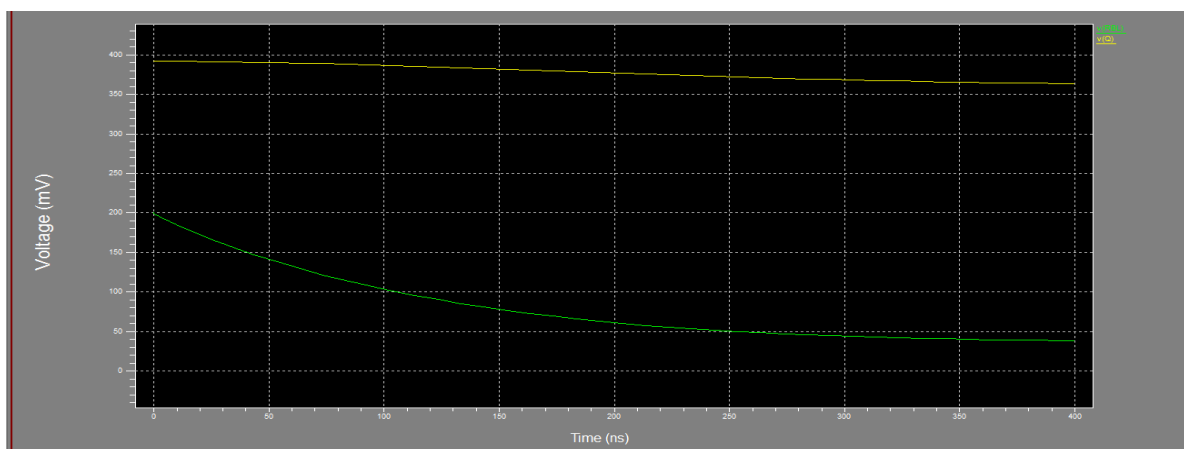


Fig.5 Read 1 of Existing System

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V. CONCLUSION

We have proposed a DRAM cell using transmission gate in which we present read/write operation at a range of operating supply voltage. In this paper it is observed that by using transmission gate instead of NMOS transistor in the circuit we can improve the read operation and also it has been observed that power consumption is decreased with increase in voltage. It can be considered that high performance and a lesser amount of power consumption as increase in working voltage at 22 nanometer technology in Tanner EDA tool.

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