

# Modified Vedic Multiplier Using Modified GDI Technique

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**ABSTRACT:** Nowadays, low power design has significant importance in digital VLSI Circuits. In this paper two new designs are proposed for the low power 4 bit modified Vedic Multiplier with less number of Transistors using the Urdhva Tiryagbhyam (UT) sutra .The topology used to reduce the power and the area is Modified GDI-MUX technique. These low power designs are realized in CADENCE VIRTUSO schematic tool.

**KEYWORDS:** Vedic multiplier, Urdhva Tiryakbhyam, Modified GDI (Gate Diffusion Input), Low power, Multiplexer (MUX).

## I. INTRODUCTION

This paper proposes low power modified Vedic multiplier architectures based on Vedic mathematics. The proposed 4 -bit topologies based on the *Urdhva Tiryakbhyam(UT)* (vertically and crosswise) [1] sutra of Vedic mathematics are realized using 45nm technology in Cadence Virtuoso Schematic tool. A 2T AND gate design, based on modified GDI-MUX , has been used in this work for generation of partial products instead of the 5T topology used in the previous work[1] . The adder chains used in the multiplier units are implemented using GDI-MUX topology, which comprise of 14T full adders and 6T half adders optimized for low power arithmetic. The use of such modified designs results in a smaller on chip silicon area requirement.

The rest of the paper is organised as follows. Section II provides a general overview UT sutra. Section III gives brief idea about modified Vedic multiplier. Section IV gives a description about Modified GDI circuit and the design of various circuits (AND,OR, Half adder and Full adder) using the new topology GDI-MUX. Section V summarizes the performance table and the result analysis. Section VI concludes the paper.

## II. UT SUTRA

Vedic mathematics provides effective computing methodologies for high speed arithmetic, only UT sutra has been discussed in this paper. Urdhva means vertically and Tiryakbhyam means crosswise. The use of UT sutra for multiplication operation reduces the latency of a multiplier unit by introducing parallel computing of partial products.

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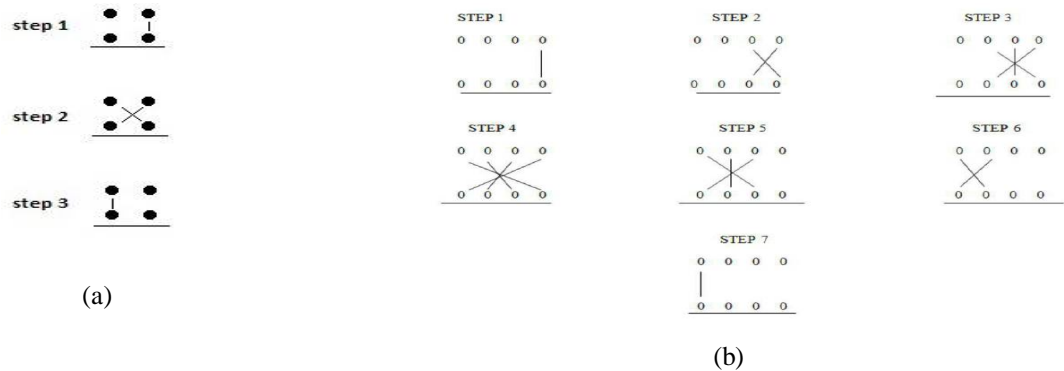


Fig.1. Line diagram of 2bit (a) and 4 bit multiplication (b)

### III. MODIFIED VEDIC MULTIPLIER

In a modified Vedic multiplier [3] the logic gates and logical expressions can be realised by using multiplexers. Here for a 4-bit Vedic multiplier it requires AND gates, half adder and full adders. The logical expressions of half adder can be implemented by AND gate and XOR for its carry and sum. Full adder requires AND gates, OR gate and XOR gates for its logic function. These basic gates (AND, XOR, OR) can be realized by using multiplexers.

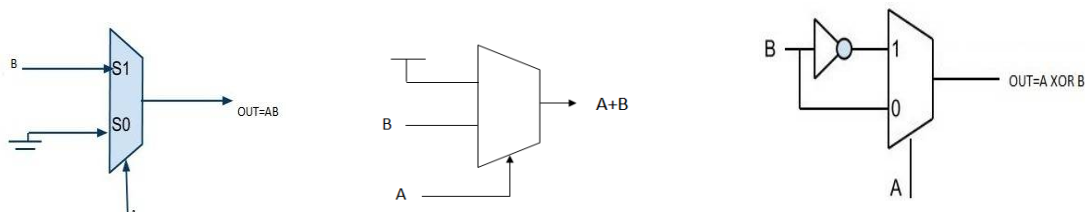


Fig2. AND, OR and XOR gate design using MUX

### IV. MODIFIED VEDIC MULTIPLIER WITH GDI TECHNIQUE

GDI structure is similar to basic CMOS inverter but instead of one input here it has three inputs such as one gate input (G), second input (P) is connected to source of PMOS and third (N) is connected to source of NMOS. By suitably choosing the values of G, P and N, it can produce various functions using the 2 transistor structure. The output of the GDI circuit is  $OUT = G'P + GN$ .

A single modified GDI [2] circuit is behaving like a 2x1 MUX. In the GDI circuit the gate input (G) act as the select line of the MUX and other two inputs such as P and N act as the inputs of the MUX. In the proposed design MUX is implemented as this modified GDI circuit. By suitably adjusting the value of three input GDI circuit, it can be able to produce different functions, which is shown in the following table.

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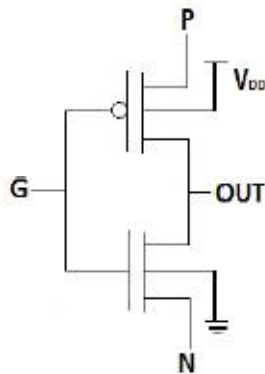


Fig3.Modified GDI circuit

FUNCTION	N	P	G	OUTPUT
INVERTER	0	1	A	A'
AND	B	0	A	AB
OR	1	B	A	A+B
MUX	C	B	A	A'B+AC
XOR	B'	B	A	A'B+AB'
XNOR	B	B'	A	AB+A'B'

Table1. Implementation of various functions using GDI

## A. AND, XOR, OR GATES USING GDI-MUX

Previous Work [1] AND Gate was Designed with 5T Transistors and XOR gate required 6T, but with GDI-MUX Technique [2] AND Gate and OR gate can be constructed with only 2 Transistors. Along with that XOR gate requires only 4T structure.

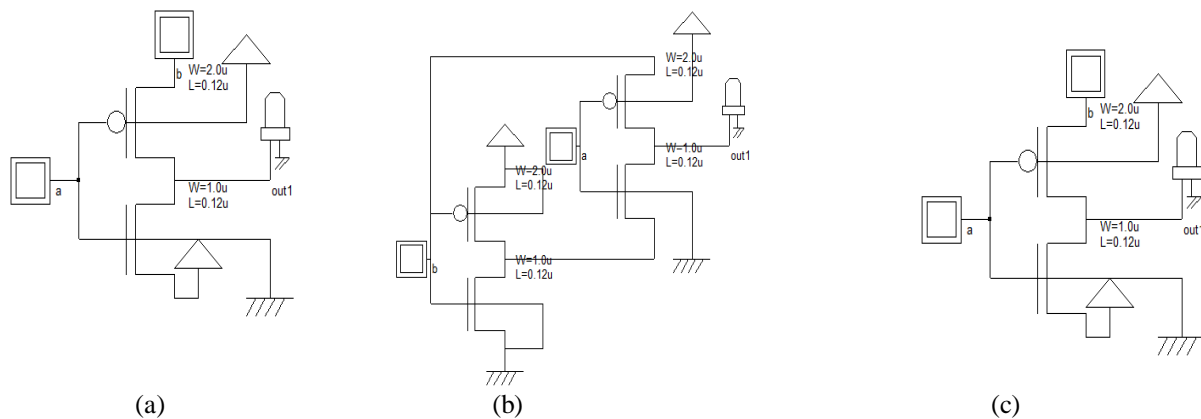


Fig4.(a)AND gate using MUX, (b) XOR gate using MUX, (c)OR gate using MUX

## B. HALF ADDER USING MUX

The half adder block used in this paper is a 6T design, whereas, the previous work [1] requires 9T structure that ensures high speed, low power and full swing arithmetic. This topology uses a 2T AND gate for carry generation, while, for the sum it need one 4T XOR gate

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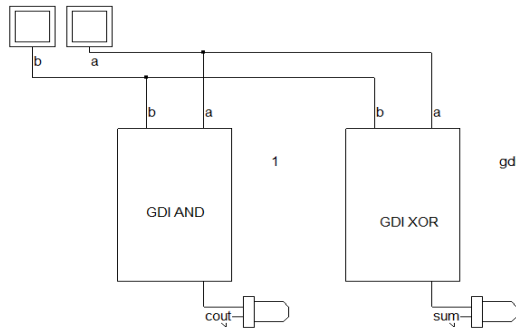


Fig7. Half adder using MUX

### C. FULL ADDER USING MUX

The full adder block used in this paper is a 14T design that ensures high speed, low power and full swing arithmetic. This topology uses a two 2T AND gate, one 2T OR gate and one 4T XOR gate for carry generation while the sum generation unit comprises of two 4T XOR gate. The compact design and smaller transistor count associated with this topology provides significant improvement in the performance of the adder chains embedded in the multiplier.

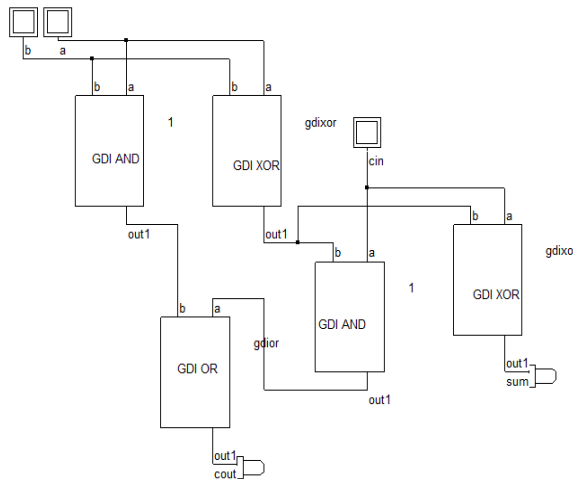


Fig8. Full adder using MUX

### D. VEDIC 2-BIT MULTIPLIER ARCHITECTURE

The UT based 2-bit Vedic multiplier [1] presented in this work comprises of four AND gates for partial product generation and two half adders to realize the required addition process. Here, all the partial products are simultaneously calculated through the 2T AND gates and that can add by passing through the 6T half adders. In total this circuit requires only 20 numbers of transistors, whereas, the existing circuit [1] has 42 transistors. So it shows a significant reduction in both power as well as area.

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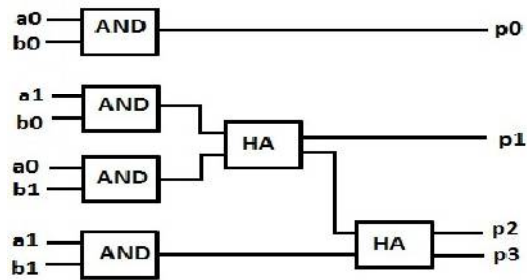


Fig9. Block diagram of Vedic 2 bit multiplier

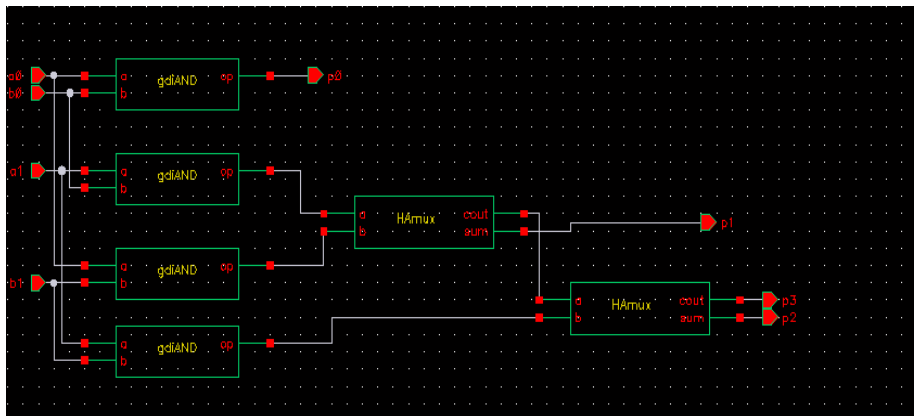


Fig10. Schematic diagram of Vedic 2 bit multiplier using MUX

## E. VEDIC 4-BIT MULTIPLIER ARCHITECTURE (DESIGN 1)

The Vedic 4-bit multiplier is realized using the UT sutra 4 bit multiplication technique[1]. All the partial products are simultaneously generated through sixteen 2TAND gates, which itself speed up the computation process. The partial products can be added with the help of several half adder (6T) and full adder (14T) arrangements and for merging the result, it is finally pass through a Ripple carry adder block. The corresponding topology is depicted in Fig. 11. Schematic implementation using GDI-MUX is illustrated in Figure. 12. In the 4x4 Multiplier existing Design1[1] requires 228 Transistors but our proposed Design1 requires 168 Transistors out of which it requires 16AND Gates (32 Transistors) 4 Half Adders (24 Transistors) and 8 full adders (112 Transistors).

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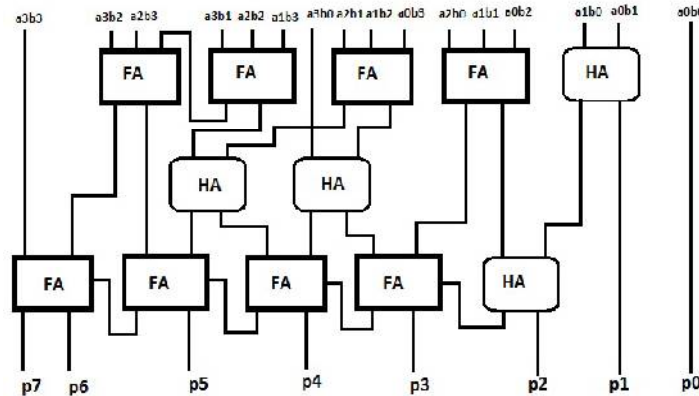


Fig11. Block diagram of Vedic 4 bit multiplier (Design1)

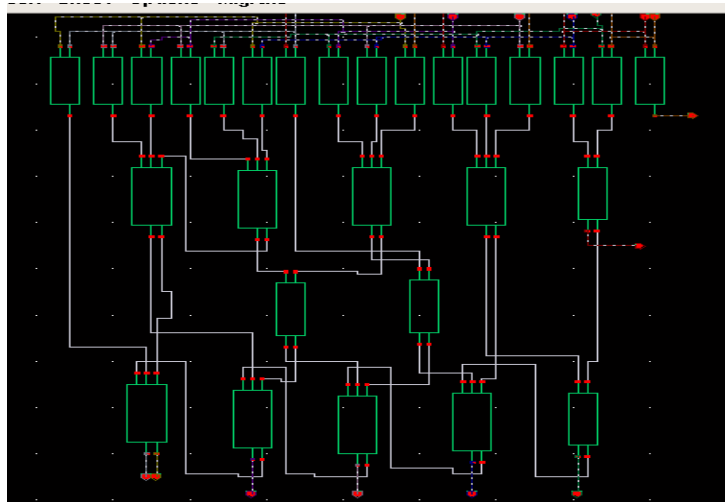


Fig12. Schematic diagram of Vedic 4 bit multiplier (Design1)

## F. VEDIC 4-BIT MULTIPLIER ARCHITECTURE (DESIGN 2)

Another method for realizing 4-bit binary multiplier is by using 2-bit multiplier as shown in Fig9. For Adding Partial products 2 blocks of Carry Save adders are used because these adders offer the fastest performance in comparison with any other adder circuit. In both carry save adder block two half adders and two full adders are used which can again reduce the power as well as the area of the circuit. Finally the result can be obtained by passing it through a ripple carry adder block. Existing Vedic Multiplier requires 286 Transistors but proposed Design2 contains only 208 Transistors. It requires four 2-bit Vedic Multipliers (80 T), seven full adders (98T) and five half adders(30T).

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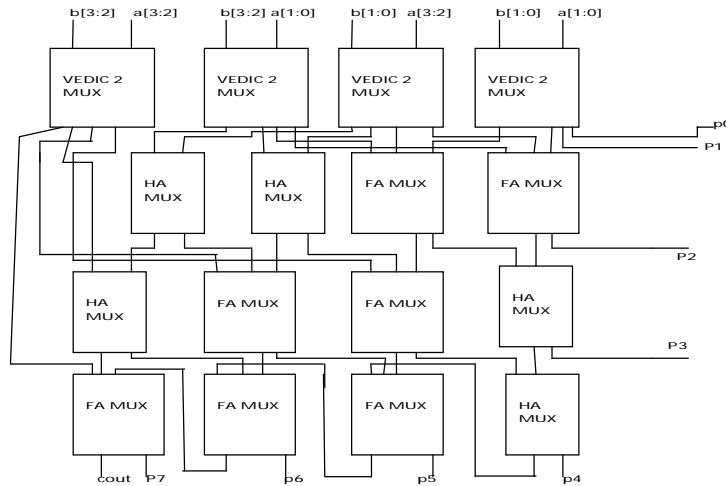


Fig13. Block diagram of Vedic 4 bit Multiplier (Design2)

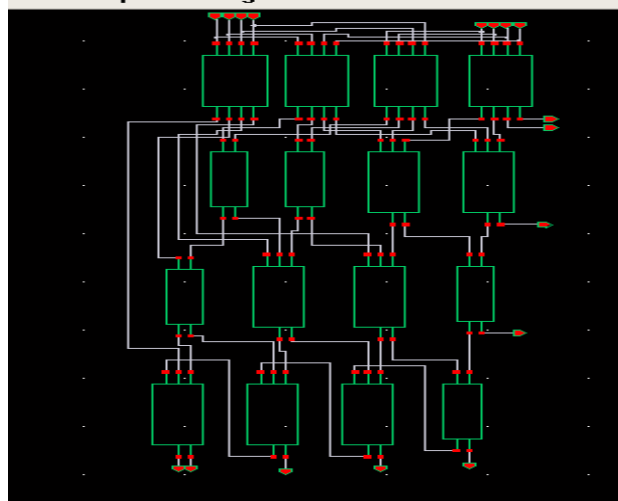


Fig14. Schematic diagram of Vedic 4 bit multiplier (Design2)

## v. RESULTS

Vedic Multipliers Designs are implemented in Cadence Virtuoso schematic tool. Power Consumption and Area (number transistors) were calculated. The table below shows the Power consumption and Area Comparison of Proposed Designs with the existing Vedic Multiplier Designs. In Modified 2bit Vedic Multiplier there is 97.7% reduction in Power Consumption and also the number of transistors get used to half of the existing topology. In Modified Vedic Multiplier (Design1) using Modified GDI there is 46.2% reduction in power Consumption occurs. Along with that in case of Modified Vedic Multiplier (Design2) the power gets declined to 72.9%.

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Multipliers	Existing System		Proposed System	
	Number of Transistors	Power	Number of Transistors	Power
2bit VEDIC Multiplier	42	0.0215	20	4.9215E-4
4 Bit multiplier 1	228	0.06227	168	0.03349
4 Bit VEDIC multiplier 2	286	0.0944	208	0.0255

Table2.Result Analysis

## VI. CONCLUSION

The paper presents new topologies for 4-bit multiplier based on UT sutra of Vedic mathematics. The topologies are realized using CADENCE VIRTUOSO schematic tool. The multiplier designs proposed in this paper demonstrate noticeable improvement in power consumption and significant reduction in number of transistors using Modified GDI-MUX Technique. A reduction in total on chip silicon area is also achieved by implementing the partial product generation unit with the help of 2T AND gates.

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