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64bit Multiplier Using Vedic Mathematics for DSP Applications

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ABSTRACT: The need of high speed processing is increasing day by day on account of recent computer applications. As the multiplication takes considerably more amount of time for its calculation, the computation time must be reduced to get speedy results. To obtain the speedy results, either computation time must be reduced or the pace of the coprocessor must be improved. In this paper we proposed an efficient 64 bit multiplication making use of VEDIC multiplier to expand the pace of operation as when compared with the existing algorithms. Architecture of Vedic multiplier with less number of gates and high speed specification is designed here. Synthesis of the Implementation of this multiplier has been done on Xilinx XST. In this paper Design of high speed MAC unit based on Vedic multiplier algorithm. Generally MAC useful application such as Digital signal processing like FFT transforms Convolution and correlation. MAC is hardware based module therefore first design of multiplier block and second one is adder block. In this paper to implementation 64bit MAC with reduces the delay and increase the speed of system. The coding done by VHDL and its synthesis and simulation on XILINX ISE.14.5 tool.

KEYWORDS: Vedic multiplier, adder, MAC, Digital Signal Processing, VHDL, FPGA

I.INTRODUCTION

Multiply accumulator consists of three main blocks, first one is multiplier, second one is adder and third one is Accumulator. Multiplier is main important block of MAC unit. It is used in arithmetic operation for multiplication. Multiplier main key role in DSP application. More number of bits size of multiplication it is very difficult to multiplication and more delay therefore the speed is decreases. To improve the performance of high speed MAC unit but to reduce delay. Different method for design MAC unit with help of various multiplication techniques such as booth multiplier, Wallace multiplier and Vedic multiplier. The main key to the proposed MAC unit is to enhance the performance of MAC using Vedic Multiplier and to compare the array, Booth and Wallace tree multiplier in terms of computation required to generate the partial products and add the generated partial products to get the final result of the multiplication.

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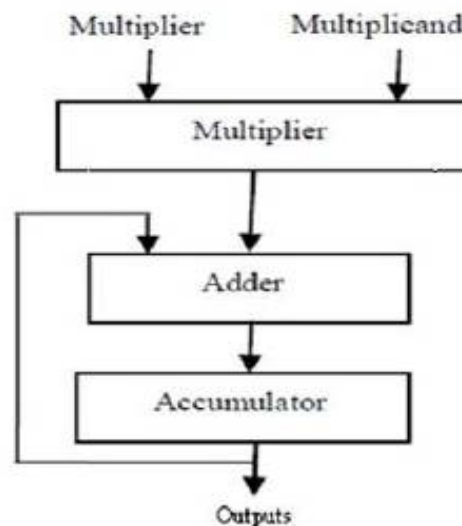


Fig.1: MAC Unit

The shown fig. 1 is a block diagram of MAC unit. The function of the MAC unit is given by the following equation $F = \sum A_i \times B_i$. The inputs for the MAC are fetched from memory location and fed to multiplier block of the MAC unit, which will perform the operation of multiplication and give the result to adder block which will accumulate the result and then will store the result into a memory location. That whole process is to be achieved in a single clock cycle. Multiplication is an important function in arithmetic operation. Multiplication based operation such as multiply and accumulate unit (MAC) and Arithmetic and logic unit (ALU).

II.LITERATURE SURVEY

AlJuffri et.al [01] proposed a robust method for improving the performance of FIR filter by designing the efficient multiplier. This paper made use of Vedic multiplier and Wallace tree for the implementation of parallel and sequential micro programmed FIR filter architecture. There are different types of multiplication algorithms and each algorithm involves three major steps, partial product generation, partial product reduction, and final summation. Some basic multiplication algorithms are serial multiplication [2], parallel multiplication and serial-parallel multiplication. Serial multiplication is well known for its less hardware and less speed of operation. Parallel multiplication algorithm works with high speed and its speed depends on number of partial products to be added [3]. There are different types of parallel multiplication like array multiplier, tree multiplier, and Vedic multiplier. Array multipliers can be categorized into Braun array multiplier. [4]The proposed algorithm is design of Multiplier using Vedic multiplier method and its application of Digital Signal processing.[1] $N \times N$ multiplier design using four $N/2$ bit multiplier, two N -bit full adder, one half adder and $N/2$ bit full adder to add the sum and carry of half adder.[2] 16×16 array of array Multiplier using Vedic multiplier this structure is hierarchical design algorithm is urdhva triyagbhyam sutra on Vedic mathematics.[5]According to Anvesh Kumar, Ashish Raman, they gave the idea that Vedic sutras should be used to design the ALU.They suggest two sutras for the designing ofALU, NikhilamSutra, Urdhva triyakbyham Sutra. Multiply Accumulate block is extensible used here. Multiplication algorithms implemented using Verilog HDL. The multiplication algorithm is applying here only for 2 digits and 3 digit. The result is simulated using modalism simulator.

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III.METHODOLOGY

1. Vedic Mathematics

Vedic mathematics is the ancient system used for doing fast calculations in the mathematics. It is used in India from an ancient time. It is the gift for fast processing of mathematics calculations to this world from ancient stages. By using Vedic mathematics for computation of algorithms of the coprocessor will reduce the computational time, complexity, power, area, etc. Vedic mathematics is based on the 16 sutras of Vedas, which are described below. This system is simpler and faster than the modern mathematics. That's why we must be thankful to Jagadguru Swami Sri BharatiKrishna TirthajiMaharaja who introduce Vedic mathematics and acknowledge the work of various people on Vedic mathematics. There are different sutras of multiplication followed in vedic arithmetic [2]. The proposed work made use of Urdhva-Tiryaghbyam sutra. This is the multiplication formula applied to all the types of multiplication. The special property of this sutra is that it partially generates product and also performs addition simultaneously at the same time. This approach is more efficient in binary multiplication.

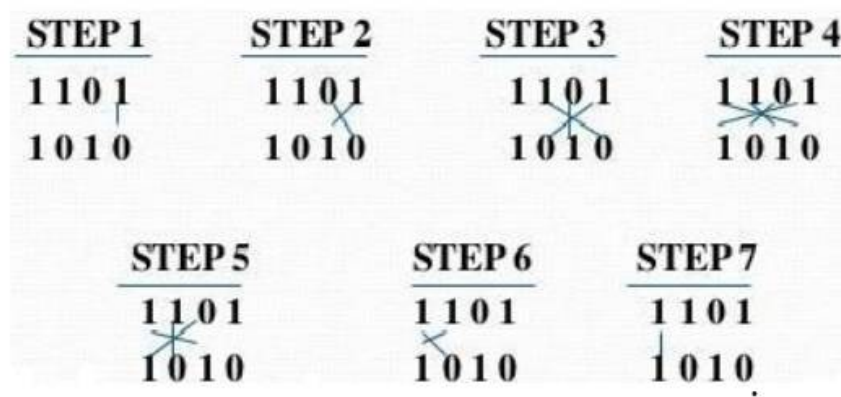


Fig.1: A Example for Urdhva-Tiryaghbyam sutra using binary multiplication

A. Multiplication on Decimal Numbers Using Urdhava Tiryakbhyam

The pictorial description of multiplication on 3 digit decimal numbers is shown in Fig1. The carry generated in each addition is propagated to the next most significant digits.

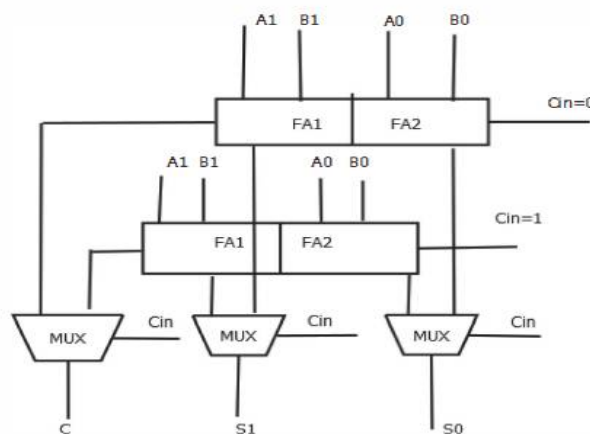


Fig.2: Architecture of Two bit carry select adder

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B. Algorithm for N-bit Multiplication based on Urdhava Tirykbhyam.

This section describes detailed method for the multiplication of two N-bit numbers. The multiplications of two N-bit numbers result in a 2N bit product. By considering two N-bit numbers A and B the algorithm steps can be described as

Step 1: Divide the N-bit numbers in to two groups, consisting of $O-(N/2-1)$ bits and $N/2$ to $N-1$ bits respectively. The first part gives the LSB of the number and second part is MSB.

Step2: Represent the complete number as $AH-AL$ and $BH-BL$, where AH , BH represent MSBs and AL , BL represent LSBs of two numbers A and B.

Step3: Use Urdhva-Tiryakbhyam sutra to generate the partial product.

Step4: The individual partial products can be obtained by portioning each higher order bit to lower order of two or four bit and then applying two or four bit Vedic multiplication to get the final result

By adopting this algorithm we can generate 8, 16, 32, 64 bit multipliers, in which 4bit Vedic multiplier works as the basic building block.

2.2x2 Bit Vedic Multiplier

Consider two 2 bit binary numbers which are represented as below to produce a 4 bit product.

$a[1:0]: a_1a_0$
 $b[1:0]: b_1b_0$

By applying Urdhva-Tiryagbhyam method to a and b, the product of a_0b_0 , a_1b_0 , a_0b_1 and a_1b_1 is found. Now a_0b_0 appears as the LSB (s_0) of final result. a_0b_1 and a_1b_0 uses half adder and the result is s_1 as in Figure-6. The obtained carry (c_1) and a_1b_1 is sent through another half adder (Alex et al 2004). The resulting bit is s_2 and its carry (c_2) is the left-most bit of the final result.

3. Design of 64x64 Bit Multiplier

Number of bit width increase to increase partial products therefore its difficulty work of multiplication. here block diagram of 64x64 bit multiplier shown in fig.8 the design of 64bit Vedic multiplier, first design 4 block 32x32bit data inputs and we get the 128 bit output data, second design of adder because to reduce the partial products of multiplication The proposed sixty four bit Vedic multiplier can be implemented by using four thirty two bit Vedic multiplier as given Fig7. Through modular approach thirty two bit Vedic multiplier can be realized by taking four bit Vedic multiplier as the basic element. The input to the sixty four bit Vedic multiplier is given as two thirty two bit pair and they produce an output of one twenty eight bit. Sixty four bit fast carry select adder is used as summation element and it can be implemented through modular approach

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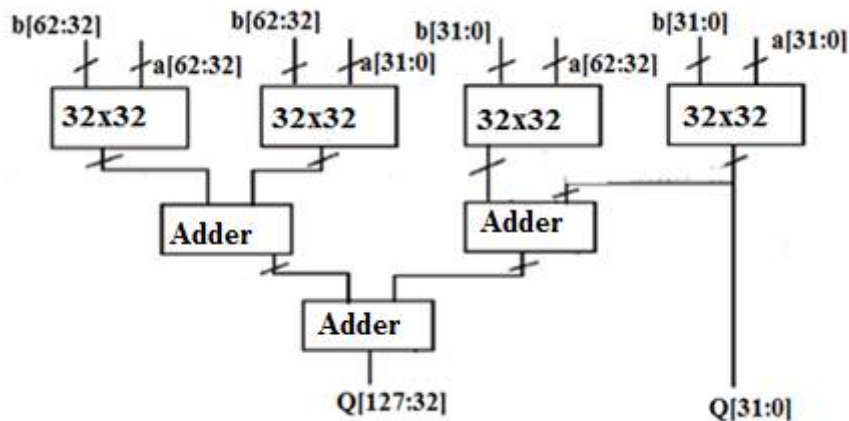


Fig.3: Block Diagram of 32x32 bit Vedic multiplier

IV.RESULT

The proposed 64 bit Vedic Multiplier is coded using Xilinx 14.1 ISE and simulated using ISim (0.61xd) simulator. The simulated experimental result is shown in the figure below.

Case:-

Input A = 1355732153214984

Input B = 6574516874352146

Output S = 07a97f4a3dd0d94cee5eb3a80de81e18

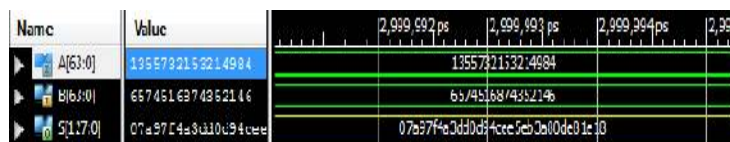


Fig.3: Result of 64x64 bit Vedic multiplier

V.CONCLUSION

This paper presents the implementation of Vedic multiplier with the use of Urdhva trikyham sutra, due to which carry will not propagated up to higher level, so propagation delay for higher number multiplication will reduce. So the speed of the multiplier will also increase. According to the above discussion it is most important issue to increase the speed and decrease the area of the multiplier, as it is the most important element in any of the processor or system. An implementation of Vedic mathematic techniques in designing of multiplier greatly improves the system performance and can be extended to reconfigurable architecture. A 32 bit modified multiplier is designed. The 64 bit multiplier is realized using four 32 bit Vedic multipliers and two modified carry save adder. Vedic arithmetic deals with themes of arithmetic reminiscent of normal mathematics. The proposed architecture proves to be incredibly fast and accurate.

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