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Differential Voltage Current Conveyor Based Clockwise and Counter Clockwise -Hysteresis Mode Bistable Multivibrator Implementation

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ABSTRACT: This paper presents a Dual hysteresis mode Flip-flop multivibrator circuit, which is composed of only one Differential voltage current conveyor (DVCC) as the active element. Projected Dual hysteresis mode Flip-flop multivibrator Circuit consists of a DVCC, two resistors R1 and R2, and a double pole double throw dual in- line package (DPDT DIP) mechanical type switch. Top and bottom saturation levels of the Flip-flop multivibrator can be set using passive components. Real structure in design of projected model describes operation of the circuit Is-Spice is the simulation software to simulate the model. Commercially available ICs AD844AN and passive elements are required for circuit implementation. Effectivity of the projected circuit is examined as measured and simulation results well agree with hypothetical result. Simulation and measurement results of Vo–Vin transfer characteristic curves for clockwise and counter clockwise mode with an operating frequency of f=1 kHz are shown. It is observed that the threshold voltages for the simulation and measurement results are close to the design values VTH=5 V, VTL= -5 V, and the projected flip-flop multivibrator circuit is capable of fulfilling the dual hysteresis operation within the same design criteria.

KEYWORDS: Differential voltage current conveyor, Flip-flop multivibrator, clockwise and counter clockwise hysteresis approach, Current conveyor, Positive feedback.

I. INTRODUCTION

Flip-flop multivibrator has wide functions in the field of processing of electrocardiogram signal (ECG), measurement systems, instrumentation, and communication schemes where typical signals like square, triangular and pulse is analyzed using Flip-flop multivibrator [1] – [7]. In the traditional structure, Flip-flop circuit consists of an operational amplifier (OPA) and two resistors but after inclusion of current conveyor, current-mode method of signal processing becomes more advantageous to fabrication of analog circuits for high presentation and useful adaptability. In OPA based design, a major disadvantage is the variation of output levels with the change of threshold voltage. Current conveyor of second generation (CCII) based design having one CCII together with three external resistors is also used earlier. A major drawback of previous described circuit is the absence of dual hysteresis mode within the same topology. Due to various disadvantages of previous popular structure, the proposed model having only one DVCC, double pole double throw dual in-line package mechanical switch and two resistors provides dual hysteresis procedures is focused as given in Table I.

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Table 1. Comparisons between different Flip-Flop multivibrator structures

STRUCTURE	ELEMENTS	PASSIVE ELEMENTS TYPE	ELECTRONICALLY ADJUSTABLE	HYSTERESIS PROCEDURE	MAXIMUM OPERATING FREQUENCY
Operational amplifier build-in	[1]Operational amplifier =1 [2] Resistor = 2	Atleast one earthed	No	Single	Tens of KHz
Second generation current conveyor (CCII)	[1] CCII = 1 [2] Resistor = 3	Atleast one earthed	No	Single	Hundreds of KHz
Differential voltage current conveyor (DVCC)	[1] DVCC =1 [2] Resistor = 2 [3] DPDT DIP switch = 1	Atleast one earthed	Yes	Dual	Hundreds of KHz

Aspects of the projected models are as follows:

- Quantity of devices applies to propose design is more or less same.
- Resistors are shorted to ground to achieve benefits of Integrated Circuit manufacturing procedures.
- Achieved functioning frequency is greater compare to Operational Amplifier constructed design.
- Using same topology uniqueness of dual hysteresis operation is obtained.
- Possibility of variation with temperature is fewer.
- Relevancy of entirely DVCC constructed design enhances.
- Higher and lower threshold voltages are electronically adjustable.

In Section 2, basic concept and construction of DVCC is emphasized. Then working ideology of bistable multivibrator model is described and associated expressions are given. Also non-ideality and parasitic properties of the planned circuit is analyzed in third Section .In fourth Section, a useful fabrication technique and parametric criteria is introduced. Later, laboratory examinations are performed on the fabricated model. Operation of planned model is checked via simulation software and laboratory examination results. Programme and laboratory examined outputs match with hypothetical concepts. Last portion consists of conclusion.

II. CIRCUIT DELIBERATIONS AND FUNCTIONING PRINCIPLE

A. Primary Concept and Implementation of DVCC

DVCC is suitable in continuous signal processing areas due to its large input resistance voltage terminals and large output resistance current terminals. Circuit symbol of DVCC with four terminals is shown in Figure 1.

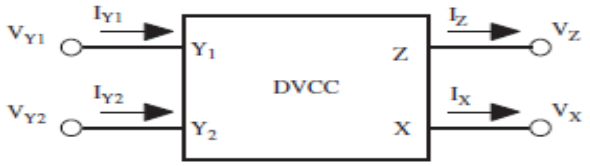

Fig. 1. Circuit symbol of DVCC

X terminal voltage drop (V_X) shows the variance of two Y terminals voltage drops, V_{Y1} and V_{Y2}, and X and Z terminal current propagation,I_X and I_Z occurs in the same manner. DVCC has zero X terminal input impedance and infinite impedances at two Y terminals; hence I_{Y1} and I_{Y2} both are zero. Voltage drop at Z terminal is denoted as V_Z .From above characteristics, V-I relations of DVCC is articulated in equation (1).

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$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{pmatrix} \quad (1)$$

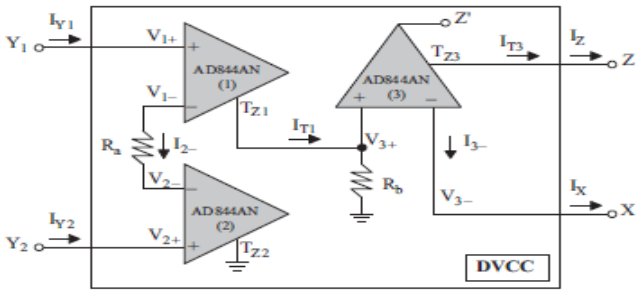

Fig. 2. Implementation of DVCC using IC844AN

Figure 2. demonstrates a hands-on assembly of DVCC consuming simply available ICAD844AN. AD844AN is a special type of OPA due to virtually short inverting and non-inverting inputs. Current propagation through inverting terminal and T_Z terminal of AD844AN occurs in the same manner. Due to presence of very high impedance at Non-inverting input terminals of the first two AD844ANs which results I_{Y1} and I_{Y2} equivalent to zero. Connection between T_z terminal and non-inverting terminal of first and third IC AD844ANs via grounded resistor R_b provides the variance of two Y terminals voltage drops,V_{Y1} and V_{Y2}, and X and Z terminal current propagation,I_X and I_Z occurs in the same manner. Figure 2. depicts the following relationships between voltage and current:

$$V_{Y1} = V_{1+} = V_{1-} \quad (2)$$

$$V_{Y2} = V_{2+} = V_{2-} \quad (3)$$

$$I_{Y1} = I_{Y2} = 0 \quad (4)$$

$$I_{TI} = I_{2-} = \frac{V_{1-} - V_{2-}}{R_a} = \frac{V_{Y1} - V_{Y2}}{R_a} \quad (5)$$

$$I_X = I_{3-} = I_{T3} = I_Z \quad (6)$$

$$V_X = V_{3-} = V_{3+} = I_{T1} R_b = \frac{R_b}{R_a}(V_{Y1} - V_{Y2}) \quad (7)$$

V_{3+} and V_{3-} are non-inverting and inverting voltage drop of third ICAD844AN, I_{T1} is current flowing through T_Z terminal of first ICAD844AN. Therefore, by adjusting resistors R_a=R_b, V-I relationship of idyllic DVCC is achieved.

B. Proposed DVCC Based Model Discussions

Figure 3. depicts projected DVCC-based flip-flop multivibrator consists of a DVCC, two resistors R_1 and R_2, and a DPDT DIP mechanical type switch. An oscillator [8] supplies triangular waveform as input signal V_{in}. Positive feedback [9] in projected model is obtained by connecting Y_1–Z in conjunction with shorted to ground impedance R_2 . DVCC runs between upper and lower saturation levels Vo^+ and Vo^-.

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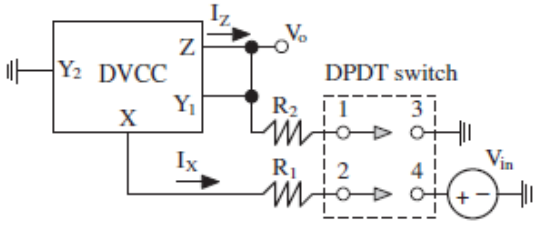

Fig. 3. DVCC-based flip-flop multivibrator controlled by switch

Figure 4 (a) shows V_o-V_{in} transfer characteristics of the projected model during Clockwise (CW) mode operation where terminals 1 and 3 and terminals 2 and 4 of DPDT DIP switch are shorted. For this mode, equations of current flowing through X and Z terminal I_x and I_z can be written as:

$$I_X = \frac{V_O - V_{in}}{R_1} \tag{8}$$

$$I_Z = \frac{V_O}{R_2} \tag{9}$$

At first output voltage Vo is at upper saturation level Vo^+ and input signal V_{in} is absent in the circuit, that is V_{in}=0. Let R_1 is smaller than R_2. From equation (8) and (9), it is clear that current I_X will be higher than I_Z. Thus, Vo remains at top saturation level Vo^+ from starting. When input signal V_{in} is applied in the circuit current I_X diminishes gradually and Vo switches from Vo^+ to bottom saturation level V_o^- as shown in path 1 of Figure 4 (a). When input signal V_{in} diminishes from zero, current I_X increases until I_X is larger than I_Z. Then, Vo switches from Vo^- to Vo^+ as shown in path 2 of Figure 4 (a).

Thus, lower and higher threshold voltages, V_{TL} and V_{TH}, can be obtained for the situation when $I_X = I_Z$. Expressions of V_{TH} and V_{TL} in CW mode are given in equation (10) and (11):

$$V_{TH} = V_O^+ (1 - \frac{R_1}{R_2}) \tag{10}$$

$$V_{TL} = V_O^- (1 - \frac{R_1}{R_2}) \tag{11}$$

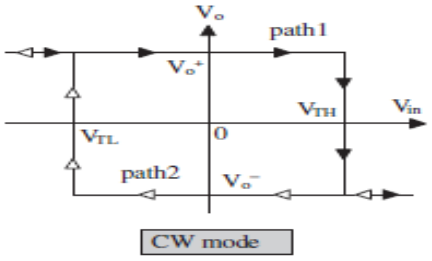

Fig. 4 (a). $Vo–V_{in}$ transfer nature of DVCC-based flip-flop multivibrator controlled by switch for CW manner approach

Figure 4 (b) shows V_O-V_{in} transfer characteristics of the projected model during Counter Clockwise (CCW) mode operation where terminals 1 and 4 and terminals 2 and 3 of DPDT DIP switch are shorted. For this mode, equations of I_x and I_z can be written as:

$$I_Z = \frac{V_O - V_{in}}{R_2} \tag{12}$$

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$$I_X = \frac{V_O}{R_1} \tag{13}$$

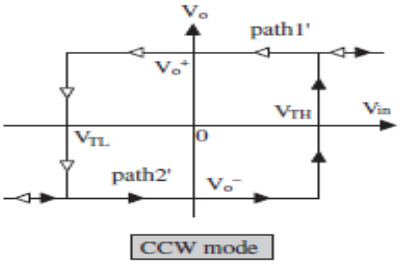

Fig. 4 (b).Vo–V_{in} transfer nature of DVCC-based flip-flop multivibrator controlled by switch for CCW manner approach

Let resistor R_1 is smaller than R_2. From (12) and (13), it is clear that current I_X will be higher than I_Z. Thus, Vo remains at the top saturation level Vo^+ from starting refer to path 1' of Figure 4 (b). When input signal V_{in} diminishes from zero, current I_Z increases. Once I_Z is larger than I_X, Vo switches from Vo^+ to Vo^-. Hence lower threshold voltage V_{TL} is obtained. In path 2', V_{in} is lower than V_{TH} and Vo is at Vo^-. Once I_Z is more negative than I_X, output level switches from Vo^- to Vo^+. Hence upper threshold voltage V_{TH} is obtained. Expressions of V_{TH} and V_{TL} in CCW mode derived from (12) and (13) are given in (14) and (15):

$$V_{TH} = V_O^+ \left(\frac{R_2}{R_1} - 1\right) \tag{14}$$

$$V_{TL} = V_O^- \left(\frac{R_2}{R_1} - 1\right) \tag{15}$$

III. REAL AND PARASITIC PROPERTIES EXPLANATIONS

Using IC AD844AN [10] Second generation current conveyor in positive mode cascaded with buffering voltage having inbuilt parasitic impedances is obtained according to the datasheet. Several non-idealities, like parasitic impedances and real gain concepts are emphasized here. A real structure of used DVCC based circuit model in Figure 5, is given where Rx, Ry, and Rz acting as terminal parasitic resistances. Parasitic resistance Rx is approximately several tens of ohms, but Ry and Rz are approximately several mega-ohms. α is considered as non-ideal voltage gain. According to the datasheet of AD844AN the typical data of α gain = 0.99, β gain =0.98, Rx=50Ω, Ry=10 M Ω, and Rz=3MΩ are considered.

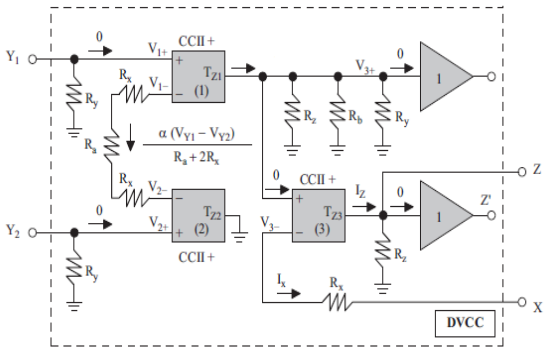

Fig. 5. Real structure of used DVCC based circuit model

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IV. FABRICATION CRITERIA AND EXAMINED OUTPUTS

A. Fabrication Techniques and Parametric Criteria

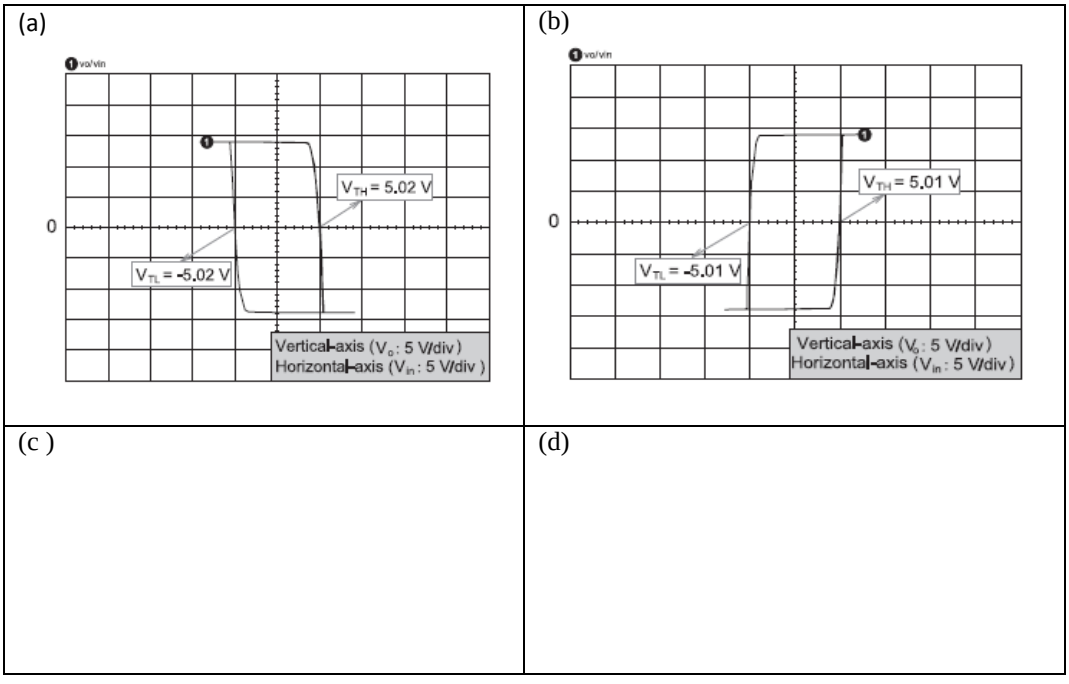
Minimization of the chance of parasitic and real gain effects of the proposed model, the criteria that Ra>>2Rx, R_1>>Rx, R_b<< (Rz//Ry), R_2<< (Rz//Ry) must be maintained in the fabrication techniques. Parasitic resistance Rx is approximately several tens of ohms, but Ry and Rz are approximately several mega-ohm range.

Thus the chosen values for resistors R_a, R_b, R_1, and R_2 range from few kilo-ohms to few hundreds of kilo-ohms. Fabrication criteria are such that R_1 must be smaller than R_2. DVCC fabricated with easily accessible ICs is able to rise above the issue of loading effect even in the absence of voltage buffer. For implementation and checking purpose, easily accessible ICs AD844AN and passive components are used to check viability of projected model.

B. Simulated and Examined Outputs

Laboratory examination is performed by using easily accessible AD844AN ICs, two resistors and a DPDT DIP mechanical type switch to obtain projected design. To simulate real structure as given in Figure 5 Spice is the simulation software. Supply voltages of ±15 V with saturation levels **Vo+= Vo-= 14 V** is maintained for circuit simulations and experiments. External function generator provides applied triggering signal V_{trg}. According to the datasheet of AD844AN the typical data of α gain = 0.99, β gain =0.98, Rx=50Ω, Ry=10 M Ω, and Rz=3MΩ are considered to satisfy the conditions: R_b=10 k Ω <<Rz/Ry=2.3 M Ω and Ra=9.4 k Ω<< 2Rx=100 Ω. During Clockwise mode operation, the lower and higher threshold voltages are considered as V_{TH}=5 V and V_{TL}= -5 V. Hence, a resistance ratio[11] of R_1/R_2=0.64 is achieved. Arbitrarily R_2 is considered as 20 k Ω (R_2=20 kΩ <<Rz||Ry=2.3 M Ω), and hence R_1 as 12.8 k Ω (R_1=12.8 k Ω >>Rx=50 Ω). For counter clockwise mode operation, a resistance ratio R_2/R_1=1.35 is chosen, depending upon the said design techniques. Thus, R_2 is considered as 20 k Ω (R_2=20 kΩ <<Rz||Ry=2.3 M Ω), and hence R_1 as 14.8 k Ω (R_1=14.8 k Ω >>Rx=50 Ω).

Figure 6(a)-(d) shows the simulation and measurement results of Vo–Vin transfer characteristic curves for CW and CCW mode operations with an operating frequency of f=1 kHz. From Figure 6(a)-(d), it is shown that the threshold voltages for the simulation and measurement results are close to the design values V_{TH}=5 V, V_{TL}= -5 V, and the projected flip-flop multivibrator circuit is capable of fulfilling the dual hysteresis operation within the same design criteria.



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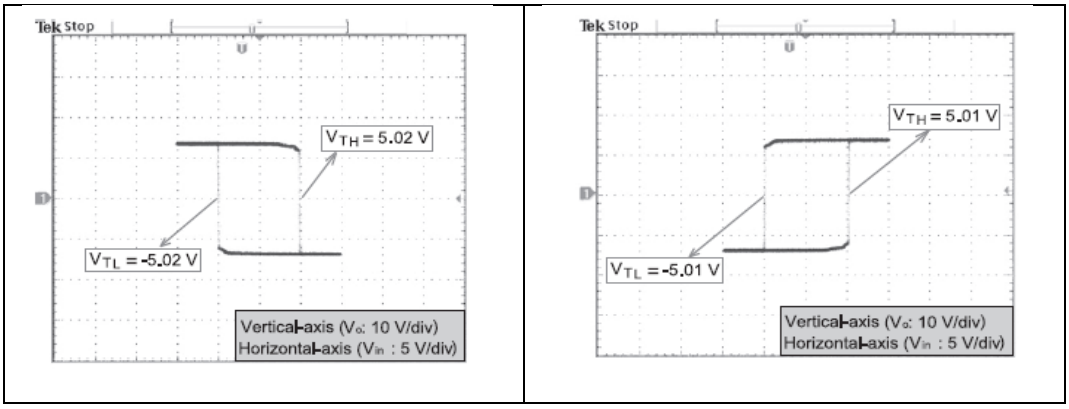

Fig. 6. Transfer characteristic with an operating frequency of f=1 kHz (a) Simulation result for Clockwise mode (b) Simulation result for Counter Clockwise mode (c) Measurement result for Clockwise mode(d) Measurement result for Counter Clockwise mode

V. CONCLUSION

In this paper, the projected bistable multivibrator model consists of only one DVCC and three resistors and one DPDT DIP mechanical switch. The projected flip-flop multivibrator circuit is able to fulfill the dual hysteresis action surrounded by alike design criteria. Effectiveness of recommended design is scrutinized due to satisfactory results of programme and experiment with theoretical results. The expected design affords new presentation for the DVCC founded systems. DVCC has extensive presentations in the area of communication systems, signal processing field specially processing of electrocardiogram signal [12-13] (ECG), instrumentation, and measurement systems.

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