

# Performance Analysis of a Low Voltage Power Efficient Dynamic Comparator

Sweta Snehi<sup>1</sup>, Ashwani Kumar<sup>2</sup>

P.G. Student, Department of Electronics and Communication Engineering, IGDTUW, Kashmere Gate, Delhi, India<sup>1</sup>

Professor, Department of Electronics and Communication Engineering, IGDTUW, Kashmere Gate, Delhi, India<sup>2</sup>

**ABSTRACT:** Analog to Digital Converters are essential for recovering digital signals from analog signals as processing of digital signals is found to be much easier and safe for transmission of information. This makes an ADC essential for applications such as wireless communication and signal processing. In today's semiconductor industry, priority is laid upon designing low-power circuits that can work at lower supply voltages. For this many low power techniques have been investigated. Used as a fundamental block in most ADC architectures, comparators with low-power and reduced delay are essential for faster operation of ADCs. In this paper, a dynamic comparator has been proposed that meets the requirement of high-speed and low-power without any added complexity. A comparative analysis has been presented in terms of various parameters that include power, delay, energy, power-delay product and kickback noise. The simulation is carried out in 0.18um CMOS technology at 0.8V supply using Cadence Virtuoso design environment.

**KEYWORDS:** Conventional dynamic comparator, Double tail dynamic comparator, High-speed ADCs, Low power, Kickback noise.

## I. INTRODUCTION

In today's VLSI industry, millions of transistors are placed on a single chip. This leads to increased power dissipation producing unwanted heat in the circuits. For cooling down of the chip, extra circuits must be incorporated that makes it expensive and denser. The most crucial task in today's VLSI industry is to reduce this power consumption and design circuits for higher speed of operations. To meet the requirement of power and speed, supply voltage is scaled down with each technology. This requires that the threshold voltage be scaled down with the same pace. But this is not achieved and a limitation is put on scaling down the supply voltage. Analog to Digital Converters (ADCs) employ comparators as their basic building blocks. Thus designing a comparator that meets the requirement of low-power and high-speed and can work at the lower supply voltages has become essential. For high speed operation of ADCs like Flash ADC, comparators with lower power consumption and working at higher speed is required. For this purpose dynamic comparators or clocked comparators are utilized. Positive feedback or latch regeneration process enhances the performances of comparator in terms of power and operation speed and are widely used in designing high-speed ADCs [2].

Comparator is an electronic device with two input terminals. Either voltage or current is provided at its input terminals. It compares the voltage or current values present at its input terminals and produces an output indicating which one among the two inputs is greater. The comparator that compares currents at its input is a current comparator and the one that compares voltages is a voltage comparator. In an ADC, the comparator is fed with sampled signal which then gives the equivalent digital output of the corresponding sampled signal.

The ideal voltage characteristic of comparator is shown in fig. 2 (b). If the input difference voltage ( $V_1 - V_2$ ) is positive, the output  $V_{out}$  is at high logic level i.e., at logic 1 and if it is negative, the output is at logic 0.

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Vol. 6, Issue 6, June 2017

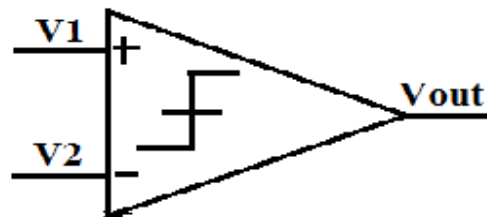


Fig. 1. Symbol of a comparator

CMOS dynamic regenerative comparators are widely known for their fast-speed, low power, high input impedance and rail to rail output swing. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time [2].

In this paper a dynamic comparator with much reduced power consumption and higher speed is proposed. The simulation is done using Cadence Virtuoso tool in GPDK 180nm technology. The kickback noise of the comparator is also calculated and it is found that the value is reduced for the proposed comparator.

The rest of this paper is arranged as follows. Section II presents schematic and operation of dynamic regenerative comparators. The proposed comparator is presented in section III. Section IV describes the Kickback noise and its schematic for calculation. Simulations and results are presented in section V. Section VI addresses the conclusion.

## II. DYNAMIC REGENERATIVE COMPARATORS

The latch regeneration due to the cross-coupled inverters generates positive feedback forcing fast decision making in the circuit. A clock regenerative comparator is a circuit which brings out decision according to the input signal which is either high or low at every clock cycle [1].

### A. Conventional Dynamic Comparator (Single Tail Comparator):

The schematic of conventional dynamic comparator is shown in fig. 3 [9]. The advantage of this structure is rail to rail output swing, no static power consumption, high input impedance and less affected by noise [4]. The drawback of this circuit is requirement of larger number of transistors due to several stacked transistors makes the circuit larger.. This also causes larger delay. A larger tail current is required for fast regeneration in the latch [3].

The operation of conventional dynamic comparator can be divided into two phases, reset phase and decision-making phase. In reset phase, when CLK=0, the tail transistor, NM0 turns off and reset transistors, PM0 and PM3 turn on. The output nodes Outn and Outp are then charged to VDD. A valid logic level is thus obtained during reset phase defining a start condition. In decision-making phase (comparison phase), when CLK=VDD, the tail transistor, NM0 turns on and reset transistors PM0 and PM3 turn off. The output nodes that have been already charged to a definite value equivalent to logic 1 begin to discharge with different rate of discharge. The rate of discharge depends upon the corresponding input voltages, INN and INP. If  $V_{INN} > V_{INP}$ , outn discharges quicker than outn. When the voltage at Outp reaches to a value equal to  $V_{DD}-|V_{thp}|$  before Outn, the corresponding pMOS transistor PM turns on. This will charge the output node, Outn to VDD which will in turn make the transistor NM4 to turn on and thus discharge the output node Outp to ground. This process is the latch regeneration process caused by the back-to-back connected inverters (PM1, NM3 and PM2, NM4) [4].

The delay of conventional comparator comprises of two delays, first one being the capacitive discharging delay of load capacitance and the second one being the latch regeneration delay [1]. Threshold voltage and load capacitance mainly affect the discharge delay while supply voltage and load capacitance affect the regeneration delay.

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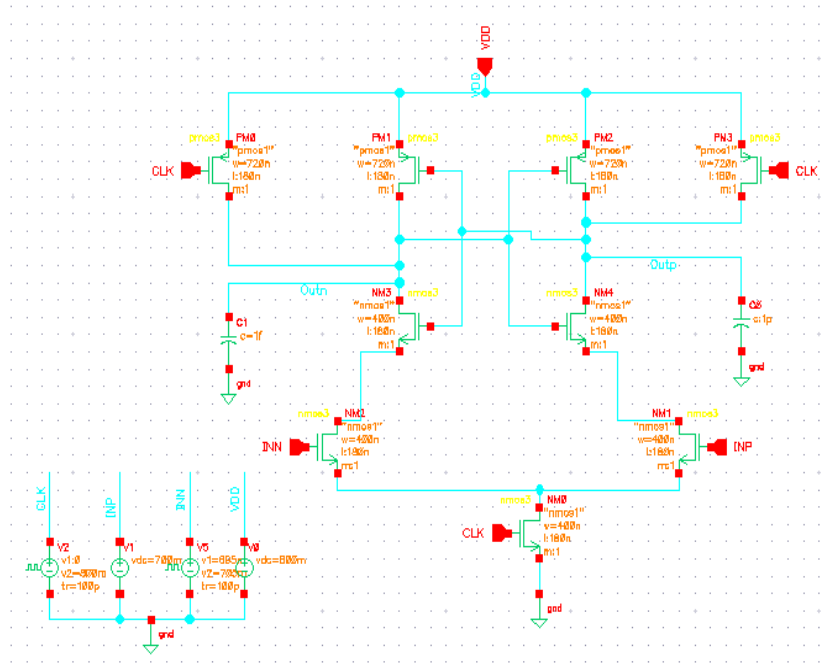


Fig. 3. Schematic of dynamic conventional comparator.

## B. Conventional Double Tail Comparator

The schematic for conventional double tail comparator is shown in fig 4 [9].

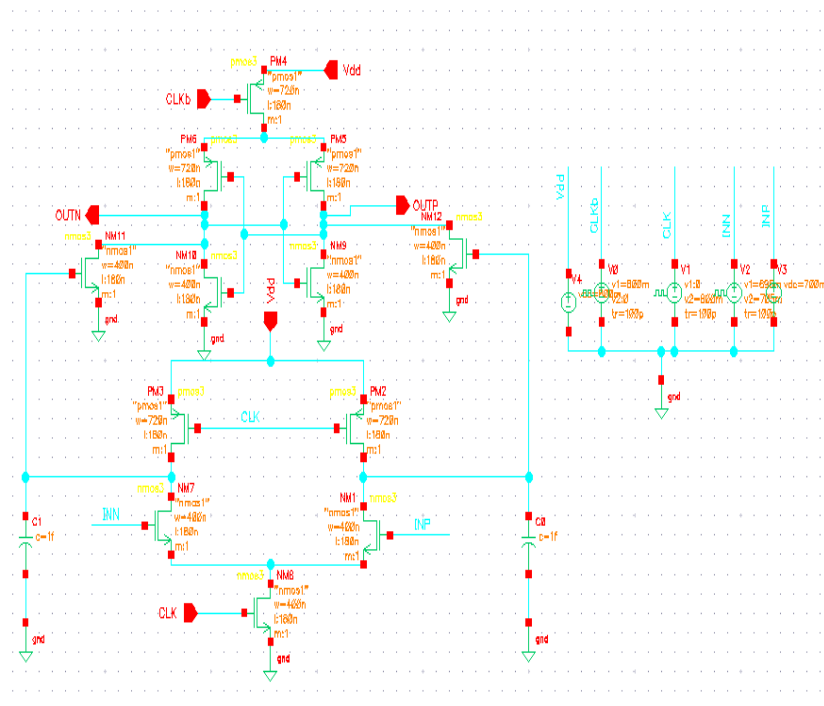


Fig. 4. Schematic of conventional double Tail comparator.

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The difference between conventional dynamic comparator and conventional double tail dynamic comparator is that the double tail comparator can operate at lower supply voltage as compared as compared to conventional dynamic comparator [3]. The schematic for conventional double tail comparator is shown in fig. 4 [7].

The operation of this comparator is executed in two phases. In reset phase (CLK=0), tail transistors (PM4 and NM8) are off. Transistors PM2 and PM3 charge the nodes fn and fp at the drain terminals of these transistors to VDD. As a result of this charging event the intermediate stage transistors, NM11 and NM12 turn on discharging the output nodes (Outn and Outp) to ground.

During comparison phase when CLK=VDD, tail transistors, PM4 and NM8 turn on. PM2 and PM3 transistors are cut-off. The voltages at fn and fp nodes begin to drop at different discharge rates. This voltage drop depends mainly on the drain current of tail transistor (NM8) and the load capacitance value at fn and fp nodes. As in conventional dynamic comparator, the delay of this comparator comprises charging capacitive delay and latch regeneration delay. The disadvantage of this circuit is that it consumes more power. The proposed circuit overcomes this drawback.

### C. Modified Double Tail Comparator [1]:

The circuit proposed in [1] as shown in fig. 5 is a modified version of conventional double tail comparator. In this paper, this modified version has been further modified for high speed and low-power. The proposed circuit is shown in fig. 6. The kickback noise calculation is also done for both these circuits and it is calculated to be lower for the proposed circuit.

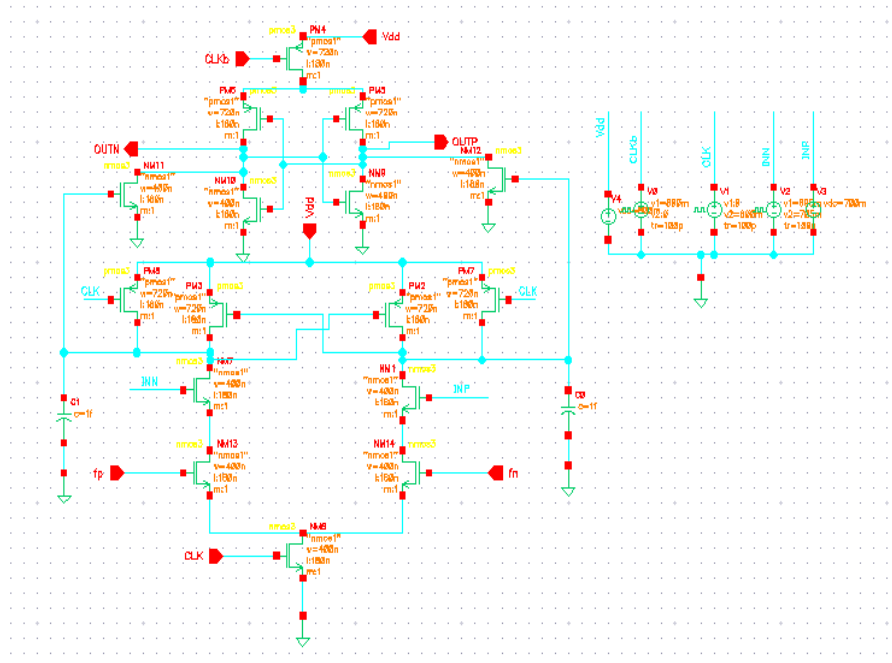


Fig. 5. Schematic of double tail comparator as proposed in [1].

The working of the comparator shown in fig. 5 is described as follows. During RESET phase (CLK=0) tail transistors turn off. The voltages at nodes fn and fp are both pulled up to VDD. Intermediated stage transistors reset both output nodes outn and outp to VDD.

During decision-making phase (CLK=VDD), tail transistors turn on. The voltages at nodes fn and fp begin to fall in accordance to the input voltages with different rate of discharge. For this circuit not only the delay parameter is improved but energy per conversion is reduced as well [1]. During the circuit's reset phase only one of the mentioned nodes (fn or fp) has to be charged unlike in conventional double tail comparator where both nodes should be pulled to VDD.

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The modification was done by inserting two control transistors for faster latch regeneration. Although the circuit is improved in terms of operation speed and thus energy per conversion, the kickback noise is increased in comparison to conventional double tail comparator [1]. The proposed comparator in this paper will improve the circuit in fig. 5 in terms of power, speed, energy and even kickback noise.

### III. PROPOSED COMPARATOR

The schematic of proposed double tail comparator is shown in fig. 6. In the proposed circuit, the control transistor as was added in the proposed circuit of [1], is removed and two extra transistors are added parallel to the two tail transistors connected between the power rail and the rest of the circuit.

The main idea behind the proposed comparator is to reduce the time period for which the circuit is on. For this two transistors are added as can be seen in fig. 6. The inputs provided to these transistors are pulse voltages which have reduced on time period. This leads to reduction in power and enhances the speed of the proposed circuit.

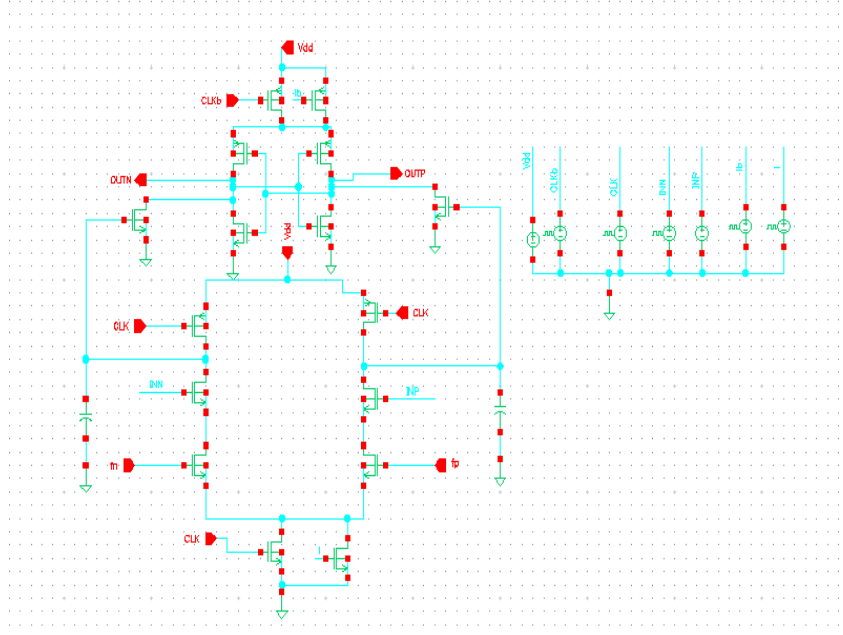


Fig. 6. Schematic of proposed double tail comparator.

### IV. KICKBACK NOISE

In latch type comparators where latch regeneration is utilised for the improvement in circuit performance, kickback noise is usually present that degrade the performance of the circuit in terms of accuracy. The large voltage variations in the internal nodes are coupled to the input, disturbing the input voltage—this is usually called kickback noise [12]. This happens due to the presence of parasitic capacitances of the transistors. The disturbance in the input voltage caused due to the coupling effect of latch is called kickback noise.

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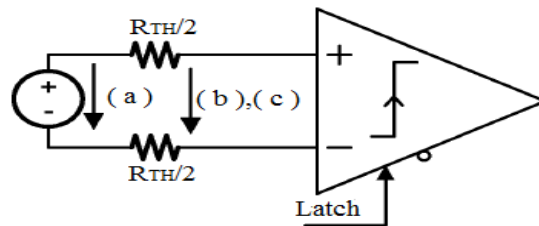


Fig. 7. Circuit to evaluate kickback noise.

The circuit used for evaluation of kickback noise is shown in fig. 7 [12]. The preceding stage is modelled as Thevenin equivalent circuit. In this paper, the value of  $R_{TH}$  is taken to be  $8K\Omega$  for simulations

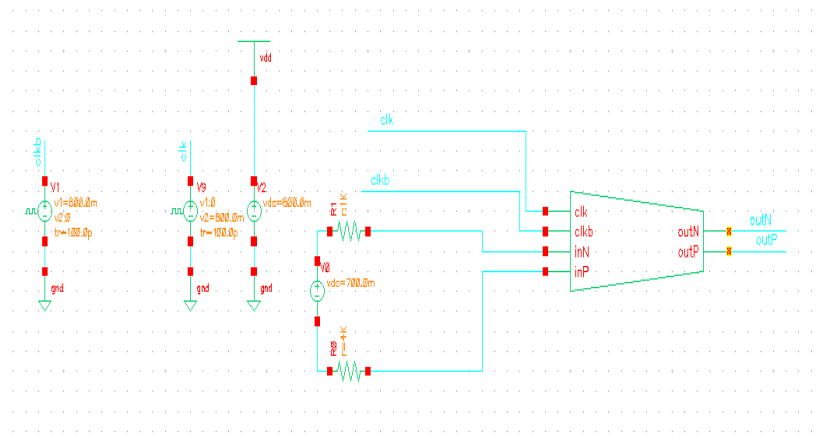


Fig. 7. Kickback noise calculation for circuit shown in fig. 5.

. A circuit has been implemented to calculate the kickback noise of the comparators, shown in fig.7 and fig. 8.

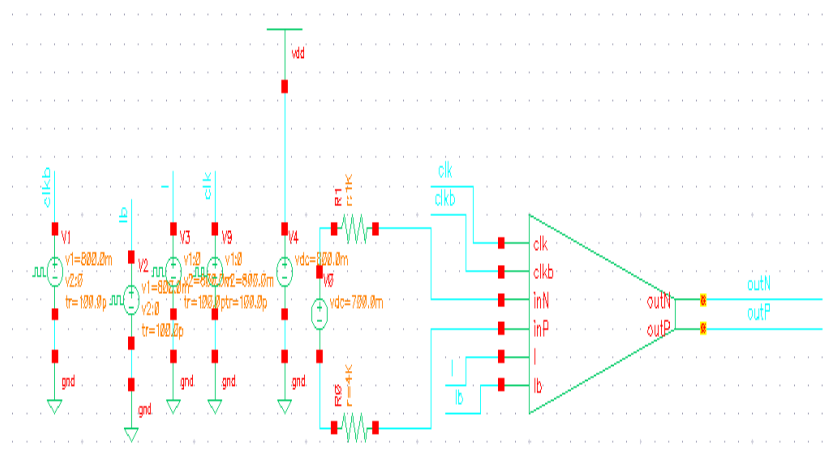


Fig. 8. Kickback noise calculation for the proposed comparator.

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## V. SIMULATIONS AND RESULTS

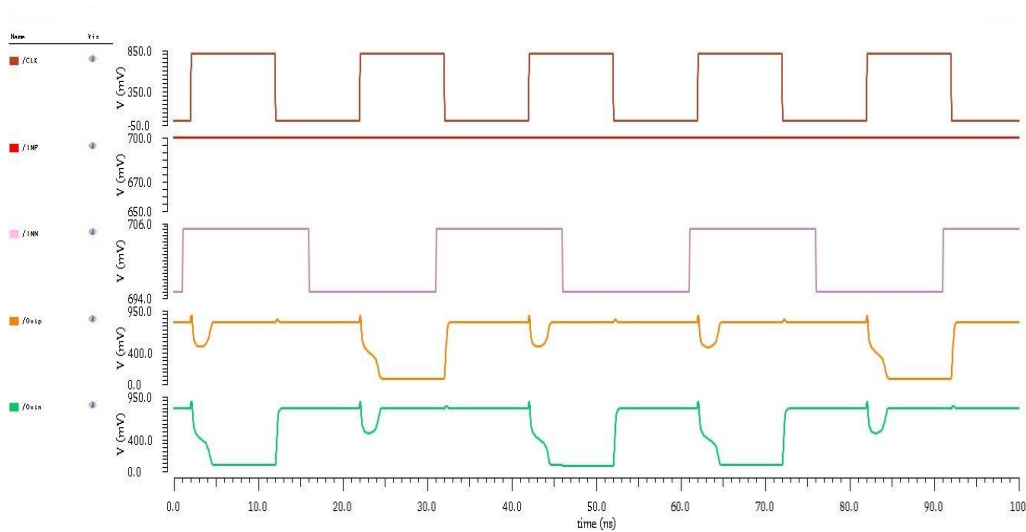


Fig. 9. Transient response of conventional dynamic comparator.

For the efficient comparison of proposed comparator with the comparator proposed in [1] as shown in fig. 5, all the circuits are simulated in 180nm CMOS technology at power supply voltage of 0.8V and clock frequency of 50MHZ.

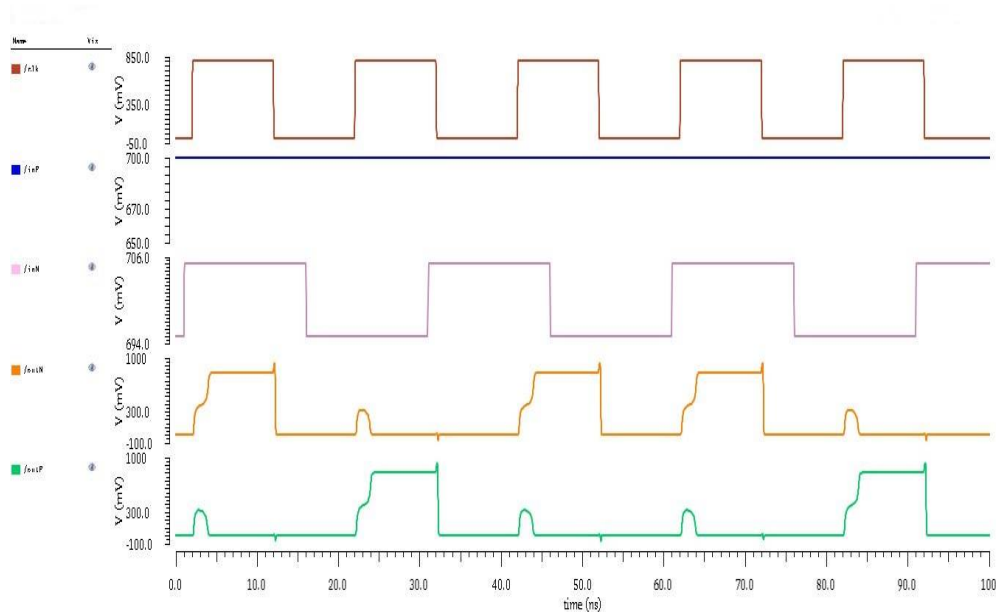


Fig. 10. Transient response of conventional dual tail dynamic comparator.

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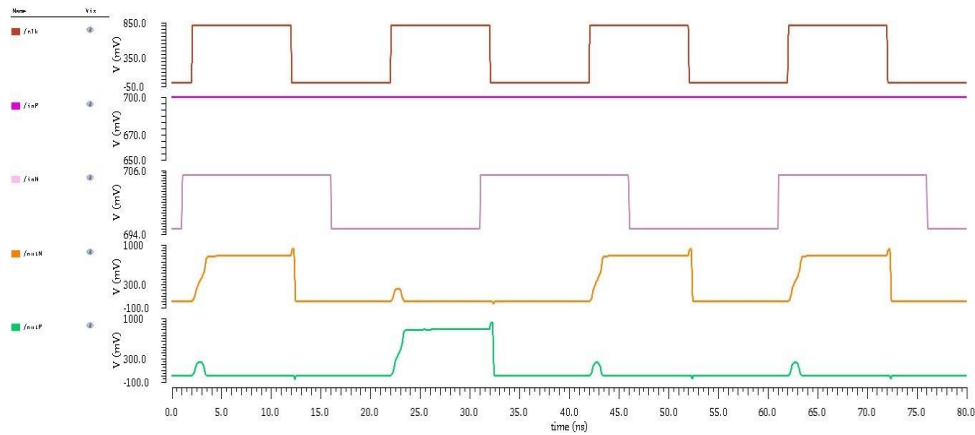


Fig. 11. Transient response for the comparator in fig. 5.

The transient response of the comparator as proposed in [1] and the transient response of the modified comparator is shown in fig. 11 and fig. 12 respectively. The value of capacitance for both the simulations is kept at 1fF.

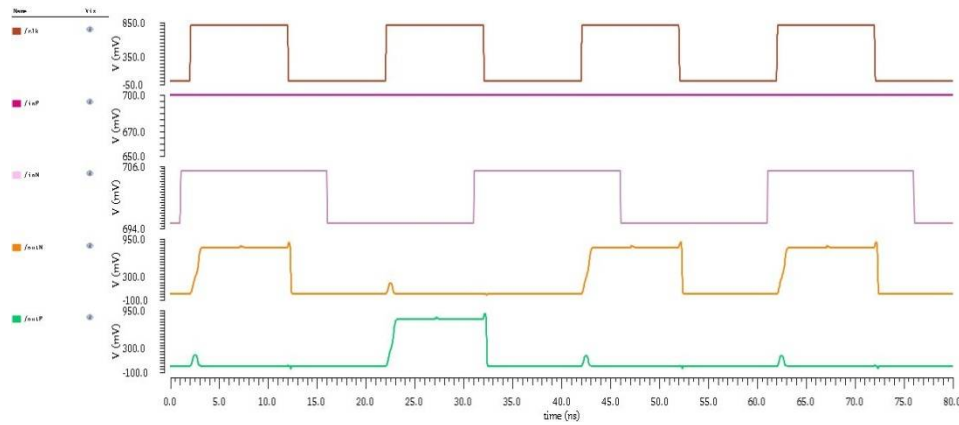


Fig. 12. Transient response for proposed comparator.

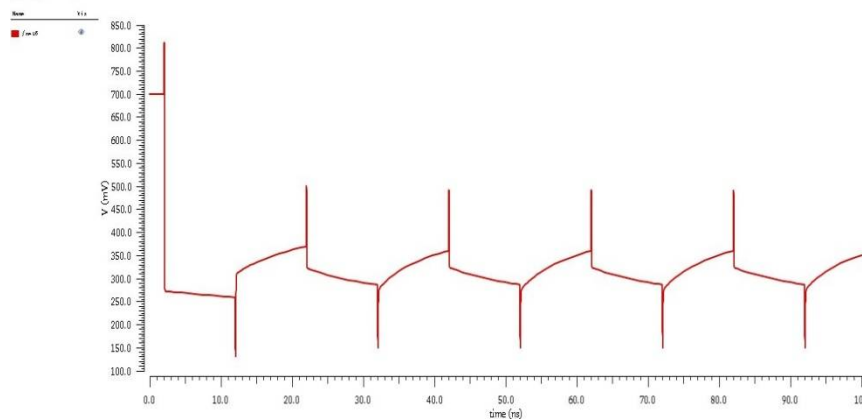


Fig. 13. Waveform for kickback noise calculation of fig. 7.



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The output waveform corresponding to the calculation of kickback noise is shown in fig. 13 and fig. 14. The spikes in the output waveform are the kickback noise voltage levels. The difference between the initial point and the final point of the spikes is calculated as the kickback noise voltage. As can be seen from the voltage waveform, the kickback noise in the proposed comparator is found to be reduced. The RTH value is 8KΩ and the Thevenin voltage is 700mV.

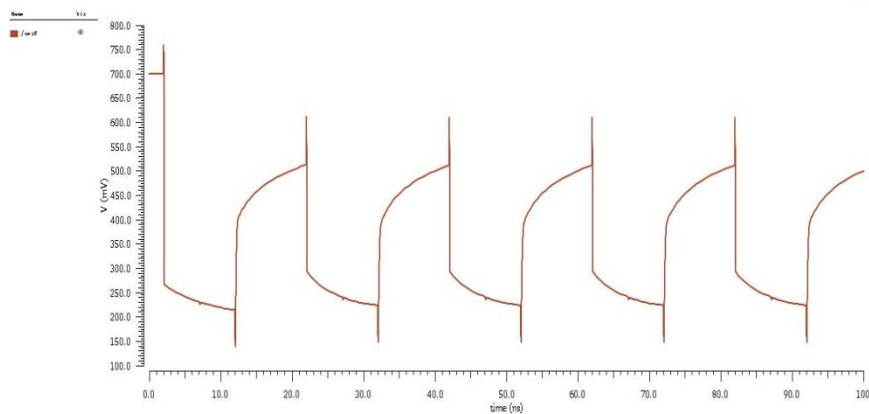


Fig. 14. Waveform for kickback noise calculation of fig. 8.

Different parameters like power, delay PDP and kickback noise has been calculated and tabulated below.

TABLE I. RESULT COMPARISON

Parameters	Base design[1]	Proposed Design
Technology	180 nm	180 nm
Supply Voltage	0.8 V	0.8 V
Power	620.3 nW	218.6 nW
Delay	346.1 ps	276.7 ps
PDP (Power Delay Product)	214.68 aJ	60.48 aJ
Kickback noise	111.62 mV	59.61 mV

## VI. CONCLUSION

In this paper, a modification of dynamic comparator has been presented. The designed circuit has been verified using 0.18μm CMOS technology at VDD=0.8V. Analysis of the parameters like power, delay, power-delay product and kickback noise .A circuit topology for calculating kickback noise has also been presented. The proposed comparator is found to be faster and dissipating lesser power with reduced kickback noise value.

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