

FPGA Implementation of Serial and Parallel FIR Filters by using Vedic and Wallace tree Multiplier

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ABSTRACT: The micro architecture of digital FIR filter consists of a data path and a control unit. The data path is the computational engine of FIR filter and mainly consists of Decoders, adders, multipliers and delay elements. The hardware implementation of a Serial and parallel digital FIR filter architecture using a micro programmed controller is presented. The main advantage of the micro programmed controller is its flexibility in modifying the micro program stored in ROM based control memory. To improve the performance of FIR filter, an efficient multiplier is required. Wallace tree and Vedic multipliers are used for the implementation of serial and parallel micro programmed FIR filter architectures we have proposed a novel high speed and area efficient Vedic multiplier using compressors is used for the implementation of serial and parallel micro programmed FIR filter architectures. The proposed technique, a 4-tap serial and parallel FIR filter is implemented using Xilinx Spartan 3E FPGA. The proposed FIR filter is coded in VERILOG. The design can be easily modified to implement higher-order and high speed FIR filters which are commonly used in video and image processing applications.

KEYWORDS: FIR filter, microprogrammed, Multiplier, FPGA.

I. INTRODUCTION

Digital filters are normally used to filter out undesirable parts of the signal or to provide spectral shaping such as equalization in communication channels, signal detection or analysis in radar applications. Adders, multipliers and shift registers are the basic building blocks commonly used in the implementation of digital filters. These building blocks are arranged and interconnected in different ways according to the filter; Different architectures of digital filters can be realized to achieve the same transfer function. The architectures possess different attributes in the form of speed, complexity and power dissipation. Finite impulse response (FIR) and infinite impulse response (IIR) are two such filters used in different applications.

FIR filters are the important building blocks for digital signal applications, video applications, wireless communication and image processing applications. Because of absolute stability and linear phase properties the FIR filters are extensively used. Basically, FIR filter performs a convolution on a window of N data samples. A common implementation of the FIR filter is shown in Fig. 1, As can be seen from the figure, N-tap or (N-1)th order FIR filter consists of N shift registers, N multipliers and N-1 adders. The impulse response of the FIR filter can be directly inferred from the tap coefficients (W). The multiplier is the fundamental component which decides the overall

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performance of the FIR filter. FPGAs have emerged as a platform of choice for faster and efficient realization of compute-intensive applications. It provides hardware speed, software flexibility and price/performance ratio much more favorable than application specific integrated circuits (ASICs)

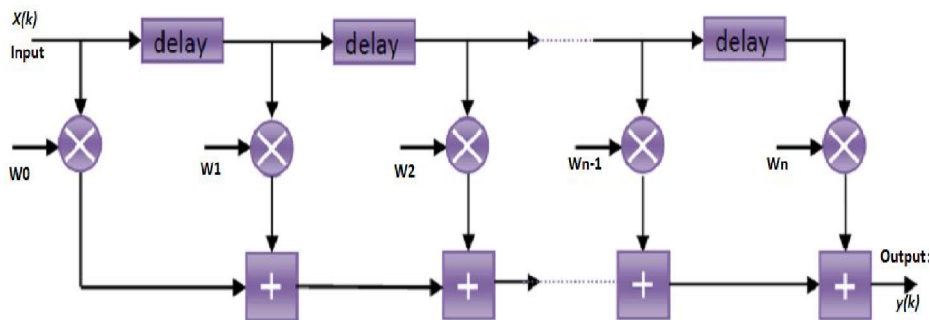


Fig 1: Basic FIR filter

II. MICROPROGRAMMED FIR FILTER

The microprogrammed FIR filter consists of a datapath and a microprogram control unit (MCU). The most important advantage of the MCU is its flexibility. Many additions and any changes can be done by changing the microinstructions in the memory.

a) Serial Architecture of Micro programmed FIR Filter: The serial architecture of N -tap microprogrammed FIR filter is shown in Fig. 2. It basically comprises of a MCU and a datapath unit. The MCU consists of a microprogram counter and microprogram memory. The datapath unit comprises of $2N$ data (X) and coefficient (W) registers and M -to- N decoder ($M = \log_2 N$), two N -input multiplexers for selecting the data and coefficients, a multiplier and an adder, a two input multiplexer to control the flow of data from multiplier or accumulator, one 16-bit accumulator and a 16-bit register to latch the data.

b) Parallel Architecture of Microprogrammed FIR Filter: In the serial architecture design single adder and single multiplier are used, but the parallel architecture utilizes multiple adders and multipliers based on the size of the FIR filter. Fig. 3 illustrates the parallel architecture of the microprogrammed FIR filter [8]. For example, the datapath microarchitecture of 4-tap parallel FIR filter consists of the following sub-modules:

- Four 8-bit data registers
- One 2-to-4 decoder
- Four 8-bit coefficient registers
- Four multipliers (8×8)

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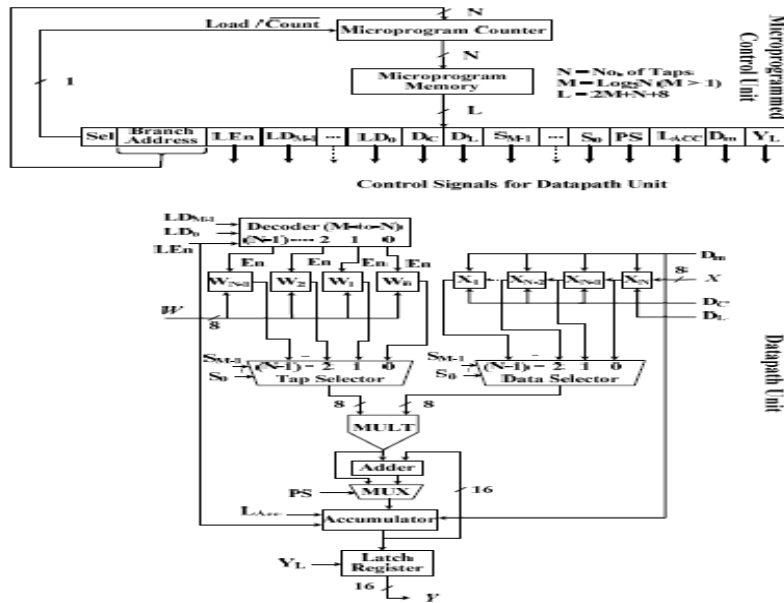


Fig. 2. Architecture of serial microprogrammed FIR filter

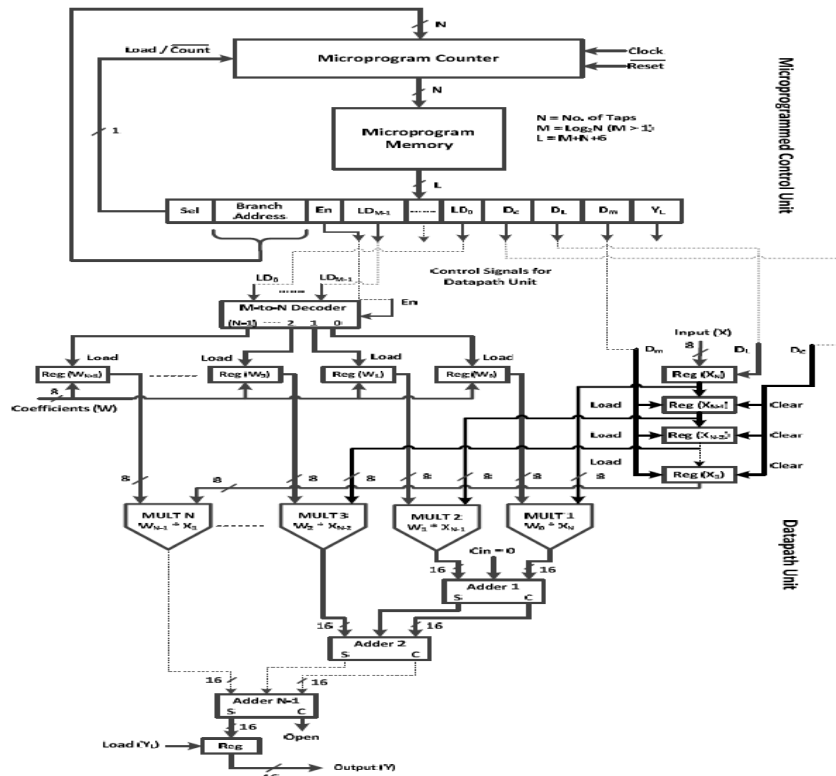


Fig. 3. Architecture of parallel microprogrammed FIR filter

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III. WALLACE TREE MULTIPLIER DESIGN

A method for fast multiplication was originally proposed by Wallace. Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. A three step process is employed to multiply two integer numbers by using this method.

Step 1: Multiply each bit of one of the arguments, by each bit of the other, yielding n^2 results. Based on the position of the multiplied bits, the wires carry different weights.

Step 2: Reduce the number of partial products to two by layers of full and half adders.

Step 3: Group the wires in two and then add them using conventional adder.

Two different architectures of Wallace tree multiplier are implemented in the paper. First one is designed using only half adder and full adder, while the second one uses a more sophisticated carry skip adder (CSA)

Wallace Tree Multiplier using Carry Skip Adder: A carry-skip adder consists of a simple ripple carry-adder (RCA) with a special speed up carry chain called a skip chain [10]. The purpose of using the CSA is to improve the worst case path delay. In this work, we used a 4-bit CSA for implementing the Wallace tree multiplier. In this design, 4-bit carry skip is used for the addition of partial products. Four bits from one row is being added with the next row as shown in Fig. 4 and the carry output from the first addition is the carry input for the second addition. The main advantage of using CSA is to improve the speed.

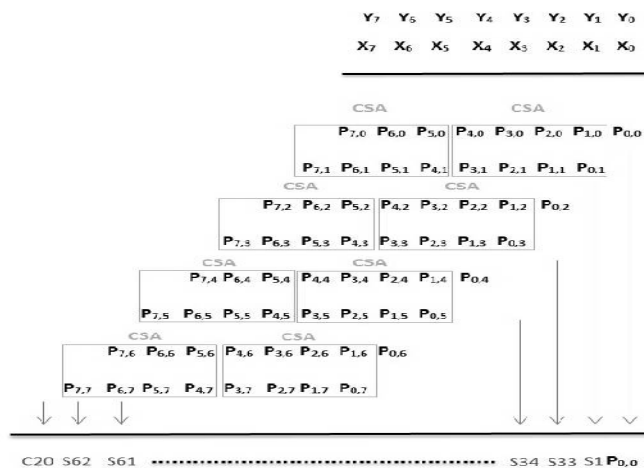


Fig. 4. Wallace tree partial product addition using carry skip adder

IV. VEDIC MULTIPLIER DESIGN

Vedic mathematics is an ancient form of mathematics which is used for efficient digital multiplication. Its calculation is defined by vertical and crosswise product that gives advantage over the normal conventional horizontal multiplication. For binary number, the multiplication operation is reduced to bitwise “AND” operation and the addition operation use full or half adders.

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The Vedic mathematics concept is applied to develop modular RTL Verilog code for 2x2 multiplier which can be used as a building block to develop 4x4 multiplier. An 8x8 multiplier can be further designed using the 4x4 multiplier and so on. The 4-bit and 8-bit multipliers used conventional half and full adders for the proposed design. The same Vedic multiplier design is realized using Kogge-Stone adder (KSA) and the architecture of 4-bit is shown in Fig. 5. KSA is a parallel prefix form of carry look-ahead adder. It generates the carry signals in $O(\log 2N)$ time, and is thus widely considered as the fastest adder design.

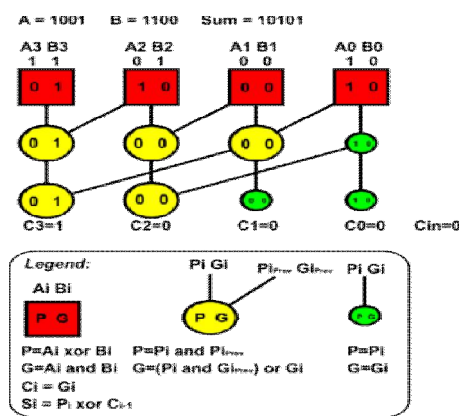


Fig.5. 4-bit Kogge- Stone adder

V. Simulation Results

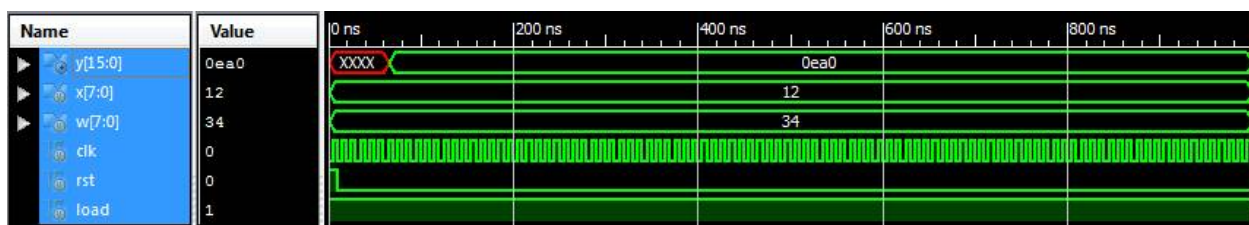


Fig. 6. Parallel microprogrammed FIR filter using Vedic multiplier

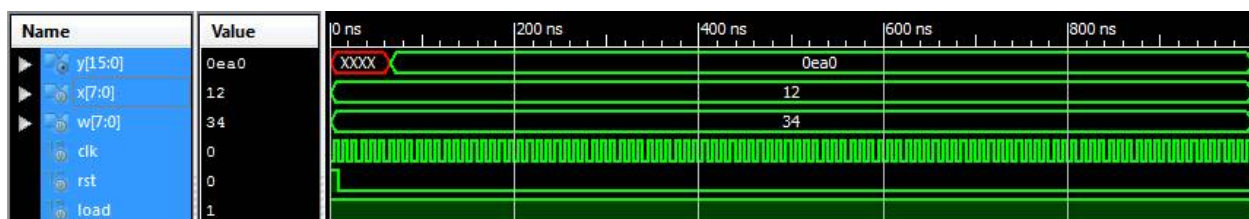


Fig. 7. Parallel microprogrammed FIR filter using Wallace tree CSA

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VII.CONCLUSION

Digital filters are one of the main elements of DSP. FIR filter which mainly comprises of multiply-accumulate structure is the most commonly used digital filter. Since the performance of FIR Filter mostly depends on the multiplier used, an enhanced and improved multiplier will ameliorate the overall system performance. In this paper, we designed and implemented micro programmed serial and parallel FIR filter architectures in Xilinx Spartan3e FPGA using ripple carry adder, Kogge-Stone adder and Vedic multiplier using compressors combinations respectively.

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