

A Survey on Fully Reused Architecture of FM0 & Manchester Encoding for DSRC Communication

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ABSTRACT: Manchester coding strategy is an advanced coding procedure in which every bits of the binary information are rearranged in a specific arrangement. Dedicated Short Range Communication is a simplex or duplex short range to medium range remote correspondence. It is utilized to support Intelligent Transport System (ITS) applications, for example, electronic toll collection, parking area, border crossing distinguishing proof etc. It proposes a VLSI engineering architecture similarity-oriented logic simplification (SOLS) procedure. The SOLS comprises of two centre strategies: area-compact retiming and balance logic operation sharing. The area-compact retiming moves the equipment and hardware resource to diminish 5 transistors. The balance logic operation sharing productively utilizes miller operator encodings to the completely reused hardware design. With SOLS strategy, we develops a completely reused VLSI design of Manchester and FM0 encodings for DSRC applications. This paper likewise demonstrated that range compaction of proposed VLSI design contrasted with existing strategy.

KEYWORDS: DSCR, Encoding, VLSI, SOLS, Encoder.

I. INTRODUCTION

Dedicated Short Range Communication (DSRC) is a convention simplex or duplex range correspondence in the advanced automotive industry. The DSRC chiefly utilized for intelligent transportation frameworks. It can be quickly named vehicle to vehicle and vehicle to street side correspondences. The DSRC can give a inter communication amongst vehicles and street sides for safety issues and open data declaration. These wellbeing message incorporate blind side, impact alert, bury autos remove and so on. The vehicle to roadside correspondence predominantly concentrates on clever transport framework, for example, electronic toll gathering (ETC) framework.

The DSRC transceiver is classified as three basic modules

- (i) Microprocessor
- (ii) Baseband Processing
- (iii) RF-Front End.

The Microprocessor used to translates directions from Media Access Control (MAC) to plan the assignments of Baseband Processing and RF-Front End. The adjustment, error correction, clock synchronization, encoding all is finished by Base Band Processing. The RF Front End transmits the remote flag through Antenna and gets the wireless flag through Antenna (i.e. physical transmission).All three modules co - work with each to perform DSRC conventions. A few nations have been set up DSRC Standard s by different associations.

The reliability of data signal is too important in DSRC standards compared to the data rate.

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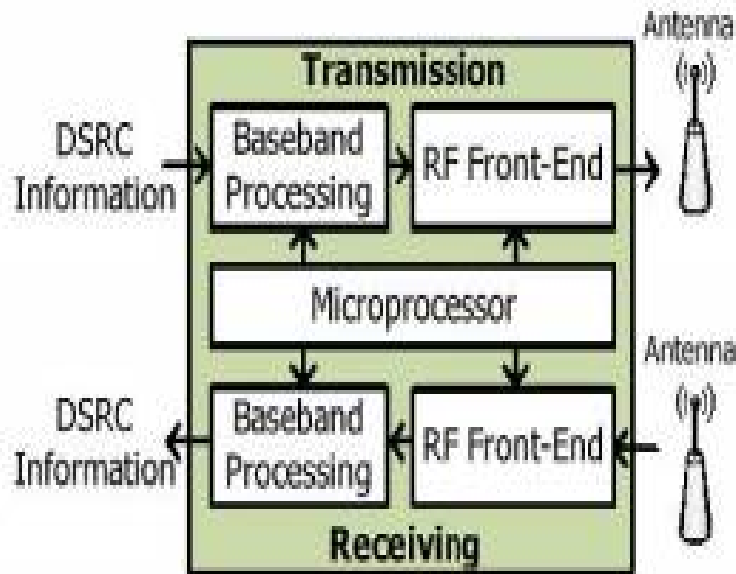


Fig1: System Architecture of DSRC transceiver

Table1: DSRC Standards of different nations

	Europe	America	Japan
Organization	CEN	ASTM	ARIB
Data Rate	500 kbps	27 Mbps	4 Mbps
Carrier Frequency	5.8 GHz	5.9 GHz	5.8 GHz
Modulation	ASK,PSK	OFDM	ASK
Encoding(Downlink)	FMO	Manchester	Manchester

CEN- European Committee for Standardization.
ASTM - American Society for Testing and Materials.
ARIB- Association of Radio Industries and Business

This paper proposes the design of VLSI Architecture using SOL's technology. Section V consists of two major mechanisms. (i) Compact Area with retiming (ii) Sharing of Logic Operation. The Compact Area with Retiming that compact the area by reducing 22 transistors in the hardware design. The Sharing of Logic Operation that achieves fully reused hardware Architecture by combining FMO and Manchester encodings. By using above technique, Section III

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gives details about the FMO and Manchester encoding Architecture designed for DSRC applications. Section IV states the limitations of Hardware architecture. And Section V consist conclusion of the proposed work.

II. LITERATURE REVIEW

In [1], [5] author proposed completely reused VLSI (Very Large Scale Integration) engineering by utilizing SOLS method for both the FM0 and Manchester encoding. The SOLS strategy eliminates the restrictions of hardware usage by utilizing two centre procedures (1) Area conservative retiming and (2) Balance logic operation sharing systems. The Area minimized retiming is utilized to lessen the equipment issue like number of transistors and the adjust logic operation sharing which help in distinguishable logic segments can be productively consolidates with the FM0 and Manchester encoding. In this paper the proposed strategy takes a shot at parameters like low power utilization, high working recurrence and so on. This paper builds up a completely reused VLSI engineering and furthermore shows a focused execution contrasted and the current works.

In [2], it is demonstrated that an unbalance calculation time brings about the glitch at the contribution of MUX that causes the logic fault on coding. This paper beats the issue of glitches by utilizing XNOR with the inverter by supplanting the XOR and this turns into the contribution of the MUX. This is done to adjust the computational time. The selection of FM0 or Manchester code relies upon Mode and CLR flag. In this plan both modes are independently allotted to framework controller. Regardless of whether FM0 or Manchester code is received, all the rationale segment of the proposed VLSI engineering is used and gives better outcomes.

The work in [3] presents an audit on Manchester, Miller and FM0 encoding strategies. This paper exhibits the circuit plan methodologies of Manchester, Miller and FM0 utilizing a limited state machine. A near investigation of every one of these procedures is likewise introduced in this work.

A survey on hypothetical foundation of FM0 and Manchester [4] is exhibited depicting the utility of FM0 and Manchester encoding and how it can be utilized for DSRC. In DSRC DC-Stability and flag dependability are satisfied by FM0 and Manchester. These works displays an arrangement of VLSI engineering of FM0/Manchester encoding utilizing SOLC procedure and furthermore contrast this strategy and different systems. The SOLS comprises of two centre techniques, for example, area compact retiming and adjust logic operation sharing. The territory smaller retiming system relocates the hardware resource to decrease transistors. The adjust rationale operation sharing strategy of SOLC proficiently joins FM0 and Manchester encodings with the completely reused equipment design. This paper actualizes a completely reused VLSI design, as well as displays a focused execution contrasted and the current methods.

In [6] presents an audit on assessment of different types of DSRC framework. DSRC is the main short-go remote option today that gives Fast Network Acquisition, Low Latency, High Reliability when Required, Priority for Safety Applications, Interoperability, Security and Privacy which is one of the testing assignment confronted by all in the around the world. This article manages dynamic Dedicated Short Range Communications (DSRC) application for Intelligent Transport Systems (ITS) and its monetary assessment concentrated on numerous remote frameworks like vehicle correspondence, versatile Communication and so on.

In [7] proposed a fully reused VLSI architecture using the SOLS technique for both FM0 and Manchester encoding. The SOLS technique eliminates the limitation of hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The performance of this paper is evaluated on the post layout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18- μm 1P6M CMOS technology. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 \times 30.43 μm^2 . This paper not only develops a fully reused VLSI architecture and also exhibits an efficient performance compared with the existing works.

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III. FMo AND MANCHESTER CODING PRINCIPLES

There are lots of urban traffic issues such as driver safety, traffic management, smart cities, traffic Optimization and parking applications. All above issues are associated with wireless sensor network. There is a requirement to provide links among infrastructures, vehicles and sensor nodes in wireless manner.

This paper aims to design the encoding and decoding techniques such as (i) FMO (Flexible Macro Block Ordering) (ii) Miller Encoding for DSRC application. The objective is achieved by using FMO and Manchester and SOLS. The coding diversity between FMO/Manchester coding limits the design of VLSI architecture of both codings. Using SOLS (Similarity Oriented logic Simplification) technique, the diversity was eliminated. It also used to achieve HUR (Hardware Utilization Rate) as 100%.

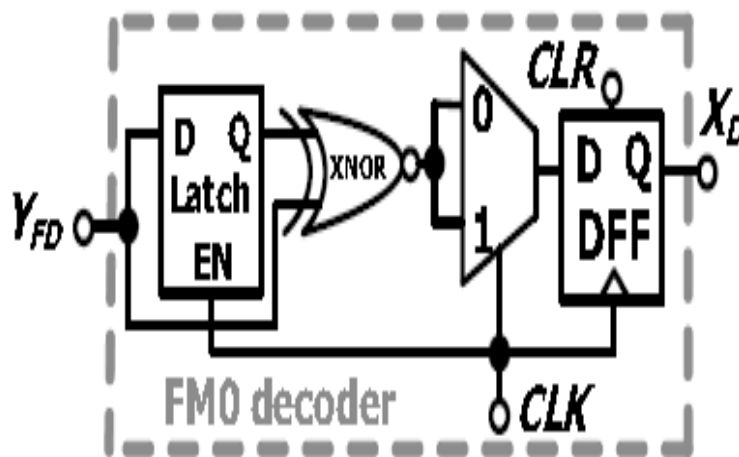


Fig2. FMo Decoder Diagram

for FMo decoder, positive-cycle logic and negative-cycle logic are identical. As a result, the DFF is originally reused with both. To fit the HCPM, this DFF is directly relocated backward after the multiplexer, as shown in Fig.2.

A. MANCHESTER ENCODING AND DECODING

The Manchester encoding is given as

$$YME = XE_CLK \dots\dots\dots (1)$$

where XE and YME stand for the binary data to be encoded and its corresponding Manchester code, respectively. The CLK is a clock signal. According to (1), YME must have a signal-transition in every cycle, whether XE is logic-1 or logic-0.

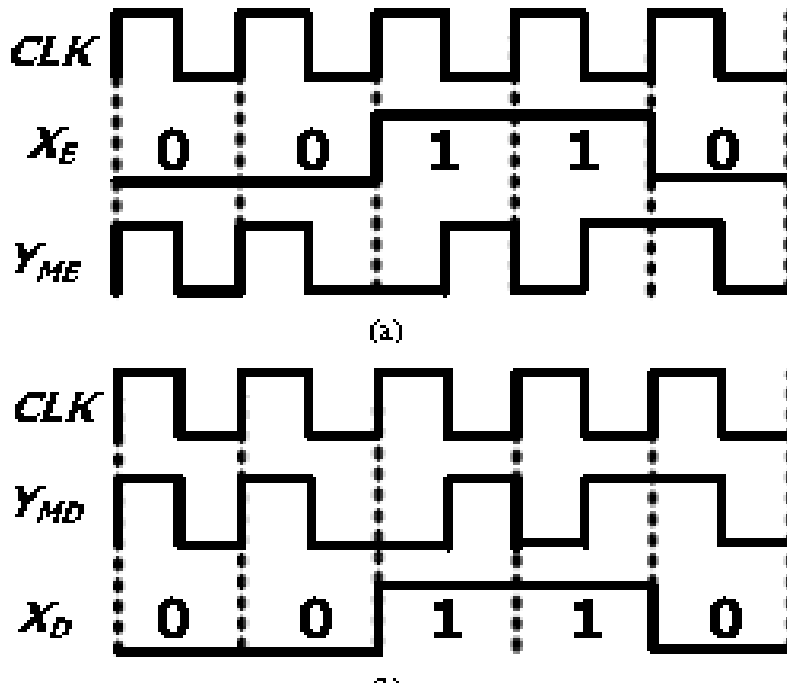


Fig3: The illustration of Manchester code. (a) Manchester encoding. (b) Manchester decoding.

With this signal transition, air conditioning parts are implanted into the YME, which can encourage the synchronization in receiver. Correspondingly, the Manchester disentangling is given as

$$X_D = Y_{MD} - CLK \dots\dots\dots (2)$$

Where X_D remains for the decoded parallel information and the Y_{MD} signifies a Manchester codeword to be decoded. Two cases are represented for Manchester encoding/disentangling in Fig. 3(a) and Fig. 3(b), separately. Both can be essentially acknowledged by a 2-input XOR door.

B. FM0 ENCODING AND DECODING

Prior to the examination of FM0 encoding/translating systems, the structure of FM0 code is depicted first. The FM0 code YFE is isolated into two sections: YFP and YFN. The YFP and the YFN speak to the FM0 code at positive-cycle and negative-cycle, individually.

The encoding method of FM0 code is ordered as taking after three principles:

- 1) For the X_E of logic-0, signal-transitions distributed amongst YFP and YFN.
- 2) For the X_E of logic-1, no signal-transition is distributed amongst YFP and YFN.
- 3) A flag move exists among each YFE.

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TABLE II
POSITIVE-CYCLE LOGIC AND NEGATIVE-CYCLE LOGIC OF FM0/MANCHESTER ENCODING AND DECODING

	Positive-cycle logic	Negative-cycle logic
FM0 encoding	$\overline{Y_{FN}(t-1)}$	$X_E \oplus Y_{FN}(t-1)$
FM0 decoding	$Y_{FN}(t) \odot Y_{FP}(t)$ (omitted)	$Y_{FN}(t) \odot Y_{FP}(t)$
Manchester encoding	$\overline{X_E}$	X_E
Manchester decoding	$\overline{Y_{MD}}$ (omitted)	Y_{MD}

IV. HARDWARE ARCHITECTURE

The motivation behind SOL's method is to plan a completely reused VLSI engineering for FM0 and Manchester encodings. The SOLS strategy is arranged into two sections: area-compact retiming and balance logic-operation sharing. Every part is independently portrayed as follows. At long last, the execution assessment of the SOLS strategy is given.

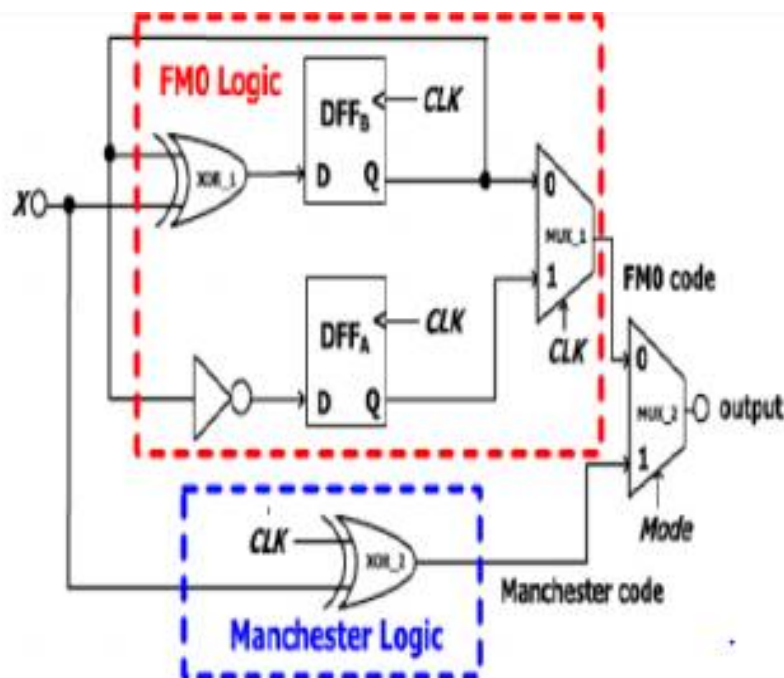


Fig4: Hardware Architecture Using FM0 Logic and Manchester Logic

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The SOLS procedure enhances the HUR from 57.14% to 100%, regardless of whether the FM0 or Manchester code is received. Along these lines, the SOLS system gives a completely reused VLSI engineering for FM0 and Manchester encodings with the HUR of 100%. The rationale elements of SOLS strategy can be acknowledged by different logic capacities to advance more execution, for example, range, power, and speed. The proposed SOLS strategy is produced from the design point of view to accomplish 100% HUR. On the off chance that the logic parts in SOLS engineering are composed utilizing static CMOS, the Manchester postponement is genuinely constrained attributable to an excessive number of transistors in the basic way of Manchester encoder. To additionally decrease the transistor check in Manchester encoding way, the transmission-gate logic is considered in the circuit plans of MUX-1, MUX-2 and XNOR. The engendering postponement of transmission-gate logic is not as much as that of static CMOS. Applying the transmission gate logic can minimized the transistor tally to reduce the propagation delay. With the over 2 conditions the equipment design of FM0 and Manchester encoding, the top part speak to the FM0 encoder while the base part signifies the Manchester encoder. The FM0 encoding relies upon the past condition of FM0 code, not just on x. The state code of FM0 is put away in DFFA and DFFB. The Mux_1 is utilized to switch A (t) and B (t) through the determination of CLK. The assurance of causing is relies upon mode choice of Mux_2.

Mode = 0; FM0 code

Mode = 1; Manchester code.

The equipment usage rate (HUR) is controlled by

$$HUR = (\text{dynamic segments} / \text{Total segments}) \times 100\%$$

The segments utilized for FM0 and Manchester encoding is named as dynamic segment though the quantity of parts utilized as a part of the whole hardware architecture without considering the encoding strategy is named as total segments.

V. VLSI IMPLEMENTATION

The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact Re-timing and balance logic-operation sharing.

A. AREA-COMPACT RETIMING

The logic for $A(t)$ and the logic for $B(t)$ are the Boolean functions to derive $A(t)$ and $B(t)$, where the X is omitted for a concise representation. $A(t)$ and $B(t)$ represent the discrete-time state code of current-state at time instant t . Their previous-states are denoted as the $A(t-1)$ and the $B(t-1)$, respectively. With this transition table, the Boolean functions of $A(t)$ and $B(t)$ are given as

$$A(t) = B(t-1) \dots \dots \dots (3)$$

$$B(t) = X \oplus B(t-1) \dots \dots \dots (4)$$

For FM0, the state code of each state is stored into DFFA and DFFB. According to (2) and (3), the transition of state code only depends on $B(t-1)$ instead of both $A(t-1)$ and $B(t-1)$.

B. BALANCE LOGIC-OPERATION SHARING

As mentioned previously, the Manchester encoding can be derived from $X \oplus \text{CLK}$, and it is also equivalent to $X \oplus \text{CLK} = X \text{CLK} + X \text{CLK} \dots \dots \dots (5)$

This can be realized by the multiplexer. The concept of balance logic-operation sharing is to integrate the X into $A(t)$ and X into $B(t)$. The fm0 and Manchester logics have a common point of the multiplexer like logic with the selection of the CLK. the diagram for the balance logic operation sharing given the following.

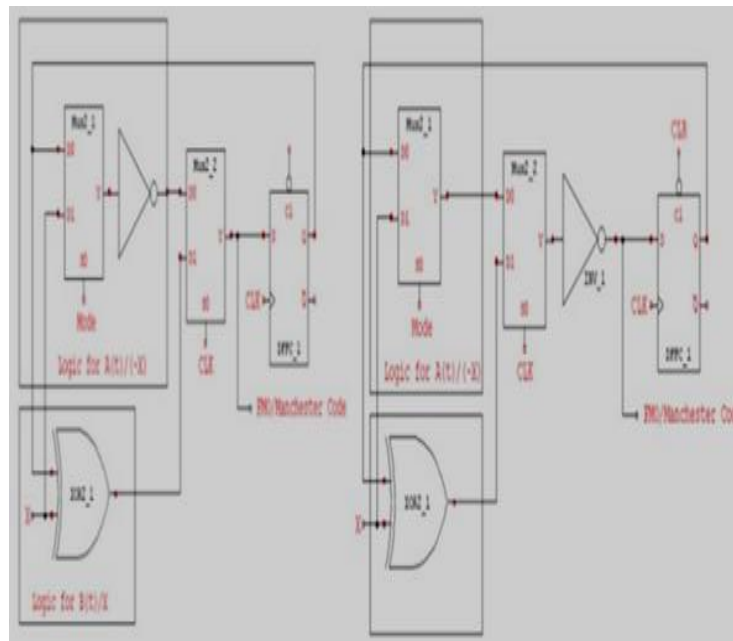


Fig.5. VLSI Architecture of Fmo and Manchester Encodings Using Sols Technique

The transistor count of the FMO encoding architecture without and with compact of area retiming are followed as 72, 50. Thus it reduces 22 transistors.

VI. CONCLUSION

The introduced work uses the outline methodologies of number of researchers and presents a brief of it. This review paper shows the basic work that clarify the whole circuits of FMO encoder, Miller, Manchester and a FSM (limited state machine) for every one of the three encoders which are outlined by utilizing VHDL (Verilog Hardware Description Languages). The idea of encoding will be utilized as a part of different applications as future work. The coding-differing qualities amongst FMO and Manchester encoding cause the restriction on hardware use of VLSI engineering outline. The restriction on hardware utilization of FMO and Manchester encodings is talked about in detail. In this paper, the completely reused VLSI design utilizing SOLS system for both FMO and Manchester encoding is proposed. The SOL's strategy eliminates the restriction on hardware use by two centre systems: territory conservative retiming and adjusts rationale operation sharing.

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