

Design of Low Power Full Adder Based Wallace Tree Multiplier Using Cadence 180nm Technology

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ABSTRACT: In recent year, power dissipation is one of the biggest challenges in VLSI Design. Multipliers are the main sources of power dissipation in DSP blocks. This project presents efficient 4-bits unsigned binary multipliers architectures, such as Array multiplier and Wallace Tree Multiplier. This implementation carried out using cadence 180nm technology. In This design, initially design transistor level schematic circuits than create the test symbol, multiplier circuits are efficiently optimized in terms of area and power. The implementation consist of combinational components such as 1-bit Full Adders, AND, XOR, Half Adder, Inverter circuits. The circuit analysis is carried out in terms of performance parameter such as transistor count, and power consumption. According to the estimation done the transistor count and power consumption of array multiplier was found to be 288, 446.5µw respectively, for Wallace tree multiplier was found to be 262, 134.7µw.

KEYWORDS: Multiplier, Power Dissipation, Wallace Tree Multiplier, Array Multiplier, Full Adder, Cadence Virtuoso Tool

LINTRODUCTION

One of the most important issues in VLSI Desig in power consumption. With the continuously increasing chips complexity and number of transistors in a chip, circuit’s power consumption is growing as well. Higher power consumption, raises chips temperature and directly affects battery life in portable designs as it causes more current to be withdrawn from the power supply. High temperature afflicts circuit operation and reliability so requires more complicated cooling and packing techniques. Full adder is the fundamental unit in circuits used for performing arithmetic operations such as multipliers, large adders therefore reducing power consumption in full adders, will reduce the overall power consumption of the whole system. Most of the VLSI applications.

Multiplier is one of the key hardware blocks in most digital signal processing (DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis. Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Multiplications are very expensive and slow the overall operation. The performances of many computational problems are often dominated by the speed at which a multiplication operation can be executed. Consider two unsigned binary numbers X and Y that are M and N bits wide, respectively. To introduce the multiplication operation, it is useful to express X and Y in the binary representation, the below fig.1 structure of Multiplier.

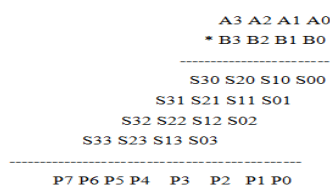


Fig1: Structure of Multiplier

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A. Different Multiplier Architecture

Array multiplier: The Array Multiplier originates from the multiplication parallelogram. The composition of an array multiplier is shown in the fig.2. There is a one to one topological correspondence between this hardware structure and the manual multiplication shown in fig.2. The generation of n partial products requires $N \times M$ two bit AND gates. Most of the area of the multiplier is devoted to the adding of n partial products, which requires $N-1$, M -bit adders. The shifting of the partial products for their proper alignment's performed by simple routing and does not require any logic. The overall structure can be easily compacted into rectangle, resulting in very efficient transistor level schematic design.

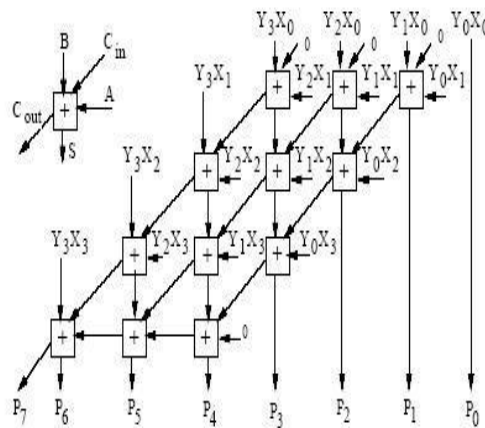


Fig 2: Block Diagram of Array Multiplier

B Wallace Tree Multiplier:

A Wallace tree is an efficient hardware implementation approach to design a digital circuit that multiplies two integers, and this multiplier is first introduced by an Australian Computer Scientist Chris Wallace in 1964. Wallace tree is known for their optimal computation time, when adding multiple operands to two outputs using carry-save adders. Other researchers also proved that Wallace tree and Dadda multipliers are the two well-known fast multipliers compared to array multiplier. However, the Wallace tree guarantees the lowest overall delay. The Wallace tree has three steps to perform during the multiplication process: first, multiplying each bit of one of the arguments, by each bit of the other. Depending on the position of the multiplied bits, the wires carry different weights. Next, reduction of the number of partial products to two by layers of full and half adders will be performed and lastly, group the wires into numbers, and add them with a carry look ahead adder.

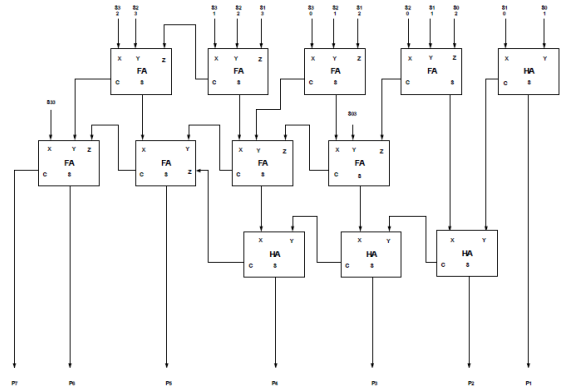


Fig 3: Block diagram of Wallace tree Multiplier

A Wallace tree is an efficient hardware implementation approach to design a digital circuit that multiplies two integers, and this multiplier is first introduced by an Australian Computer Scientist Chris Wallace in 1964. Wallace tree is known for their optimal computation time, when adding multiple operands to two outputs using carry-save adders. Other researchers also proved that Wallace tree and Dadda multipliers are the two well-known fast multipliers compared to array multiplier. However, the Wallace tree guarantees the lowest overall delay. The Wallace tree has three steps to perform during the multiplication process: first, multiplying each bit of one of the arguments, by each bit of the other. Depending on the position of the multiplied bits, the wires carry different weights. Next, reduction of the number of partial products to two by layers of full and half adders will be performed and lastly, group the wires into numbers, and add them with a carry look ahead adder.

Applications of Wallace Tree Multiplier

- Multiplication is the basic arithmetic operation important in several microprocessors and digital signal processing applications.
- Digital Signal processing Systems require multipliers to implement DSP algorithms such as convolution and filtering where the multiplier lies directly within the critical path.
- Multipliers are the most frequently used devices in Image processing. Fast Fourier Transformation (FFT) is one of the important transforms often used in image processing. The computational process of FFT involves a large number of addition and multiplication operations.

C. Cadence EDA Tool Used For Design:

Cadence EDA Tool:

- **Operating System:** Red Hat Linux 5.1.19.6
- **Design Tool:** Cadence IC6.1.6

Cadence Features: Cadence Virtuoso Schematic Editor: It provides numerous capabilities to facilitate fast and easy design entry, including design assistants that speed common tasks by as much as 5x.

Cadence Virtuoso Analog Design Environment: Designed to help users create manufacturing-robust designs, it is the advanced design and simulation environment for the Virtuoso platform. It gives designers access to a new parasitic estimation and comparison flow and optimization algorithms that help to center designs better for yield improvement and advanced matching and sensitivity analyses. By supporting extensive exploration of multiple designs against their objective specifications, Virtuoso Analog Design Environment sets the standard in fast and accurate design verification.

II.LITERATURE SURVEY

Multipliers play an important role in today’s digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of following – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one

multiplier. Thus, making them suitable for various high speed, low power, and compact VLSI implementation. The common multiplication method is add and shift algorithm. Multiplication is a mathematical operation that at its simplest is an abbreviated process of adding an integer to itself, a specified number of times. A number (multiplicand) is added to itself a number of times as specified by another number (multiplier) to form a result (product).

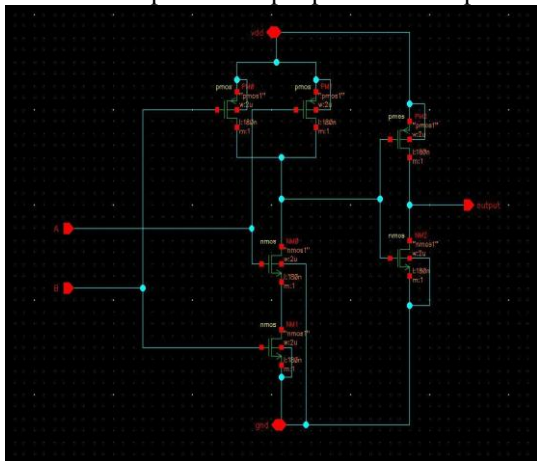
Multiplication hardware often consumes much time and area compared to other arithmetic operations. Digital signal processors use a multiplier unit as a basic building block and the algorithms they run are often multiply-intensive. Multiplication-based operations are currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in microprocessors in its arithmetic and logic unit. In this chapter, we discuss different architectures for multiplication and the methods that improve speed and/or area. Also, it is important to consider these methods in the context of VLSI design. It is beneficial to find structures that are modular and easy to layout.

III. IMPLEMENTATION OF MULTIPLIER AND BUILDING BLOCKS

1: AND Gate:

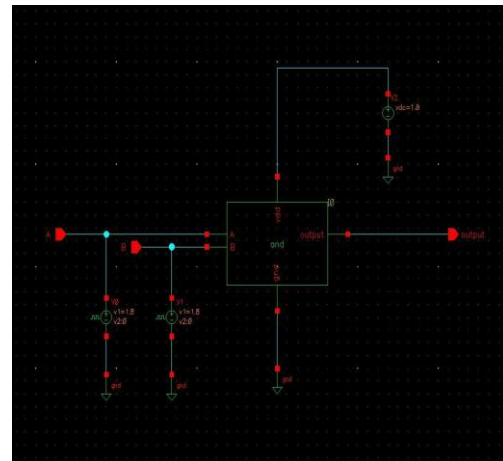
The Schematic of AND gate which is designed by using 6 transistors is shown in the below figure4 (a)

The test symbol of the AND gate is shown in the belowfigure 4(b).By using test symbol we can easily simulate the design as it contains input and output ports with simple architecture.



(a)

Fig 4: (a) Schematic of AND Gate



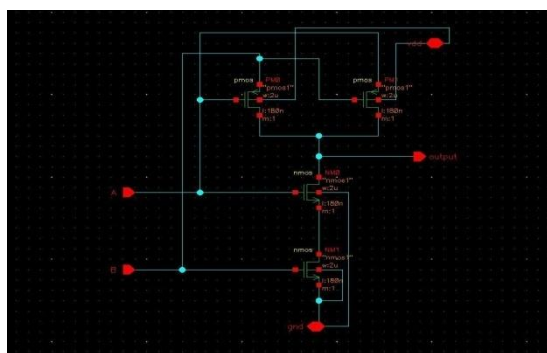
(b)

(b) Symbol of AND Gate

2: XOR Gate:

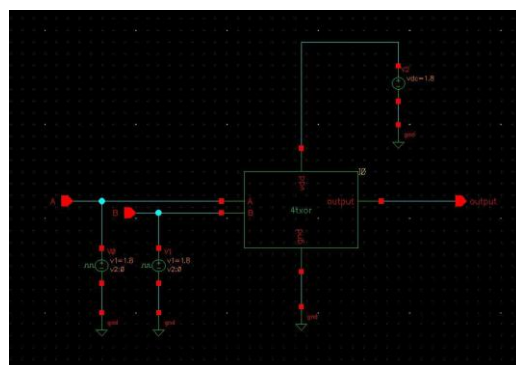
The Schematic of XOR gate which is designed by using 4 transistors is shown in the below figure 5(a)

The test symbol of the XOR gate is shown in the below figure 5(b).By using test symbol we can easily simulate the design as it contains input and output ports with simple architecture.



(a)

Fig 5: (a) Schematic of XOR Gate

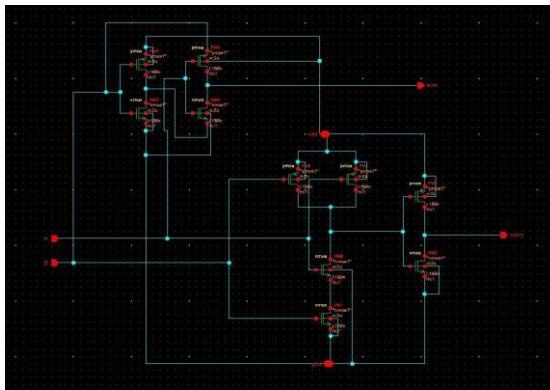


(b)

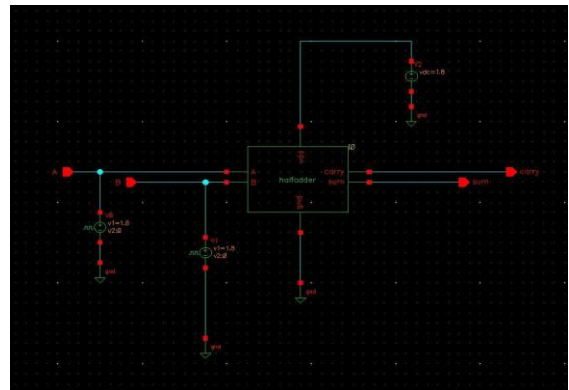
(b) Symbol of XOR Gate

3: Half Adder:

The Schematic of Half Adder which is designed by using XOR and AND gate is shown in the below figure 6(a). The test symbol of the Half Adder is shown in the below figure 6(b). By using test symbol we can easily simulate the design as it contains input and output ports with simple architecture.



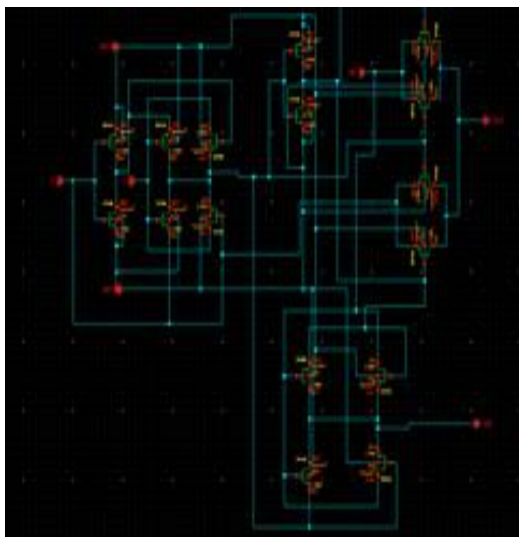
(a)
Fig 6: (a) Schematic of Half adder



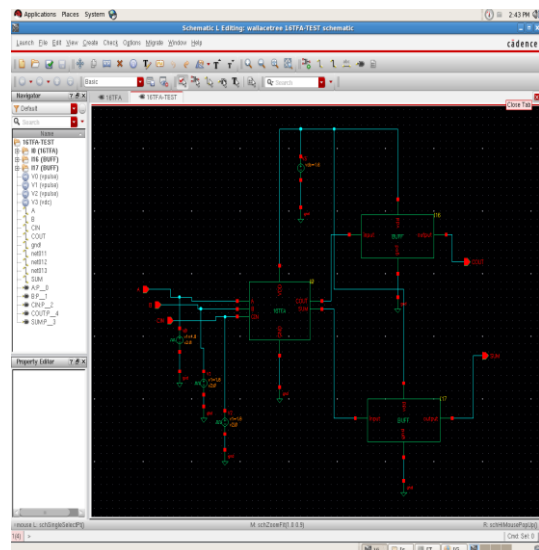
(b)
(b) Symbol of Half adder

4: Full Adder

The Schematic of full Adder which is designed by using 16 transistors is shown in the below figure 7 (a). The test symbol of the 16 transistors full Adder is shown in the below figure 7 (b). By using test symbol we can easily simulate the design as it contains input and output ports with simple architecture.



(a)
Fig 7: (a) Schematic of Full adder



(b)
(b) Symbol of Full Adder

5: Array Multiplier:

There is a one to one topological correspondence between this hardware structure and the manual multiplication

The Schematic of Array Multiplier which is designed by using 16 transistors full Adder is shown in the below figure.8 (a).The test symbol is shown in figure 8(b).

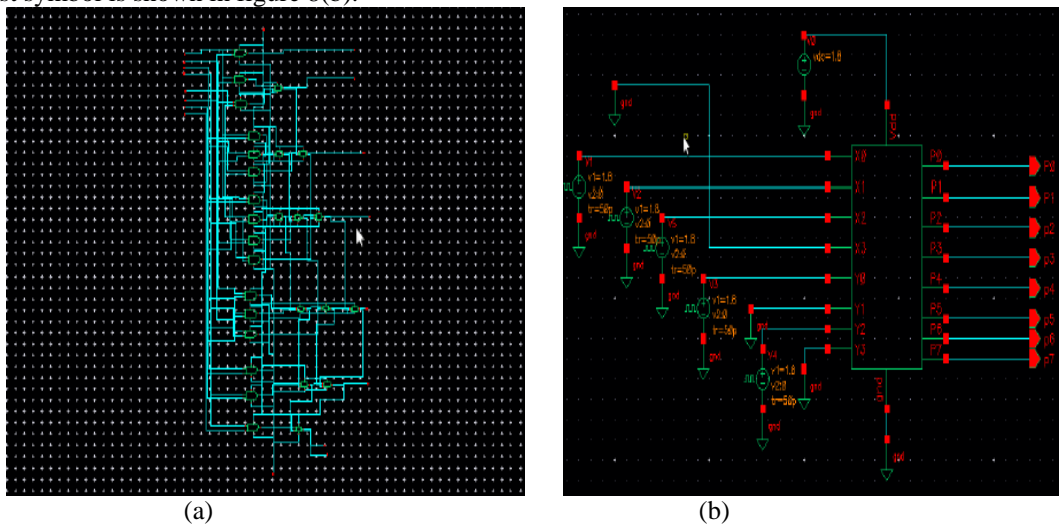


Fig 8: (a) Schematic of Array Multiplier

(b) Symbol of Array Multiplier

6.Wallace Tree Multiplier:

The new design obtained for Wallace tree multiplier that has the reduced number of half and full adders resulted in a reduced number of AND & OR gates

The Schematic of Wallace Tree Multiplier which is designed by using 16 transistors Full Adder is shown in the below figure 9.

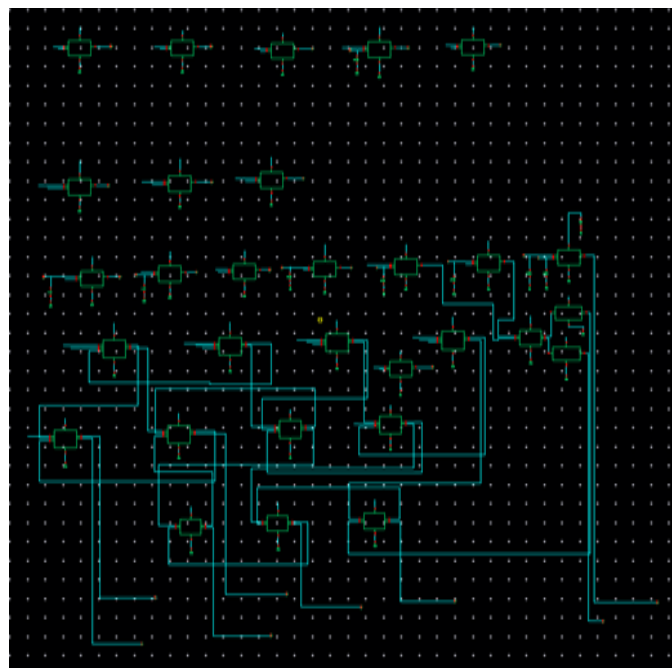
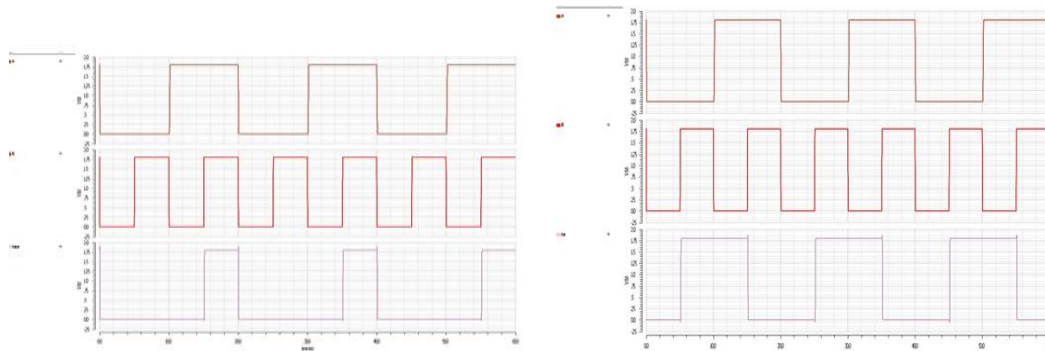


Fig 9: 4*4 Wallace tree Multiplier

IV.SIMULATION RESULTS

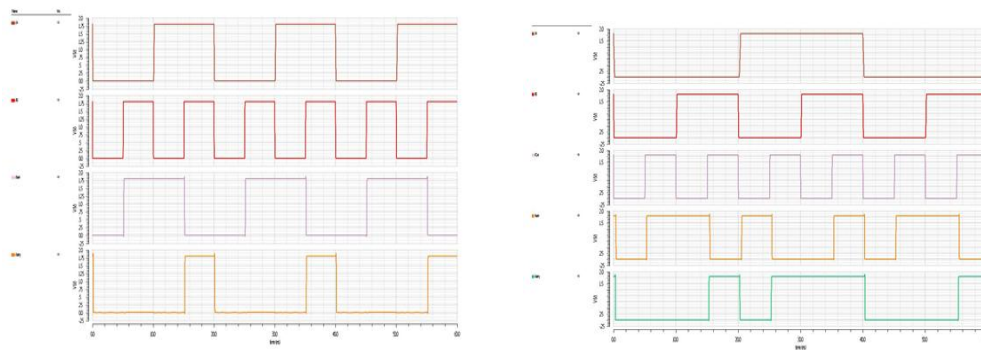
The below figures shows the Simulation results of all the blocks of multiplier which are simulated in Cadence 180nm technology. Figure 10 (a) represent the transient analysis of 2 inputs AND gate with input and output waveforms and figure 10 (b) shows the transient analysis of XOR gate with input and output waveforms



(a)
Fig 10: (a) AND gate Output

(b)
(b) XOR gate output

Figure 11(a) represents the transient analysis of half adder with a ,b as inputs and sum, carry as outputs and (b)represents the full simulation results of full adder with a , b , c as inputs and sum ,carry as outputs which are simulated by using cadence virtuoso tool 180nm technology



(a)
Fig 11: (a) Half Adder Output

(b)
(b) Full adder output

The transient analysis of a 4-bit Array multiplier is done by applying two inputs each of 4-bit. Input and output transient waveforms for the multiplier are shown in the Fig.12 respectively. Cadence virtuoso tool is used to simulate the design in 180nm technology.

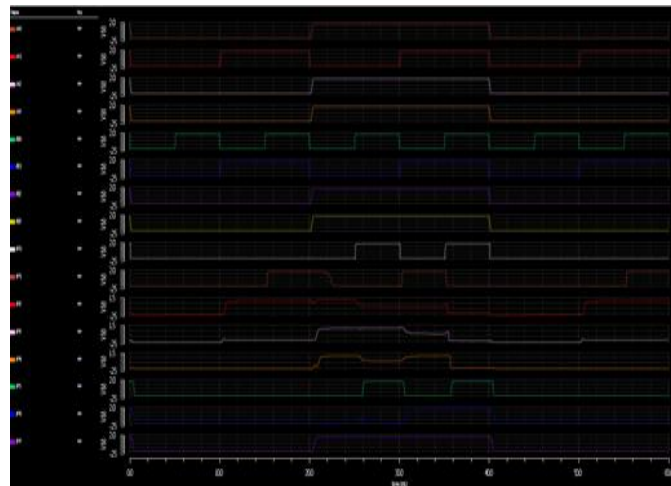


Fig 12: Array Multiplier Output

The transient analysis of a 4-bit Wallace multiplier is done by applying two inputs each of 4-bit. Input and output transient waveforms for the multiplier are shown in the Fig.12 respectively. These results are simulated using Cadence Virtuoso tool in 180nm technology.

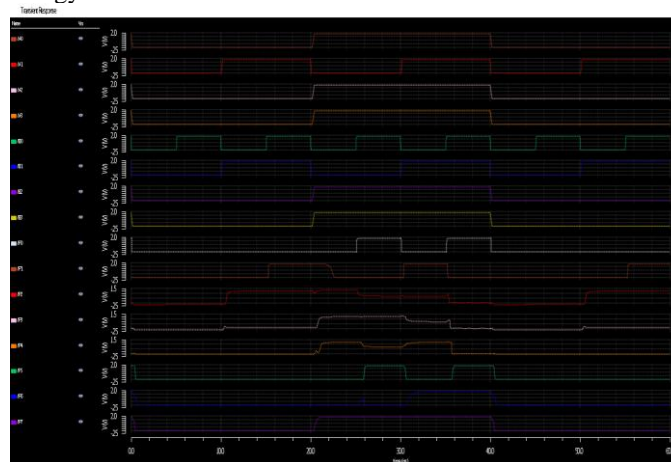


Fig 13: 4*4 Wallace tree Multiplier

Comparison between Transistor counts, power consumption of different multiplier architectures shown in below table. Comparison shows that the proposed Wallace tree multiplier using full adder in consumes less power when compared to Array multiplier with less number of transistors

Table 1: Comparative Analysis of Multiplier Architecture between power and Transistor Count

Circuit	Transistor Count	Power
Full adder	16	17.53 μ w
16t full adder based Array Multiplier	288	446.5 μ w
16t full adder based Wallace tree Multiplier	262	134.7 μ w

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V.CONCLUSION

In this project, we presented design and implementation of 4-bit unsigned different multiplier architectures such as Array multiplier and Wallace tree multiplier. The multiplier architectures are implemented in Cadence EDA tool. The simulation results match the expected results with accuracy. The main aim to optimize the the multiplier architectures are design in terms of area and power. The performance of the different multiplier circuits are analyzed in terms of parameters such as transistor count and power consumption.

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