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Variable Body Biasing Technique to Reduce Leakage Current in 4x4 DRAM in VLSI

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ABSTRACT : As the technology is improved to support very large chip sizes, the system designers have faced with power consumption and leakage current problems. The CMOS technology has increased in level of importance to the point where it now clearly holds center stage as the dominant VLSI technology. The Self controllable Voltage Level (SVL) technique is used in DRAM 4×4 (Dynamic Random Access Memory) to reduce leakage current. By using SVL technique the leakage current reduce up to some extent. Further the Variable body biasing technique (VBB) is used to reduce ultra low power consumption and leakage currents. By using Body Biasing technique threshold voltage can be controlled. With the increase of the threshold voltage leakage current decreases resulting in a decrease in Static Power or Leakage power. The sleepy transistors are used to achieve ultra low leakage power consumption. When the circuit is in active mode, there is now voltage difference between the body and source in the sleep transistors as the added transistors are ON and also offer no resistance between the body and source which means body and source are short. When the circuit is in sleep mode there is a high resistance between body and source resulting in a higher threshold voltage (V_{th}). Consequently, the leakage power consumed reduces. Moreover, due to low V_{th} during active mode delay remains in a reasonable range. The simulation result shows that the power consumption has been reduced by using Variable Body Biasing technique compared to SVL technique for implementing DRAM.

KEYWORDS: DRAM, self controllable voltage level technique, Variable body bias technique, VLSI.

I. INTRODUCTION

In Computer system there are various types of memory utilization techniques with different access time. The main memory is usually the most rapidly accessible memory. The main memory is usually of the random access type. the random access memory is one in which the time required for storing (writing) information and for retrieving (reading) information is independent of the physical location (within the memory) in which the information stored. The bulk of memory chip consists of the cells in which the bits are stored. '1' the capacitor is charged to ($V_{DD}-V_t$). When a '0, is stored, the capacitor is discharged to a zero voltage. Because of leakage effects, the capacitor charge will leak off, and hence the cell must be refreshed periodically. During refresh the cell content is read and the data bit is rewritten, thus restoring the capacitor voltage to its proper value. The refresh operation must be performed every 5ms to 10ms. Dynamic RAM is volatile that is they require the continuous presence of a power supply. The memory access time is the time between the initiation of a read operation and the appearance of the output data. Memory operation is usually taken to include both read and write.

II. RELATED WORK

This paper shows how to reduce the leakage current in 4x4 DRAM by using Self controllable Voltage Level technique [1]. The papers have constructed a measurement system which can make automatic remote monitoring of leakage current data using the Internet [2]. Method to approximation the difference of leakage current due to both intra-die and inter-die gate length development changeability [3].The research is apprehensive with the investigation of leakage

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current [4]. The paper introduces a input vector method for leakage current [5]. The paper shows a lithography process-aware edge effects improvement method to reduce the leakage current in the shallow trench isolation (STI) [6]. The paper gives the address the rising concern of gate oxide leakage current (gate) at the circuit level [7]. The reduction of interface situation densities and the improvement in oxide regularity would be the possible reasons for the reduction in leakage currents of samples [9]. The paper gives a high-performance bipolar CMOS-technology for an 1- M bit DRAM [10].

III. EXISTING SYSTEM

The 4x4 DRAM consists of four word lines and four bit lines. If word line one (WL1) is ON then the entire row will be in conductive mode and all the transistors in word line one are in ON mode. If we want to store the data in transistor one then first the WL1 is activated and the data is given to the bit line one (BL1). The output is observed at S1 as shown in figure. If '1' is given as input the capacitor stores the data and '0' is given as input then the capacitor is discharged. By using 4x4 DRAM we can store large amount of data. The 4x4 DRAM circuit as shown below

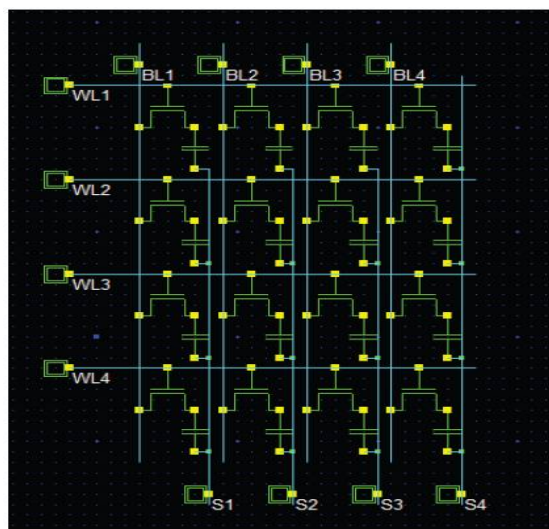


Figure 1: Schematic of 4x4 DRAM

The 4x4 DRAM is implemented with the Self controllable Voltage Level Technique (SVL) to reduce leakage current present in the DRAM. The circuit of DRAM with SVL technique is shown below. The lower SVL Technique is used to reduce the leakage current of 4x4 DRAM circuit. SVL circuit consists of one NMOS and one PMOS transistors connected in parallel. The upper SVL technique is connected in between VDD and the bit line of the circuit. Source of N and PMOS transistors are connected to VDD and drains of the transistors are connected to bit line of the DRAM circuit.

Technology scaling is one of the driving forces behind the tremendous improvement in performance, functionality, and power in integrated circuits over the past several years. Power dissipation has become a very critical design metric with miniaturization and the growing trend towards wireless communication.

For deep-submicron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. Leakage current is the current that flows through a transistor when it is switched off. It depends on gate length, oxide thickness and varies exponentially with threshold voltage, temperature and other parameters

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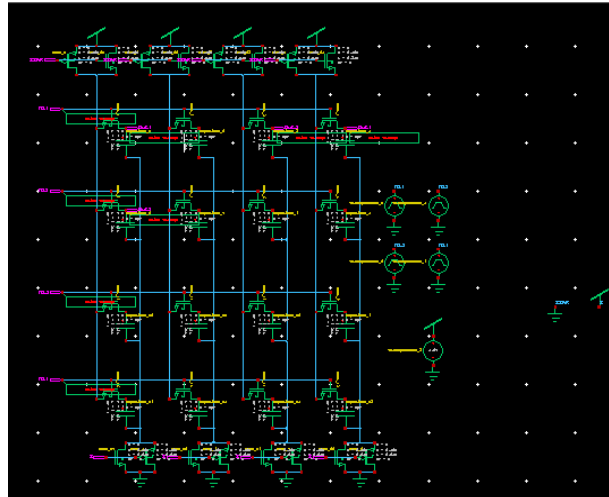


Figure 2: Schematic of DRAM with SVL Technique

SVL technique is of three types. They are upper SVL technique which is used to reduce the power consumption of the circuit in active mode. The lower SVL Technique is used to reduce the leakage current of 4x4 DRAM circuit. SVL circuit consists of one NMOS and one PMOS transistors connected in parallel. The upper SVL technique is connected in between VDD and the bit line of the circuit. Source of N and PMOS transistors are connected to VDD and drains of the transistors are connected to bit line of the DRAM circuit.

The lower SVL circuit is connected between the ground and load circuit. Output line is connected to the drains of the SVL circuit and sources are connected to the ground. By using SVL circuit we can reduce leakage current up to some extent and voltage delay is also present in 4x4 DRAM with SVL circuit. To reduce more leakage current and power consumption Variable Body Biasing technique is proposed.

IV. PROPOSED SYSTEM

The 4x4 DRAM is proposed with the Variable Body Biasing (VBB) Technique. The VBB technique is applied to the DRAM circuit. The Upper VBB circuit is consists of two PMOS and one NMOS transistors are connected between VDD and all bit lines of the DRAM circuit. Lower VBB circuit consists of two NMOS and one PMOS transistors are connected between outputs of the DRAM circuit and ground.

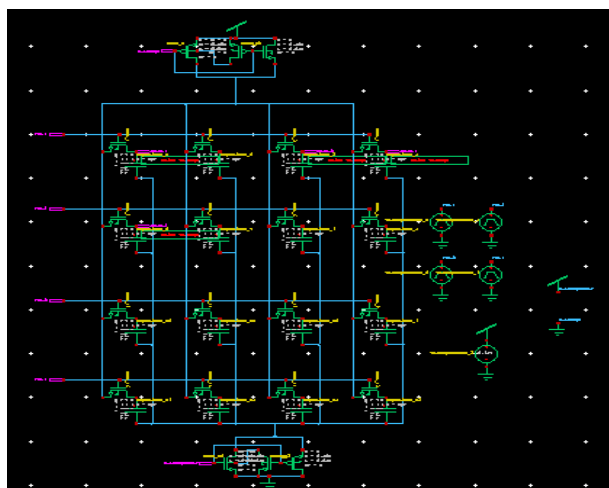


Figure 3: Schematic of 4x4 DRAM with VBB Technique

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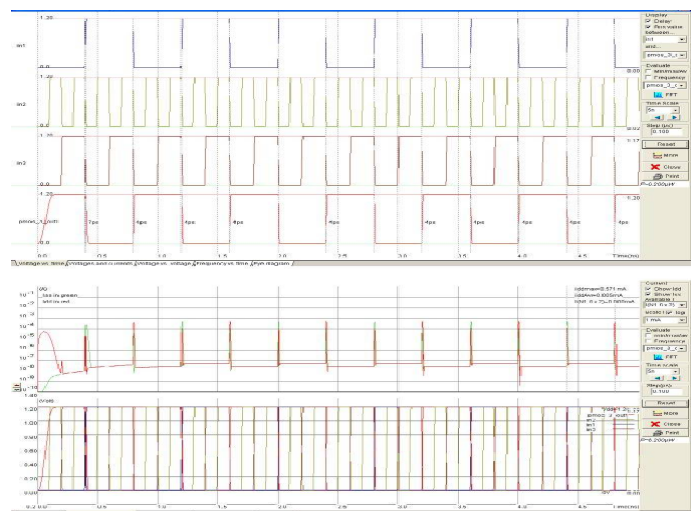
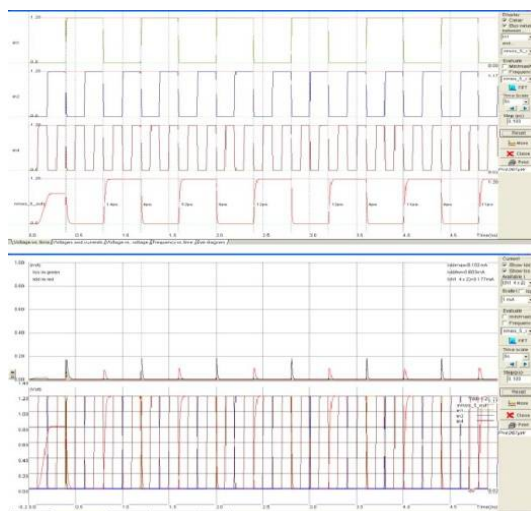
By using VBB technique power consumption is reduced in active mode and leakage current is reduced in standby mode of the DRAM circuit. Variable-threshold circuits dynamically control the threshold voltage of transistors through substrate biasing and hence overcome shortcoming associated with multi-threshold design. When a variable-threshold circuit is in standby, the substrate of NMOS transistors is negatively biased, and their threshold increases because of the body-bias effect.

Circuit	Power Consumption
Conventional DRAM 4x4	1.249005e-004 watts
Proposed DRAM 4x4 with SVL	3.366790 e-005 watts
DRAM 4x4 with Variable body bias technique	1.593818e-008 watts

Similarly the substrate of PMOS transistors is biased by positive body bias to increase their V_t in stand-by. Variable-threshold circuits can, solve the quiescent/static leakage problem, but they require control circuits that modulate substrate voltage in stand-by. Fast and accurate body-bias control with control circuit is quite challenging, and requires carefully designed closed-loop control. When the circuit is in standby mode the bulk/body of both PMOS and NMOS are biased by third supply voltage to increase the V_t of the MOSFET as shown in the Figure .

V. SIMULATIONS AND RESULTS

In this section, simulations of the proposed methods are shown. Simulations are obtained in Microwind Tool. First step in obtaining the simulations is to compile the Verilog file in Microwind 3.1. Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in Microwind 3.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in Microwind. After that simulations are performed on the layout. Simulations of proposed methods are shown below in figures.



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Simulations shown in these figures include the waveform of Voltage vs. Time and Voltage vs. Current. The corresponding simulations of sleep transistor approach with NMOS are shown in Figure. It can be observed from waveform that the performance obtained from the sleep transistor approach with NMOS is very good as compared to conventional sleep transistor approach. Delay is also less and maximum current in this new approach is more.

VI. CONCLUSION

The implementation of 4x4 DRAM with SVL technique reduces leakage current up to some extent but by using Variable Body Biasing technique the leakage current can be reduced up to 74%.

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