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FPGA Implementation of Background Subtraction and Image Threshold method for Object Detection

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ABSTRACT: Object Tracking is a procedure of locate the object to associate the target in successive video frame over time and it finds wide scale applications in the field of security and surveillance, video communication, augmented reality, traffic control, medical imaging etc. This paper describe an image detection technique by background subtraction algorithm was developed to identify moving objects from a stable system in which visual inspection plays a major role. Among all presented algorithms running average mean algorithm after subtraction was selected due to low computational difficulty which is the major factor of time in VLSI. The concept of the background subtraction is to subtract the existing image with respect to the reference image and compare it with to the certain threshold values. At this time we have written the core Processor SPARTAN-6 is intended in Verilog-HDL (VHSIC hardware description language), implemented using XILINX ISE 14.2 Design suite the algorithm is written in system C Language and tested in SPARTAN-6 FPGA kit. Area and the speed of the algorithm are also evaluated.

KEYWORDS: Image features, FPGA, and Matlab, Background Subtraction, Micro blaze, Object Detection, UART, VHDL.

I. INTRODUCTION

Extracting moving objects from image sequences is basic problems in computer vision systems that are utilized in a variety of applications, such as video surveillance, human tracking, movement examination and image synthesis .To sense the object, we use methods such as background subtraction [1], inter –frame difference and optical flow. The frame difference method is highly adaptable to dynamic environments, but in general it is not a good option to extract the complete forms of certain types of objects in motion. The optical flow [2] is an approximation of the movement of the local image and specifies how much each pixel of the image moves between the adjacent images. Optical flow is a very complex algorithm, which requires high memory resources and is also difficult to apply in real time due to its high computational cost. In most cases, a fixed camera is used, which means that background subtraction techniques can be complete object detection. The simplest implementation of background subtraction is to estimate the difference between a background image and the current image in a pixel mode, and then determine the difference value to determine the pixels that belong to moving objects.

Common background subtraction process includes the average execution pattern (RA), the Gaussian GMM mixing model, and the non-parametric methods of the kernel [2]. Even though GMM and non-parametric methods are stable algorithms, their complication makes it likely to execute them through the hardware approach. RA is also a stable algorithm, but its signal processing is more manageable for hardware implementation due to the unique mode of statistical modeling. Moving item following is the essential application goes under picture preparing. Serial handling for complete System on a Chip (SOC) inserted item improvement, while FPGA offers very adaptable, parallel preparing for a System on Programmable Chip (SoPC) advancement for verification of idea at developmental phase of the framework outline, prompting model that can be made at a later stage before the last Application Specific Integrated Chip (ASIC) usage. The FPGA contains a few rationale segments that can be customized as pre prerequisite to do

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complex computational capacity. This quality makes them exceedingly reasonable for planning network executing calculations. Along these lines FPGAs are chosen to do the Image preparing calculations.

There are two methodology in FPGA based preparing firstly it is conceivable to exchange the memory-based methodology from programming based picture handling to FPGAs. This may have little advantages, as it is conceivable to have a high parallelism with FPGAs. Be that as it may, it is likewise required to have a lot of memory accessible. Besides, the read and compose paths of such a memory can turn into a restricting element because of high parallelism. This sort of picture handling is frequently alluded to as disconnected from the net picture preparing. The second approach is stream-based handling. Rather than perusing and composing picture information from and to the memory, the picture information is spilled line-wise, pixel after pixel, through equipment segments.

In stream preparing, the equipment framework is timed with an altered pixel clock. With each clock cycle, another pixel is spilled into an equipment part. The equipment part as a rule has a yield of one pixel esteem for every clock cycle. This should effectively be possible in one clock cycle. This sort of picture handling has a few ramifications that should be considered when planning stream-preparing calculations. The most serious ramifications are that it is impractical to stop the info. The second ramifications are that irregular pixel access is impractical. At the point when taking a shot at a picture in the memory, all pixels of the picture can be gotten to. In the spilling mode, pixels that take after the present pixel are not accessible yet, and pixels that went before the present one must be put away keeping in mind the end goal to secure further get to.

In this paper we proposed a technique commonly used for the segmentation of movement in static images. It will detect moving regions by subtracting the current pixel per pixel from a reference background image that is created by mediating images over time in an initialization period. The basic idea of the background subtraction method is to first initialize a background and then subtract the current frame in which the moving object is present, that the current frame is subtracted with the background frame to detect the moving object. This method is simple and easy to capture and accurately extract the characteristics of the target data, but is sensitive to changing the external environment, so it is applicable to the condition that the background is known.

II. OBJECTIVE OF THE PROJECT

The scope of project is to do research in image processing techniques and algorithms. The techniques which can be implemented on FPGA for the optimizing in Speed of operation, resource utilization, memory requirements and algorithms used to extract objects The possible implementation of tracking objects and anticipating there further location to reduce the overall resource requirements on processor. A reliable and robust background subtraction algorithm should handle:

1. Sudden or gradual illumination changes,
2. High frequency, repetitive motion in the background (such as tree leaves, flags, waves.), and
3. Long-term scene changes (a car is parked for a month).

III. ALGORITHMIC DEVELOPMENT

The following modules construct the Object Tracking System:

1. Separating image frame on time frame and storing in BRAM
2. Object extraction by difference between frames (Background Subtraction algorithm)
3. Thresholding on mean value bases. (Threshold Method)
4. Trace Identification and display.

Object Tracking System

1. Separating Image Frames and storing in BRAM of is achieved by the fact the video is made of image frames. This image frames are break down into its color constituents of base colors (R,G,B). The value of intensity of

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these basic components gives an illusion of color of that particular spot. The image here is considered in 2D matrix with pixel size of 64x64 pixels. This is stored in block RAM as an input to algorithms.

- The Object extraction (background subtraction algorithm)

The alienating of object pixels as compared to pixels on same location as compared with previous image is done in this step and after we separate the image frame on time bases. The current image is treated as foreground image and it is denoted by $F_k(x, y)$. and the hold frame of time $k-1$ is denoted by $B_{k-1}(x, y)$. This hold frame is the base image or background image over which changes has to be detected. After obtaining the background image $B_{k-1}(x, y)$, we subtract the background image $B_{k-1}(x, y)$ from the current frame $F_k(x, y)$ as shown in Figure 1.

```

if (m==64) && (n==0) begin
for (s1=0;s1<64;s1=s1+1)
begin
for (s2=0;s2<64;s2=s2+1)
begin
high[s1][s2]=image[s1][s2]-image2[s1][s2]; // high as difference image stored in temp name
end
end
end

```

Figure:- 1 Difference of Image program flow for image of pixel [64] x [64] resolution

- Thresholding on mean value bases. (Threshold Method)

If the pixel difference is greater than the configured threshold T , then it determines that the pixels appear in the moving object, otherwise, as background pixels. The Algorithmic sequence is as shown in Figure 2. The moving object can be detected after the threshold operation. Its expression is the following:

$$Dk(x, y) = \begin{cases} 1 & |Fk(x, y) - Bk - 1(x, y)| > T \\ 0 & \text{others} \end{cases}$$

Threshold Expression

```

201 always@('Pixel start definations')
202 begin
203 if('Init Rows & Column with value 64')begin
204 for (p=0;p<64;p=p+1)
205 begin
206 for (q=0;q<64;q=q+1)
207 begin
208 Adaptive mean= mean value +Difference[p][q];
209 end
210 end
211
212 always@(posedge clk)
213 begin
214 if('Pixel value limits'))begin
215 if(mean comparison with base value >=32'h000000FF)
216 begin
217 if(l<64)begin
218 if(k<64)begin
219 addracl=addracl+1'b1;
220 weacl=1'b1;
221 extract image from pixel = high[l][k];
222 k<=k+1;
223 end
224 end

```

Figure:- 2 Program flow for Threshold check of result image and considering validity of extracted object

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Where $D_k(x,y)$ is binary image (which is calculated by differential image result). T is a gray scale threshold; its size determines the accuracy of the identification of the object. Since algorithm T is a fixed value, only for an ideal situation, it is not suitable for complex environments with changing lighting. Therefore, this document proposes the dynamic threshold method, dynamically changing the threshold value according to the variations in the illumination of the two images obtained.

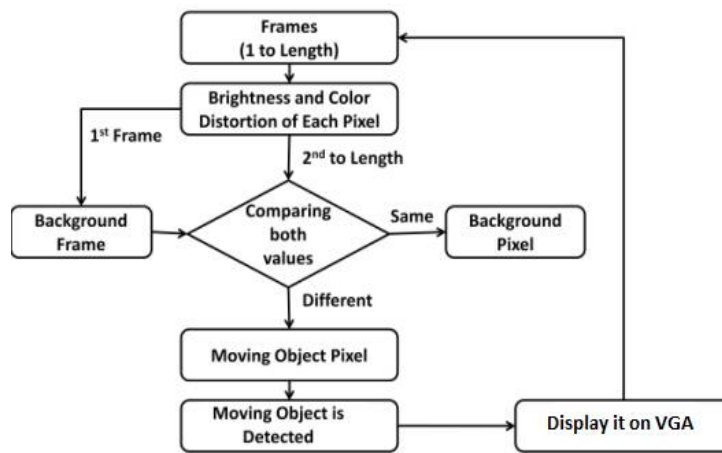


Figure:3 The flow chart of moving object detection.

4. Trace Identification and display.

After the object detection we have to display it on VGA display. This image pixel is then stream on VGA display and then result is shown. Through observation, we can find that when an object appears on the move appears on the scene.

IV. HARDWARE IMPLEMENTATION

The hardware part, used mainly for the VGA part, was developed in Xilinx Spartan-3E FPGA (XC6SLX9, FG414). The frequency of the system is 50MHz. Our Vga controller communicates with the bus through the Fast Simple Link (FSL). In our project, data should only be sent to the VGA driver if the data is prepared for FSL and memory access is not required. BRAM is used only for data storage and software instructions. The VGA port on the SPARTAN-6 card uses 10-pin FPGA signals to create an 8-bit color VGA port and two standard synchronizations (VS-Vertical Sync). There are eight signal levels in the red and green VGA signals and four levels in blue, so you can see 256 different colors, one for each of the 8-bit input data. The image on the screen is obtained by continuously refreshing the pixel from top to bottom of the lower right corner. Both synchronization signals and pixel color signals must be generated so you can track what you want on the screen.

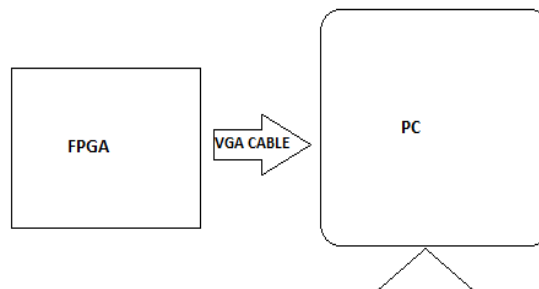


Figure:-4 Block diagram of proposed system.

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In our project, we use the VGA driver to generate VGA display and sync signals to generate color signals for each pixel. The block diagram of the VGA part is shown. The VGA driver has to retrieve and apply video data to the screen just as the electronic beam moves through a given pixel. Therefore it has to generate HS and VS timing signals and coordinate the output of pixel data as a function of the pixel clock.

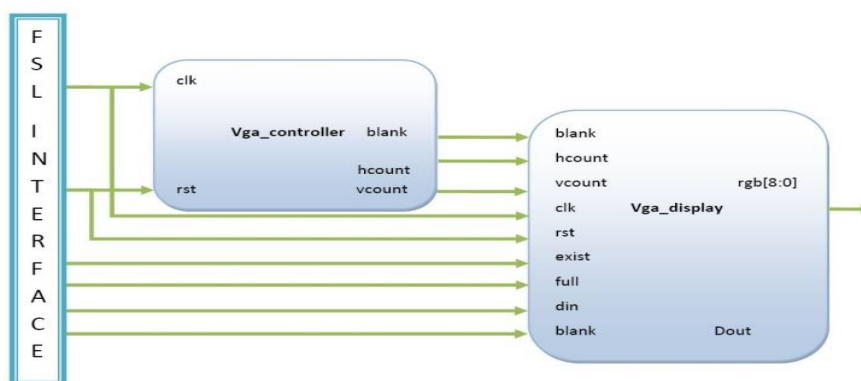


Figure:-5 VGA Block diagram

V. EXPERIMENTAL SETUP AND RESULTS

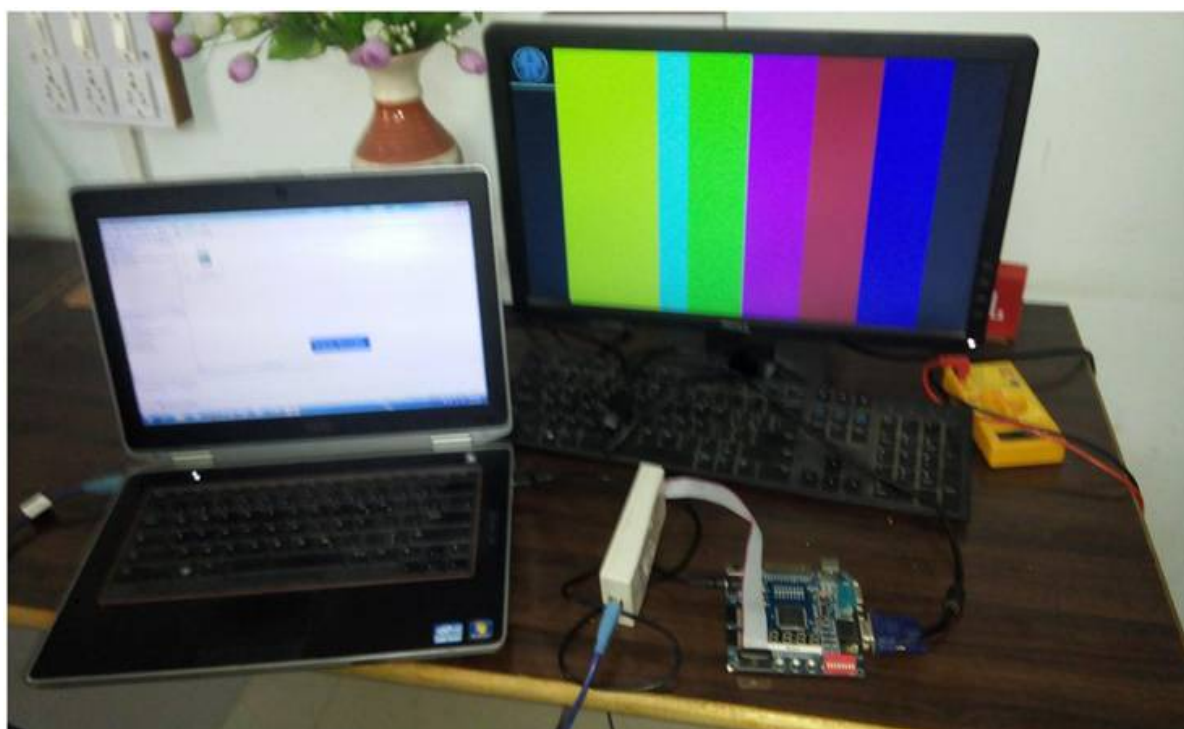


Figure:-6 experimental setup for project.

In this experiment we can see in figure that FPGA is connected to VGA connector and the result is shown on left corner of screen. The program is downloaded or burned on FPGA using JTAG USB cable. Then the PROM used for booting of FPGA with always holds the background subtraction program. The Clear image of object extracted form

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the black background / stable background is obtained. The object can be identified due to high difference in the mean value of its luminance as compared to the background image. As compare to Hybrid back ground subtraction method ,Horprasert model and blob detection Algorithm which utilizes 6% , 47% and 2% onVertex at 100 MHz frequency respectively of available hardware resource and 4 block RAM for complete processing, this experiment setup use only 1% of hardware and 2 block RAM when implemented over in Xilinx Spartan-3E FPGA (XC6SLX9, FG414) where the frequency of the system is 50MHz.

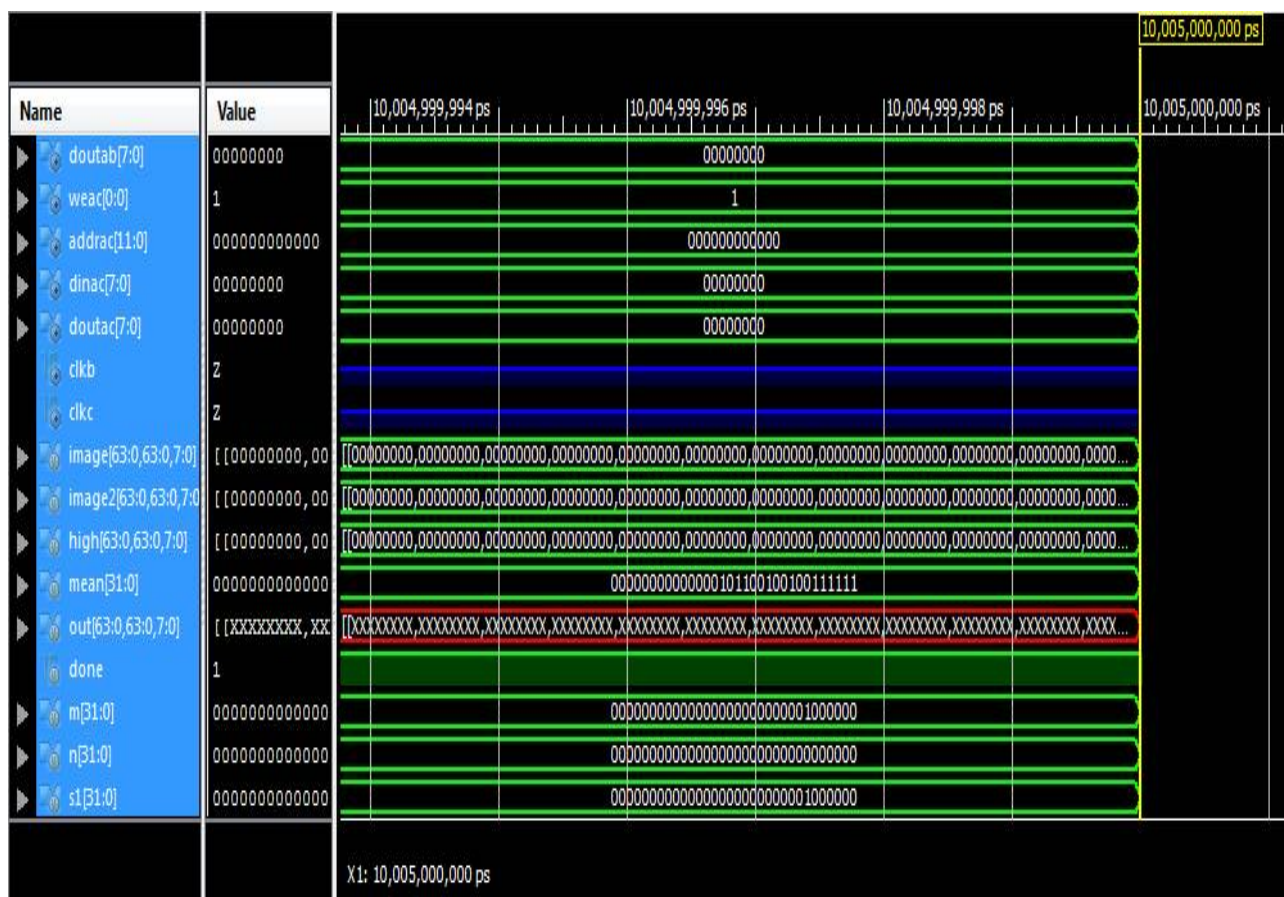


Figure:-7 Simulation of output of object subtraction.

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Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	78	12480	0%
Number of Slice LUTs	119	12480	0%
Number of fully used LUT-FF pairs	75	122	61%
Number of bonded IOBs	2	172	1%
Number of Block RAM/FIFO	3	26	11%
Number of BUFG/BUFGCTRLs	1	32	3%

Figure:-8 Area used by proposed system

Table 1 gives a comparative study of some methods used for background subtraction application to detect object is compared in below chart. For the system used for applications like surveillance / security or in thermal imaging or night vision sensors where the object is present in monochromatic format the Proposed method proves to be superior over the existing methods. In terms of the block RAM or flip flops used, LUT and Registers memory used in the method.

Study Parameters	Method Implemented	Background subtraction based on Horprasert Model[13]	Blob detection algorithm [11]	Hybrid Background Modeling and subtraction [12]
Number of Block RAM	2 Block RAM (1%)	8 Block RAM (6%)	4 Block RAM in Vertex V (100 MHz)	6 4 (47%)
Slice Registers and Slice LUT's	Almost ~ 0%	4% LUTs 2784/69k	More than 1% area as compared to First method	191/128k <1% 313/63k <1% But Higher than Column 1
Power Utilization	Less than 11 mw	More than Blob detection and Hybrid modeling	More than Implemented subtraction method	91 mw

Table:- 1 Comparison study of Implemented method with other methods

VI. CONCLUSION

In this document, a reconfigurable system based on background subtraction is designed using the XILINX ISE 14.1 tool. The hardware architectures of the moving object detection algorithm have been implemented. This type of work that uses FPGA can be extended to other applications of the integrated system. Mainly for surveillance and security purposes where cost v/s system performance is critical. This type of work using FPGA SPARTAN XC6SLX9 can be extended to other applications of integrated systems. As we can see from the comparison chart the object detection using background need only two block RAM (1%) but as compared to the blob detection, Hybrid method and method based on Horprasert system this figure is less and more efficient considering the FPGA model and clock

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frequency. The Slice Registers and LUTs are also compared and found less required in the experimented model as compare to other two algorithms. This shows that the power requirement also comes in ascending order from implemented method to the Hybrid method. Thus making the system efficient in its area as well as power efficient factor as compare to other algorithm.

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