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Design of Modified Carry Select Adder with Low Power and Efficient Area Using D-Latch

B. Vijaya Lakshmi, B. Praveen Kumar

M. TECH Student, VLSI Design, Department of Electronics and Communication Engineering, Sri Aditya College
of Engineering and Technology, India

Assistant Professor, Department of Electronics and Communication Engineering, Sri Aditya College of Engineering
and Technology, India

ABSTRACT: Carry select adder (CSLA) is a one of the high speed adders used in many computational systems to perform fast arithmetic operations. Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method which replaces the BEC using D latch. Experimental analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

KEYWORDS: Low Power, CSLA, Area Efficient, BEC, Multiplexer.

I. INTRODUCTION

Design of area- and power - efficient high- speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry Propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. The carry Select adder (CSLA) provides a compromise between small areas but longer delay ripple carry adder (RCA) and larger area with shorter delay carry look-ahead adder. CSLA uses multiple pairs of ripple carry adder (RCA) to generate partial sum and carry by considering carry multiplexers. The modified CSLA using BEC has reduced area and power consumption with slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by D latch with enable signal. The proposed architecture reduces the area, delay and power. This paper is organized as follows section III presents the detailed structure and the function of the binary to excess-1 convert logic. Section VI and Section V explains the regular and modified CSLA respectively. Deals with the proposed architecture. Results are analyzed in the section VII. Section VIII concludes.

II. LITERATURE REVIEW

Bedrail 1962 proposes (1) that the problem of carry propagation delay is overcome by independently generating multiple radix carries to select between simultaneously generated sums. Ram Kumar 2010 (2) proposed a BEC method to reduce the maximum delay of carry propagation in final stage of carry save adder. Ram Kumar and Harish 2011 (3) propose BEC technique which is simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.

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III. BEC

To reduce the area and power consumption of regular CSLA, RCA with $C_{in}=1$ is replaced with BEC. An $n+1$ bit BEC replaces the n bit RCA. The function table of a 4-bit BEC is shown in Fig. 1 and Table 1 respectively. By the use of BEC logic, we can reduce the significant amount of silicon area reduction in the VLSI design. The Boolean expression of the 3-bit BEC is given below. $S_0 = \sim B_0$, $S_1 = B_1 \wedge B_2$, $S_2 = B_2(B_0 \wedge B_1)$

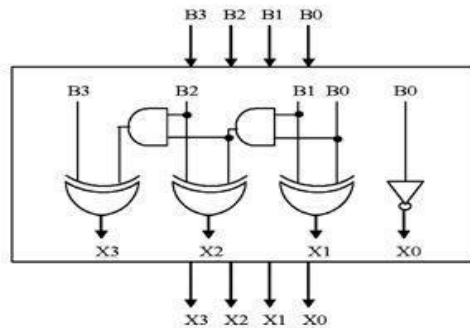


Fig. 1 4-Bit BEC

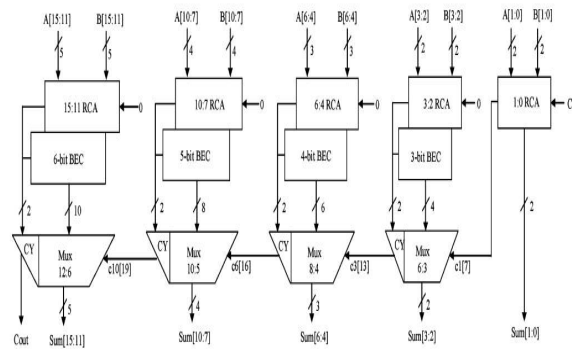


Fig. 6. Modified 16-b SQRD CSLA. The parallel RCA with $C_{in} = 1$ is replaced with BEC.

Fig: 2 modified SQRD CSLA

IV. REGULAR SQRD CSLA

The structure of the 16-b regular SQRD CSLA is shown in Fig. 5. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 2, in which the numerals within [] specify the delay values. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer. Internal structure of the group 2 of regular 16-bit CSLA is shown Fig. 3. By manually counting the number of gates used for group 2 is 57 (full adder, half adder, and multiplexer). One input to the mux goes from the RCA with $C_{in}=0$ and other input from the RCA with $C_{in}=1$. The group 2 has two sets of 2-b RCA. The arrival time of selection input c_1 [time (t) = 7] of 6:3 mux is earlier than s_3 [t = 8] and later than s_2 [t = 6]. Thus, sum_3 [t = 11] is summation of s_3 and mux [t = 3] and sum_2 [t = 10] is summation of c_1 and mux.

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V .MODIFIED CSLA USING BEC

The structure of the proposed 16-bit SQR T CSLA using BEC for RCA with $C_{in}=1$ to optimize the area and power is shown in Fig.4. We again spilt the structure into five groups. The delay and area estimation of each group 2 is shown in Fig.5. One input from the BEC. Comparing the group 2 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA.

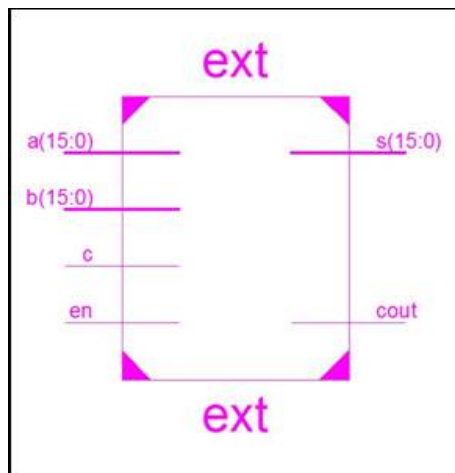


Fig: 3 Existences CSLA

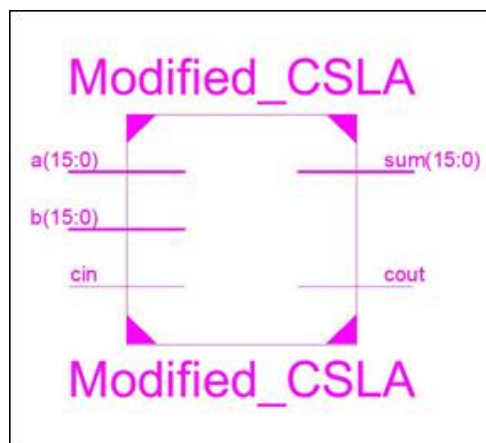


Fig: 4 Modified CSLA

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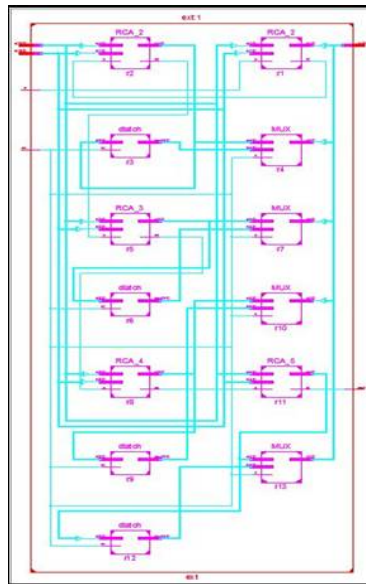


Fig: 5 Modified RTL diagram

VI. MODIFIED 16-BIT CSLA USING D-LATCH

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their inputs. D-latch and its waveforms are shown in Fig. 6 & 7. The architecture of proposed 16-bit CSLA is shown in Fig. 8. It has different five groups of different bit size RCA and D-latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two addition is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2-bit wide. The upper half of the adder i.e., most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig. it can understand that latch is used to store the sum and carry for $C_{in}=1$ and $C_{in}=0$. Carry out from the previous stage i.e., least significant bit adder is used as control signal for mux to select final output carry and sum of the 16-bit adder.

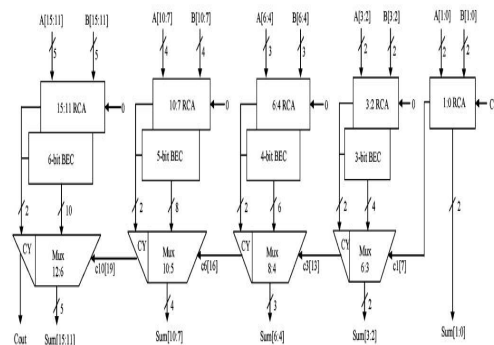


Fig. 6. Modified 16-bit SQR T CSLA. The parallel RCA with $C_{in} = 1$ is replaced with BEC.

Fig:6 Modified CSLA using d latch

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If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero. MSB adder is accessed. Cout is the output carry. The Fig.9 shows the internal structure of group 2 of the proposed 16-bit CSLA. The group 2 performed the two bit addition which is a2 with b2 and a3 with b3

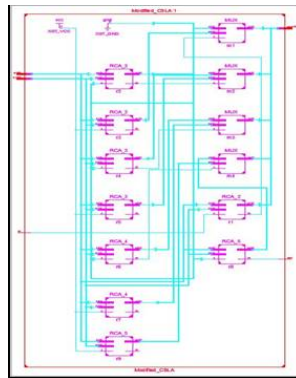


Fig7: Modified RTL diagram

This is done by two full adder (FA) named FA2 and FA3 respectively. The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2. The group 2 structure has five D-Latches in which four are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carry. Multiplexer is used for selecting the actual sum and carry according to the carry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer. When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the first D-Latch is not enabled. The second D-Latch store the sum with cin =0 by using inverted clock enable. When the clock is high, the addition is performed with carry is equal to one. The other D-Latches enabled and store the sum and carry for carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry.

VII .SIMULATION RESULTS

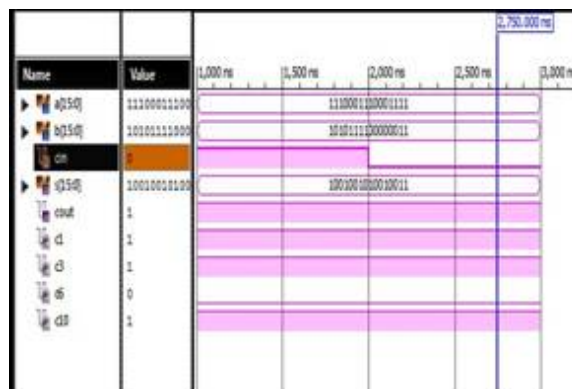


Fig.8 Regular SQR CSLA Simulation

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Fig.9 CSLA using BEC

Fig. 9. We change the MOSFET's configuration for the better results. Here we work on the current and voltage of the MOSFET's. We



Fig.10 Modified CSLA using D-Latch

Adder(16-bit)	Delay(ns)	Power(mW)	PDP($\times 10^{-12}$)
Regular SQRT CSLA	20.7	1710.63	35410.04
CSLAusing BEC	21.598	874.37	18884.64
Modified CSLAusing D-Latch	17.84	324.21	5783.906

TABLE I: COMPARISON

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In table we are discussing about the difference between the existences and modified that is delay, power.

VIII. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRD CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power (Table II). The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by the use of D-latches.

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