

Design and Simulation of 32-Bit Carry-Ripple Adder using HSPICE and Mentor Graphics

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ABSTRACT: An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N-bit parallel adder, there must be N number of full adder circuits. The main objective of this project work is to calculate power, area, delay, less than 40 pin-out count and get a Good Noise Margin. Complete design of this project consists of two main parts: (1) Serial-In and Parallel-Out (SIPO) shift register; (2) 32-bit Full adder. The design of Serial-In and Parallel-Out (SIPO) and Full adder for low power is obtained and the low power units are implemented on the carry ripple adder and the results are analyzed for better performance. The designs are done using Mentor Graphics tool and are simulated using HSPICE.

KEYWORDS: Full adder, HSPICE, Mentor Graphics, Delay, Schematic and Layout.

I. INTRODUCTION

Digital Adder is a digital device capable of adding two digital n-bit binary numbers, where n depends on the circuit implementation. Digital adder adds two binary numbers A and B to produce a sum S and a carry C. The Half Adder is a digital device used to add two binary bit 0 and 1. The half adder outputs a sum of the two inputs and a carry value.

$$0 + 0 = \text{Sum } 0 \text{ Carry } 0$$

$$0 + 1 = \text{Sum } 1 \text{ Carry } 0$$

$$1 + 0 = \text{Sum } 1 \text{ Carry } 0$$

$$1 + 1 = \text{Sum } 0 \text{ Carry } 1$$

Half Adder can be constructed from AND gate and XOR gate as shown below:

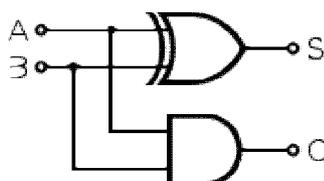


Fig 1.1: Half adder circuit

Full Adder is used to add three input binary numbers. Implementation of full adder is difficult compared with half adder. Full adder has three inputs and two outputs, inputs are A, B and Cin and outputs are sum 'S' and carry 'Cout'. In three inputs of the full adder, two inputs A and B are addend and augend, whereas third input Cin is carry on preceding

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Vol. 7, Issue 1, January 2018

digit operation. The full adder circuit generates a two-bit output and these are denoted with the signals namely S and Cout (where, $sum = 2XCout + S$).

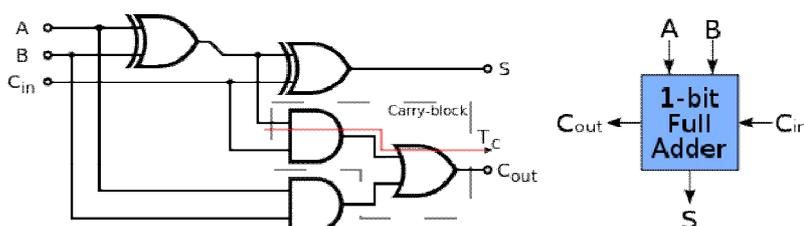


Fig 1.2: Full adder circuit and block diagram.

Truth table of Full adder is shown below:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Carry Ripple adder: It is possible to create a logical circuit using multiple full adders to add N -bit numbers. Each full adder inputs a C_{in} , which is the C_{out} of the previous adder. This kind of adder is a *carry ripple adder*, since each carry bit "ripples" to the next full adder. The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 32-bit ripple carry adder, there 32 full adders, so the critical path (worst case) delay is $32 * 3 = 96$ gate delays.

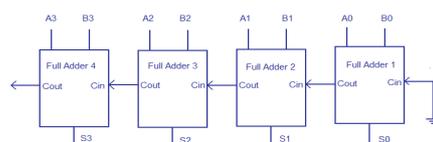


Fig 1.3: 4-bit Carry Ripple adder circuit

Serial-In Parallel-Out (SIPO) Shift Register: A serial-in/parallel-out shift register is similar to the serial-in/ serial-out shift register in that it shifts data into internal storage elements and shifts data out at the serial-out, data-out, pin. It is different in that it makes all the internal stages available as outputs. Therefore, a serial-in/parallel-out shift register converts data from serial format to parallel format. If four data bits are shifted in by four clock pulses via a single wire at data-in, below, the data becomes available simultaneously on the four Outputs Q_A to Q_D after the fourth clock pulse.

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Vol. 7, Issue 1, January 2018

The practical application of the serial-in/parallel-out shift register is to convert data from serial format on a single wire to parallel format on multiple wires. Perhaps, we will illuminate four LEDs (Light Emitting Diodes) with the four outputs ($Q_3 Q_2 Q_1 Q_0$).

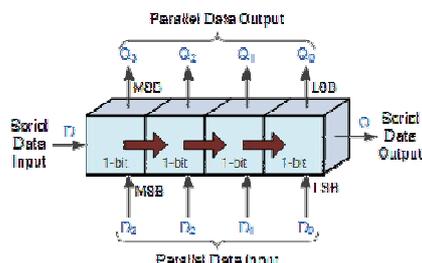


Fig 1.4: SIPO Shift Register

SIPO Shift Register is used along with the carry ripple adder in order to minimize the number of pin-out count while designing the circuitry. As shown below, as the clock gets HIGH, the output '1' at Q_a is obtained. When the clock gets HIGH again, Q_b equals '1' is obtained, and this goes on for Q_c and Q_d .

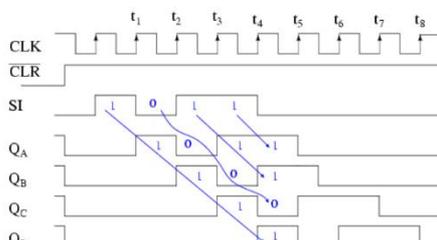
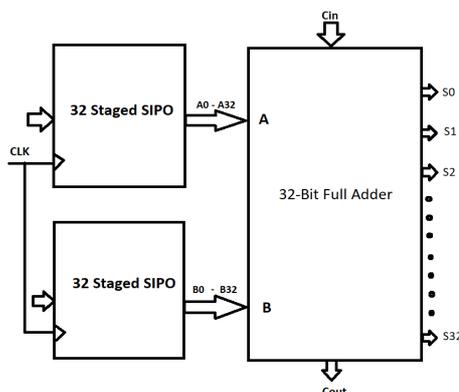


Fig 1.5: SIPO Waveforms

SIPO shift register is used in order to minimize the number of pin-out count to 39. This shift register uses D-flip flop and the output Q is given as the input to either A or B up to 32. Hence, two shift registers are used, one for input A and one for input B.

II. RELATED WORK



BLOCK DIAGRAM: 32-BIT CARRY RIPPLE ADDER

Fig 3.1: Design Approach

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Vol. 7, Issue 1, January 2018

1. **Creating Schematic:** All the gates and CMOS transistor are arranged in such a way to get a ripple carry adder. The transistor level circuit is made to form gate and gate level Schematic is used in creating full adder. Using full adder and SIPO shift register, carry ripple adder is created and finally carry ripple adder schematic is sketched.
2. **Generating Symbol:** For a simplified approach of the schematic, symbols are generated of simple basic transistor level schematic. These symbols are further used as instance in the bigger complex circuit to make the approach simple and convenient.
3. **Making Layouts:** The Mentor graphics IC layout editor is used for creating layouts according to the schematic. Different types of approaches are available for creating schematic. In this project the hierarchical approach is followed for the successful execution of the layouts.
4. **Extracting Parameters:** The Mentor graphics IC layout editor is used for creating layouts according to the schematic. Different types of approaches are available for creating schematic. In this project the hierarchical approach is followed for the successful execution of the layouts.
5. **Simulation:** The process of simulation includes execution of parameters extracted from layout in HSPICE. This step gives the result in the waveforms. The waveforms can be used to calculate the delay & power.

III. DESIGN PARTS

AND Gate: The AND gate is the basic building block required in the Ripple Carry Adder. The AND gate is also used for executing the carry part of the full adder.

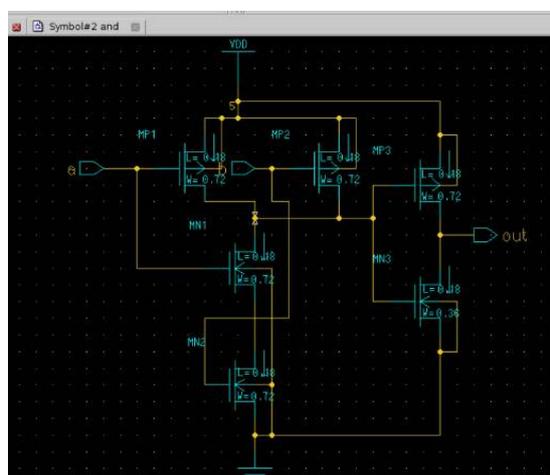


Fig 3.1: AND gate CMOS schematic

The above circuit is converted into symbol of AND gate using the Generate Symbol option in Mentor Graphics Schematic Editor. The layout of AND gate was created as shown below.

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Vol. 7, Issue 1, January 2018

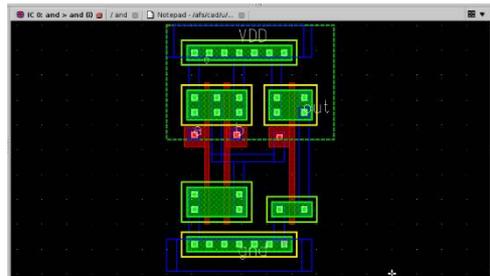


Fig 3.3: AND gate optimized layout

The output waveform of the designed AND gate is obtained which is shown below. Here it can be observed that it follows the AND logic, having a delay of 108ps.

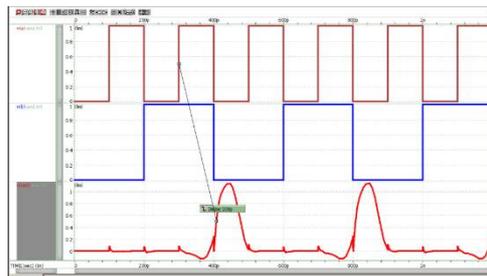


Fig 3.4: AND gate output waveform in WaveView.

OR Gate: The OR gate is further used in the circuit diagram of the full adder. Hence the schematic of the OR gate is created.

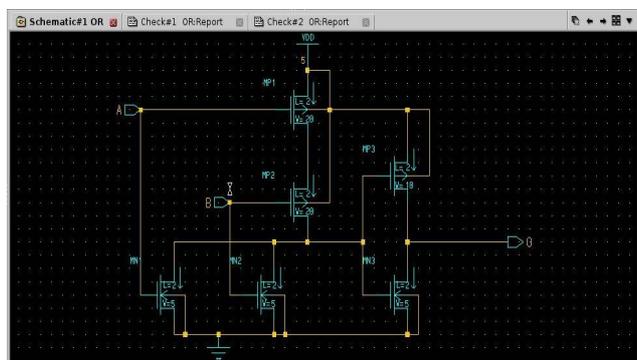


Fig 3.5: OR gate schematic

Thus, after creating the schematic of OR the layout design was achieved, as shown below. The layout was designed in Mentor Graphics Layout editor.

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Vol. 7, Issue 1, January 2018

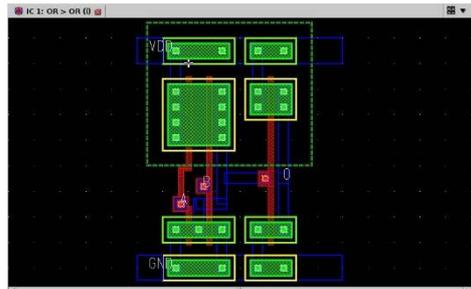


Fig 3.7: OR gate layout

As per the truth-table of OR gate, the waveform output is obtained and is true.

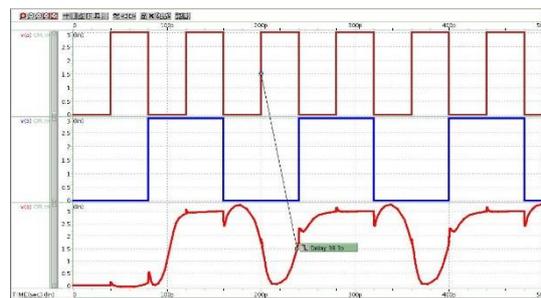


Fig 3.8: OR output waveform obtained in WaveView

The output waveform of the designed OR gate is obtained which is shown above. Here it can be observed that it follows the OR logic, having a delay of 38.8ps.

XOR Gate: One of the two main parts of the project is Full Adder. The output sum of this is calculated by using XOR of the three inputs A, B and Cin.

$$\Rightarrow S_{out} = A \oplus B \oplus C_{in}$$

Using the XOR Schematic, we derived the CMOS layout and the waveform, using wave-view, of this gate as shown in the image below.

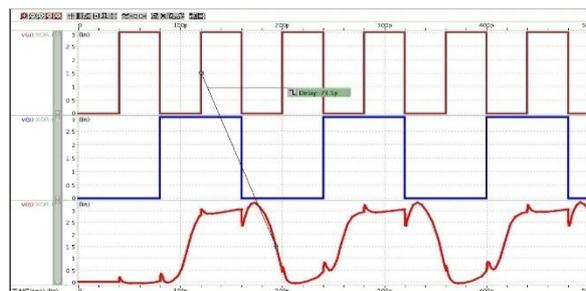


Fig 3.11: XOR output waveform obtained in WaveView

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Vol. 7, Issue 1, January 2018

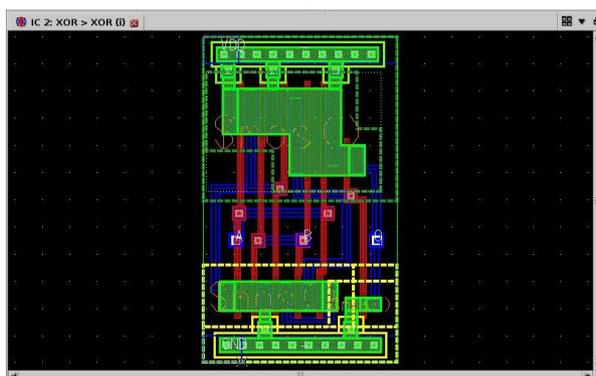


Fig 3.10: XOR gate layout

The output waveform of the designed XOR gate is obtained which is shown above. Here it can be observed that it follows the XOR logic, having a delay of 73.5ps. The Full Adder circuit is used for adding three one-bit binary numbers such as A, B and Cin as inputs. The outputs are two one-bit binary numbers such as SUM and Cout. The full adder is actually a component is cascade of adders which add 8, 16 and 32-bit numbers. The carry output from the full adder is fed to another full adder as input if the full adders are in cascade. The full adder consists of two half adder connected with the OR gate. The circuit diagram of full adder can be represented as follows:

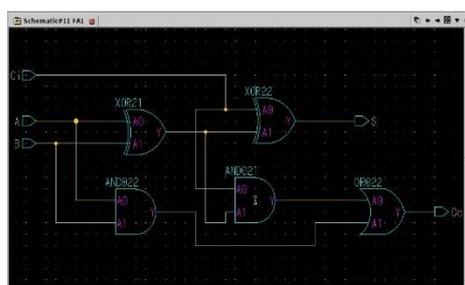


Fig 3.12: Full Adder gate level schematic

After designing the final schematic of full adder, the full custom layout of full adder was completed and checked on the Mentor Graphics Simulator, as shown below:

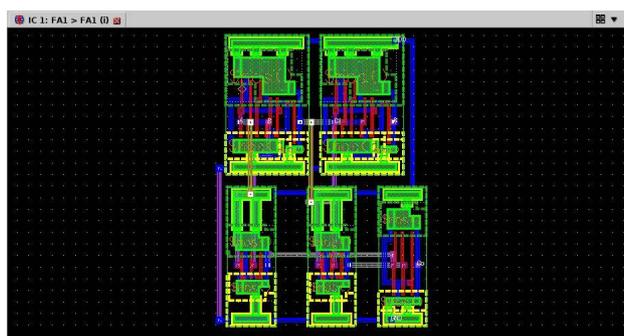


Fig 3.13: Full Adder layout

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Vol. 7, Issue 1, January 2018

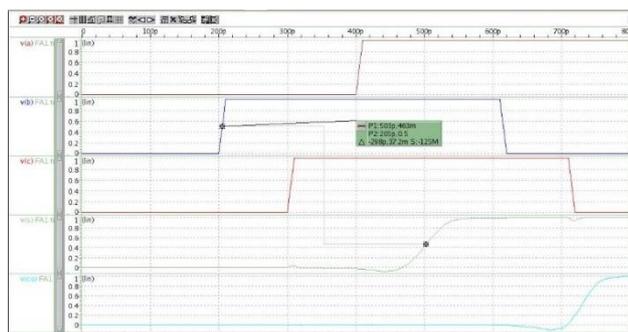


Fig 3.14: Full adder output waveform obtained in WaveView

The output waveform of the designed Full Adder is obtained which is shown above. Here it can be observed that it has a delay of 298ps when one input goes high and output goes high.

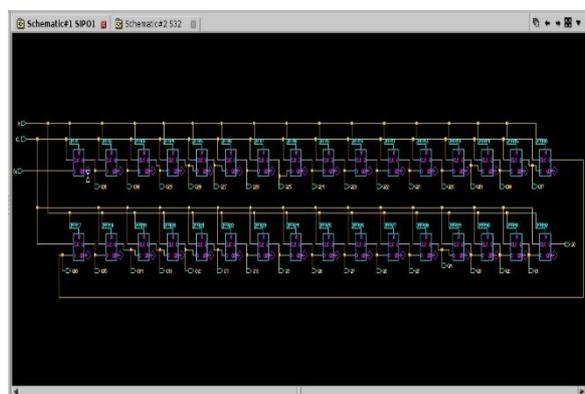


Fig 3.15: 32-Bit SIPO Shift Register schematic

To reduce the pin-out count, we designed the SIPO shift register – one for input A, one for input B of the full adder. Hence, we got in total of 39 pin-out counts. Here, 32 D flip-flops are connected in series to get the final SIPO schematic and layout design.

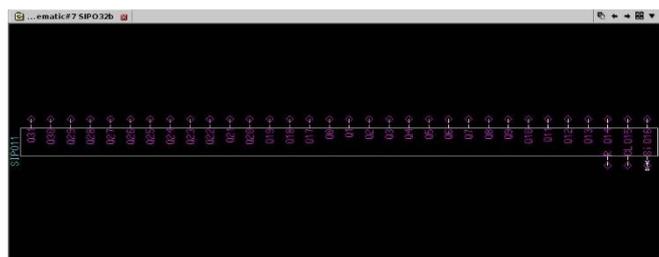


Fig 3.16: SIPO Symbol generated from schematic

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Vol. 7, Issue 1, January 2018

As shown below, the SIPO layout generated in the Mentor Graphics simulator is completed.

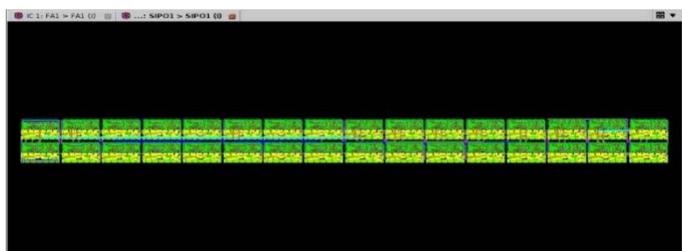


Fig 3.17: SIPO layout

The output waveform after simulation was correctly obtained in WaveView.

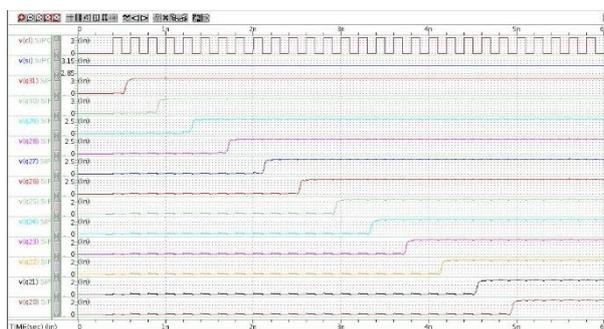


Fig 3.18: SIPO waveform obtained in WaveView

IV. EXPERIMENTAL RESULTS

This is the final schematic obtained for 32-bit Carry Ripple adder by connecting 32 full adders with Cout of one FA into the Cin of the next.

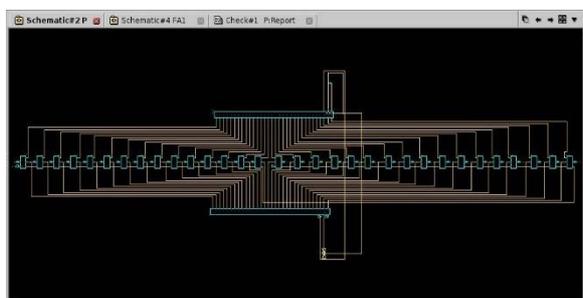


Fig 4.1: 32 bit Carry Ripple Adder schematic

Finally, the full custom layout obtained on Mentor Graphics layout designer was successfully achieved, which is shown below.

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Vol. 7, Issue 1, January 2018

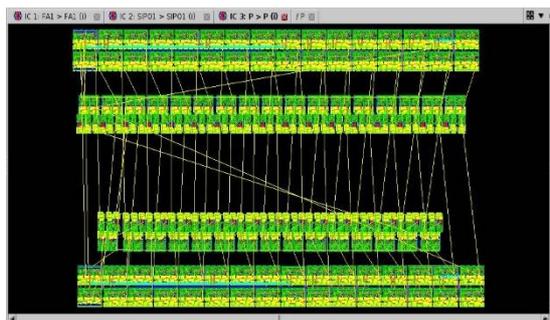


Fig 4.2: 32 bit Carry Ripple Adder layout

V. CONCLUSION

The process of parameter extraction was executed on the final layout for simulation purpose. The results obtained are as follows: LOGIC STYLE: CMOS; NUMBER OF PINS: 39 (VDD, GND, 32 Sout, input A, input B, Cin, CLK, Cout). The full custom layout for 32-Bit Carry-Ripple adder successfully passed the Design Rule Check (DRC) and Layout Versus Schematic (LVS) check.

REFERENCES

- [1] Neil H. Weste, David Money Harris, "CMOS VLSI Design: A Circuit and Systems Perspective", Fourth Edition.
- [2] S. Archana, G. Durga, "Design of low power and high speed ripple carry adder", IEEE trans. International Conference on Communication and Signal Processing, 2014.
- [3] Shams A. M., Darwish T. K., Bayoumi M. A., "Performance analysis of low-power I-bit CMOS full adder cells", IEEE Transactions on VLSI Systems, vol. 10, no. 1, pp. 20-29, 2002.
- [4] Hassoune D., Flandre J. I., Connor J. D., Legat, "ULPFA: a new efficient design of a power-aware full adder", IEEE Transactions on Circuits and Systems-I, vol. 57, no. 8, pp. 2066-2074, 2010.
- [5] Vahid Foroutan, Mohammad Reza Taheri, Keivan Navi, Arash Azizi Mazreah, "Design of two Low-Power full adder cells using GDT structure and hybrid CMOS logic style" Integration the VLSI Journal (Elsevier) (2013).
- [6] Arkady Morgenshtein, Fish A., Israel A. Wagner, "a power-efficient method for digital combinatorial circuits", IEEE Transactions on VLSI Systems, vol. 10, no. 5, pp. 566-581, 2002.
- [7] C. H. Chang, J. Gu, M. Zhang, "A review of 0.18 um full adder performances for tree structure arithmetic circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems vol. 13, no. 6, pp. 686-695, 2005.
- [8] H. T. Bui, Y. Wang, Y. Jiang, "Design and analysis of 10w-power IO-transistor full adders using novel XOR-XNOR gates", IEEE Transactions on Circuits and Systems. Part II: Analog and Digital Signal Processing vol. 49, no. 1, pp. 25-30, 2002.
- [9] Zimmennan R., Fichtner W., "Low-power logic styles: CMOS versus pass-transistor logic", IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1079-1090, 1997.