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## Power Reduction in Pasta Using 32nm Technology

M.Swathi<sup>1</sup>, Ravi Tiwari<sup>2</sup>

M.TECH Student, Department of Electronics and Tele communication Engineering, SSTC College, Bhilai,  
Chhattisgarh, India<sup>1</sup>

Assistant Professor, Department of Electronics and Tele communication Engineering, SSTC College, Bhilai,  
Chhattisgarh, India<sup>2</sup>

**ABSTRACT:** As technology calibration down into the lower nanometer values power, delay becomes essential parameters for the analysis and design of any circuits. The design of a parallel self-timed adder by adopting transmission gate logic style was applied for multi bit binary addition.. Multiplexer is adopted in this design to ignore complications of interconnections. The procedure is parallel to ignore carry chain propagation. In carry-look ahead adder due to carry chain propagation there is a trouble of high fan-in and fan-out. In this PASTA completion detection unit is present for combining all carries to avoid high fan-out. The simulation of the expected design is carried out by using an industry standard toolkit Tanner 16 that testify the practicality and supremacy of the suggested approach over current asynchronous adders. The simulation results of suggested model gain better power consumption and delay and results are verified with suggested technique in 32nm BSIM4 CMOS TECHNOLOGY.

**KEY WORDS:** TG logic, Adders, Asynchronous circuits.

### I. INTRODUCTION

Binary addition is the single most essential operation that a processor executes. Even though there is active interest in clock less circuits, most of the adders have been designed for synchronous circuits. Asynchronous circuits do not estimate any quantization of time. Therefore, they control great prospects for logic design as they are free from any issues of clocked (synchronous) circuits. In precepts, logic flow in asynchronous circuits is guarded by On the other hand, wave pipelining is a approach that can affix pipelined inputs before the outputs are balanced. The suggested circuit operates automatic single-rail pipelining of the carry inputs detached by propagation and immobility delays of the gates in the circuit aisle.

Self timed assign to logic circuits that lean on timing assumptions for the appropriate operation. As initial completion sensing can ignore the need for the worst case bundled delay mechanism of synchronous circuits, self-timed adders have the prospects to run faster unexceptional for dynamic data. The PASTA circuit is executed in tanner 16 tools with transient analysis. As transient analysis is called process behind PASTA.

### II. RELATED WORK

In the architecture of PASTA shown in Fig.1, the parallel self timed adder all along the initial phase, selection line of the multiplexer prefers the first input and executes the half addition. Then next, it shifts to the SEL=1 and selects the feedback path that means sum and carry executes the half addition. Multiple iterations are arising until all carry values are pretended to be zero to the completion detection unit. Completion detection adopts pseudo NMOS logic. In this n-block PMOS transistor performs as a pull-up device. High speed is the asset of pseudo-NMOS logic and low transistor count. If all carry values to the completion detection unit are pretended to zero access completion signal (TERM). Parallel Asynchronous Self Timed Adder (PASTA) is produced by adopting transmission gate based on recursive

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formulation This brief shows up a parallel single-rail self-timed adder. It is hinge on a recursive formulation for executing multi bit binary addition. Thus, the design obtain logarithmic act over irregular operand conditions without any certain speedup circuitry or look-ahead schema. A practical exertion is provided along with a completion detection unit. The attempt is regular and does not have any sensible limitations of high fan outs. A high fan-in gate is enforced though but this is inevitable for asynchronous logic and is operated by connecting the transistors in parallel.

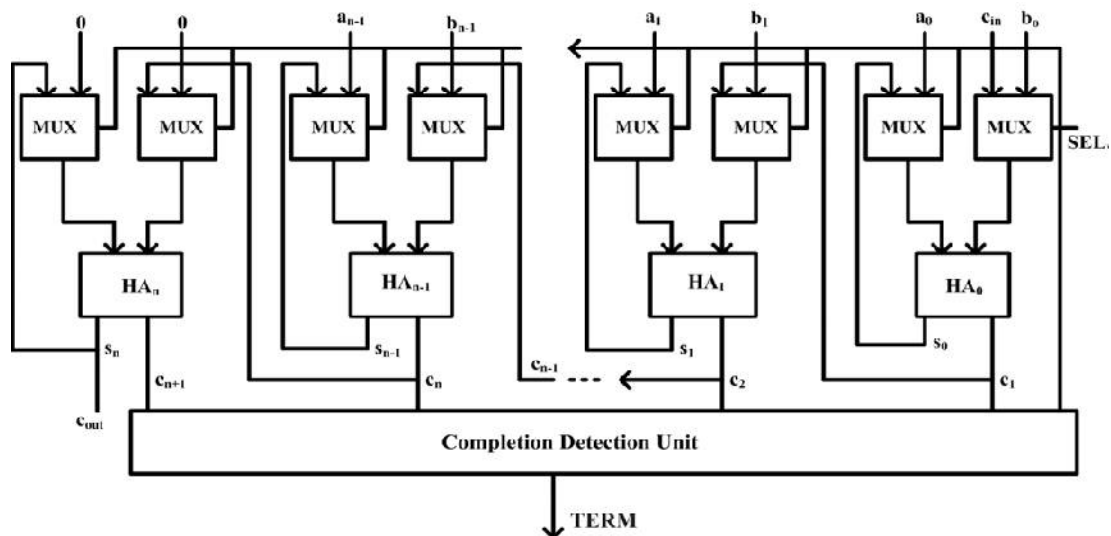


Fig. 1: Block Diagram of PASTA

### State diagram

The state diagrams of parallel self timed adder are shown in below Fig 2. The two states are initial state and iterative state. Each state is represented by  $(C_{i+1}, S_i)$  pair.  $C_{i+1}, S_i$  is the carry-out and sum respectively. Instead of FA, we use HA because (11) state is not present. The  $SEL=1$  is activated in the iterative phase. When  $SEL=1$ , the feedback path is activated. Iterations are performed until all carry values are assumed to be zero. Once all carry values are zero then recursion is completed.

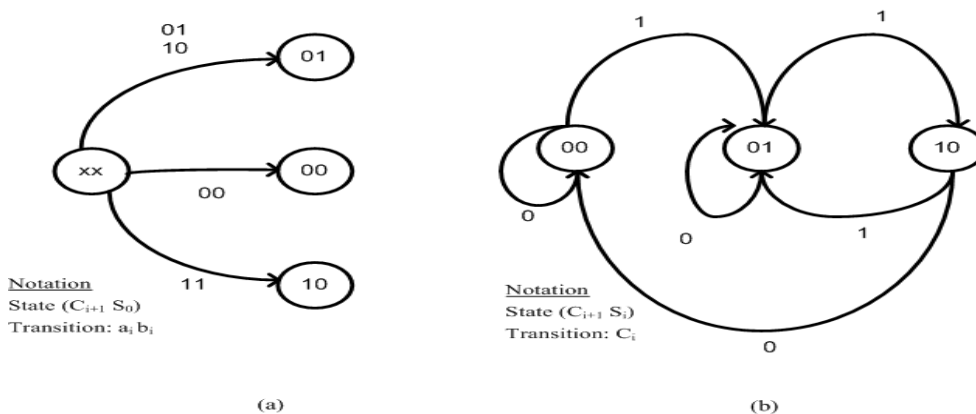


Fig.2: State Diagram of Pasta. (a)Initial Phase (b)Iterative Phase

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Let us assume  $S_i^k$  and  $C_{i+1}^k$  stand for the sum and carry respectively for  $i$ th bit and  $k$ th iteration. The initial Position ( $k=0$ ) for addition is

$$S_i^0 = a_i \oplus b_i \quad (1)$$

$$C_{i+1}^0 = a_i b_i \quad (2)$$

The  $k$ th iteration for the recursion addition is given by

$$S_i^k = S_i^{k-1} \oplus C_{i+1}^{k-1} \quad 0 \leq i < n \quad (3)$$

$$C_{i+1}^k = S_i^{k-1} C_{i+1}^{k-1} \quad 0 \leq i < n \quad (4)$$

Recursion is concluded at  $j$ th iteration when

$$C_n^j + C_n^{j-1} + \dots + C_i^j = 0, 0 \leq j \leq n \quad (5)$$

The recursive formulation of (1)—(5) will produce correct sum for any number of bits and will conclude within a finite time. *Basis:*

If  $C_i^0 = 0$  for  $\forall i, i \in [0, \dots, n]$  then the recursion is stop by (5).

*Induction:* Let that  $C_{i+1}^j$  not equal to 0 for  $i$ th bit and  $j$ th iteration. Let us consider  $l$  be the bit for  $C_{i+1}^j = 1$  then addressed to next bit ( $j + 1$ ) iteration. The  $j$ th iteration of  $l$ th bit state ( $C_{l+1}^j, S_l^j$ ) and ( $l + 1$ ) th bit ( $C_{l+2}^j, S_{l+1}^j$ ) in any of (0, 0), (0, 1), (1, 0) states. If  $C_{i+1}^j = 1$  then  $S_l^j = 0$  from (4),  $C_{i+1}^{j+1} = 0$  for any input between 0 to 1 bits.

Suppose we assume the ( $l + 1$ ) th bit ( $C_{l+2}^j, S_{l+1}^j$ ) for  $j$ th iteration. It also be (0, 0), (0, 1), (1, 0) states. In ( $j + 1$ ) iteration, the (0, 0), (1, 0) states from the  $j$ th iteration following (3) and (4) will produce appropriate result. Thus the recursion is addressed when all carry values are zero.

### III. EXECUTION OF PASTA

The PASTA circuit is executed by designing Multiplexer, Half Adder and Completion Detection Unit. These are designed separately in the latest version of tanner tool i.e. tanner 16. The HA is considered in this operation because in HA (1,1) state is not present there is no requirement of (1,1) state in PASTA. The final circuit is designed in the system. The interconnections in the circuit are less and the area efficiency is also less in this circuit. In PASTA circuit the supply of 0.5 v and 0.4v is given. The circuit is executed and the result obtained is less power consumption and delay compare to previous values. The following is the procedure of PASTA implementation and operated in the system A TG implementation for the multiplexer shown in Fig.3. The schematic of PASTA is shown in Fig.6. In order to activate the high completion signal (TERM), the completion detection circuit is executed. For the completion detection unit Pseudo NMOS design is used to avoid the high fan in issues by connecting all NMOS in parallel and the PMOS transistor is connected to Vdd.

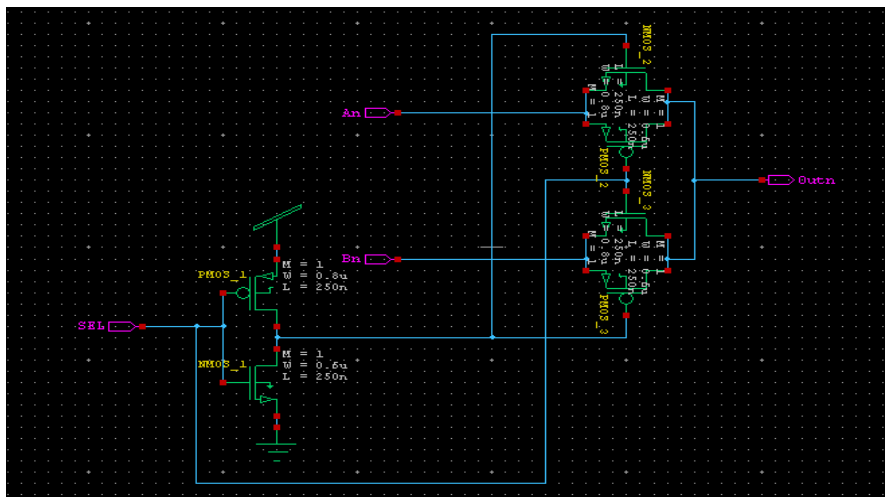


Fig. 3: Schematic of MUX using TG Logic

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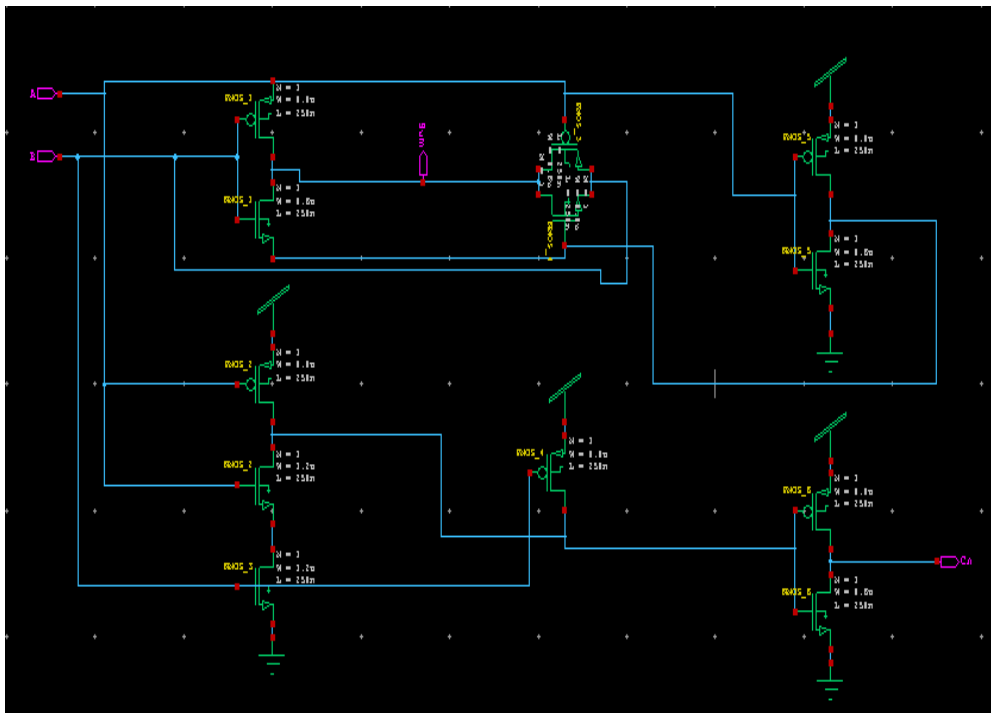


Fig.4: Schematic of HA using TG Logic

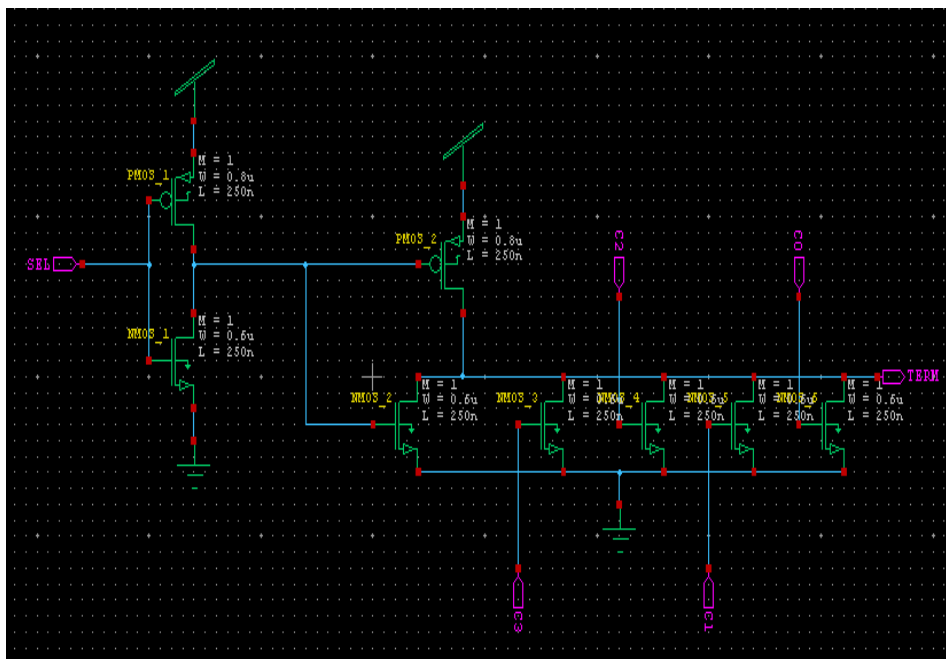


Fig.5: Completion Detection Circuit

## IV. SIMULATION RESULTS

We can understand the superiority of the proposed 4 bit PASTA using TG (Transmission Gate) Logic. 32nm BSIM4 CMOS technology is used. The analysis and execution of PASTA using TG logic is completed the simulation is done in tanner 16.

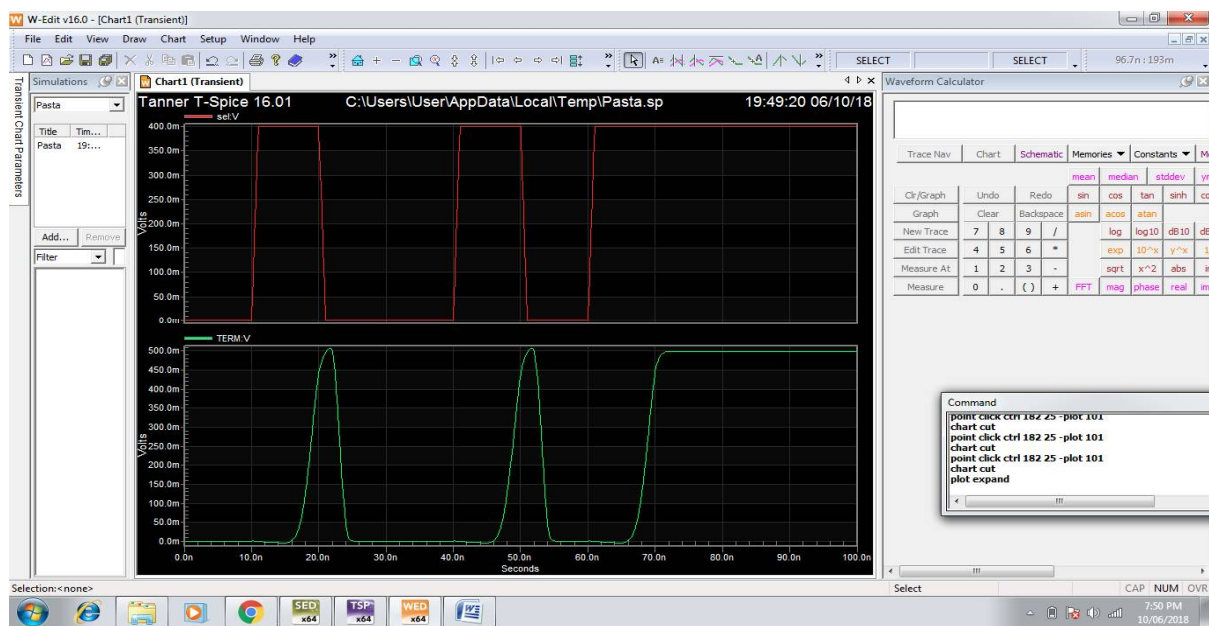


Fig.6: Waveform after Simulation

**Table.1: Power Consumption ( $\mu\text{W}$ ) of Pasta using Gate Diffusion input Technique (GDI) and Transmission gate (TG) technique**

TECHNOLOGY	PASTA using GDI	PASTA using TG
90nm	1.40 $\mu\text{W}$	0.90 $\mu\text{W}$
45nm	0.95 $\mu\text{W}$	0.63 $\mu\text{W}$
32nm	0.50 $\mu\text{W}$	0.149 $\mu\text{W}$

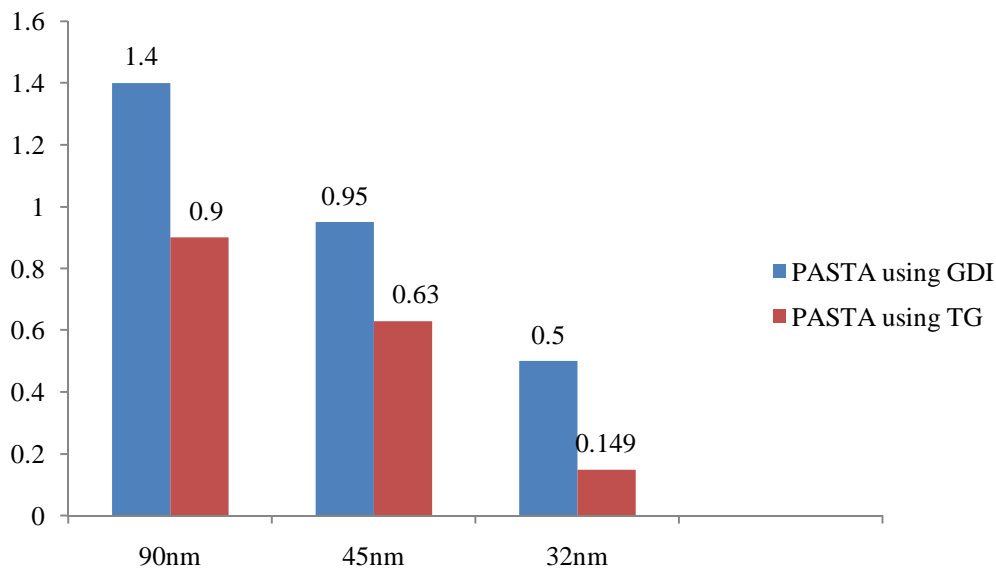
According to the above obtained result the power consumption is greatly reduced by using TG logic, the comparison is shown in below graph so PASTA can be used for low area, high speed and low power applications.

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**Fig.7: Graph of Power Consumption in PASTA**

## V. CONCLUSION

In this paper, the PASTA is executed in new version of tanner i.e. tanner 16 tool. In PASTA (Parallel asynchronous self-timed adder) using TG power consumption is compared with PASTA using GDI Technique. This 4bit PASTA using TG technique is more efficient in terms of power consumption. The advantages of PASTA are verified by using simulation results.

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