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# Design of Ripple Borrow Subtractor with Full Subtractor Using Hybrid Logic to Reduce the Power Dissipation and Area

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**ABSTRACT:** The full subtractor design using hybrid logic and MTCMOS technique is proposed in this paper. Subtractor is one of the arithmetic circuit and it plays a vital role in designing of VLSI circuit. The combinational logic circuit is used in various field like DSP, low power VLSI design and also in microprocessor. Power dissipation is the main issue in vlsi design. The objective of this project is to reduce the power dissipation. One of the method to reduce the power dissipation is scaling. It causes the sub threshold leakage current which is the predominant component in the total average power dissipation. In this paper we proposed a modified approach to decrease the power dissipation using hybrid logic technique in full subtractor design. This design is used as basic cells for designing ripple borrow subtractor. The simulation is performed at 1.8v using tanner tool in 180nm technology.

**KEYWORDS:** Tanner, Hybrid logic, Power dissipation, Area.

### I. INTRODUCTION

In the designer view, the most required feature for modern electronic system is energy efficient required for high performance and portability. The ever increasing trends demand the low power, less area that can be achieved by incrementing the required function. At the circuit design level, considerable method for power saving is by choosing proper logic style. And the other side to increase the throughput required in high performance devices is accomplished by applying scaling technology to the electronic devices. Scaling of supply voltage reduces the threshold voltage but increases the sub threshold leakage current. Sub threshold current is the current flowing from drain to source when the transistor is off. The sub threshold leakage current mainly depends on supply voltage, size of the device, temperature

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and other parameters. The working principle behind the sub threshold leakage current is the mos device operated in gate voltage rather than threshold voltage resulting in diffusion current. The diffusion current is mainly due to the minority charge carriers. In this technique each NMOS and PMOS transistors in the logic gates is split into two transistors. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in drain to source voltage in the opposite NMOS transistor. This reduces the power dissipation in logic circuits. This technique is implemented to basic gates such as AND, XOR etc, Combinational Circuits such as full subtractor, fulladder, sequential circuits.

Arithmetic circuits are the heart of vlsi circuit. Subtractor is one among them. We implement the design and performance of full subtractor based on the multiplexing of the Boolean function AND/OR and XOR/XNOR, to obtain the difference and borrow outputs respectively. The smallest unit in the combinational circuit is known as subtractor which is used in the arithmetic calculation in processor and also used in calculating addresses. It is also used in stack pointer to perform push and pop logical operation. The resultant proposed full subtractor is more efficient than conventional full subtractor in terms of power consumption and area. In this paper the full subtractor is designed with modified structure using dpl(double pass transistor logic)with ptl (pass transistor logic) .

## II. RELATED WORK

Many methods have been proposed to reduce the leakage current in the combinational circuits. MTCMOS technique is used in the conventional full subtractor to reduce the leakage current and power was proposed by Milind Gautam Shyam Akashe [1]. The AVL incorporated half subtractor to reduce the power dissipation is presented by Devendra kumar Gautam & Sinha [2]. The design of low power full adder with powerless/groundless logic style was proposed by Mariano Aguirre- Hernandez and Monico Linares-Aranda. Reto Zimmermann and Wolfgang Fichtner [4] demonstrated the advantages of CMOS with respect to the parameters like speed, area, power dissipation and power delay products. The design of an energy efficient high speed and low power full subtractor using Gate Diffusing Input (GDI) was presented by Krishnendu Dhar and Aanam Chatterjee [5]. The author has showed the reduction in average power consumption, delay time as well as power delay product using GDI (Gate Diffusion Input) technique. The reduction in leakage current and ground bounce noise in the full subtractor design using MTCMOS technique was proposed in [6]. The autho introduced tri mode technique to get reduction in the peak of ground bounce noise and overall power mode transition noise.

## III. CONVENTIONAL FULL SUBTRACTOR

A full subtractor circuit is one which implements the subtraction between three bits. First bit is minuend, next bit is subtrahend and the third bit is borrowed in input. And the output bits are difference and borrow. The standard full subtractor consists of half two subtractor and one OR gate.

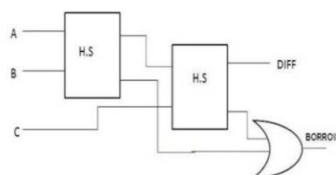


Fig.1: Conventional Full Subtractor.

It requires two XOR gate, two AND gate, two NOT gate and one OR gate and the output of full subtractor depends on the intermediate signal.

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TABLE I: FUNCTIONAL TABLE

A	B	C	DIFFERENCE	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The propagation delay of the intermediate signal affect the overall time delay of the circuit. So in order to increase the performance of full subtractor the modified structure is developed using Double Pass transistor Logic Pass Transistor Logic style. The conventional full subtractor is shown in figure 1. And the functional table of full subtractor is also shown in above.

### IV. MODIFIED STRUCTURE WITH DPL AND PTL STYLE

By observing the functional table in Table I, It is observed that the Difference output is equal to (A XOR B) when C = 0 and (A XNOR B) when C =1 similarly the Borrow output is equal to B when (A XOR B) = 1 and C when (A XNOR B) =1. So one taking “C” as a selection signal and another multiplexer is used to obtain the borrow output by taking (A XOR B) as a selection input. By using this concept the modified full subtractor is proposed using PTL as depicted in figure 2.

$$\text{Difference} = (A \text{ XOR } B) + (A \text{ XNOR } B) C \dots\dots\dots (1)$$

$$\text{Borrow} = (A \text{ XOR } B) B + (A \text{ XNOR } B) C \dots\dots\dots (2)$$

The full subtractor designed with Double Pass transistorLogic (DPL) is shown in figure 3. It consists of two transistors i.e. nMOS and pMOS in parallel. According to pass transistor logic, the nMOS transistor transfers poor logic1 and the pMOS transistor transfers poor logic 0. The main advantages of Double Pass Transistor logic is full swing output due to both pMOS and nMOS transistors. No level restorer is required and the circuit robustness is high.

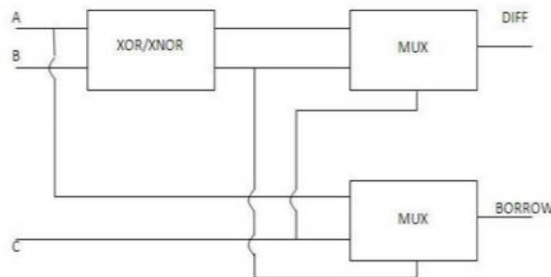


Fig.2: Full subtractor using ptl

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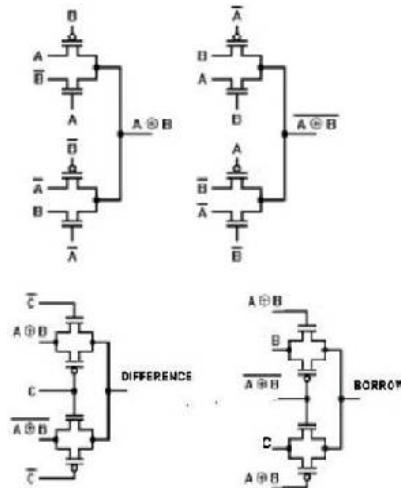


Fig.3: Modified Full Subtractor using DPL logic.

The basic approach of this proposed full adder is to have a fast and low power adder circuit. Here we have used two design logic i.e. GDI and PTL combining both we are going to analyze the result of the circuit. It basically consists of three modules, one is made by GDI second is by PTL and other is inverter by CMOS . It is shown in figure 4.

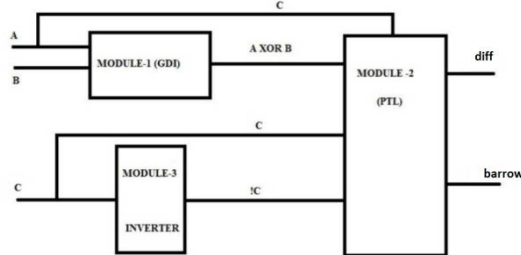


Fig.4: proposed Full subtractor using hybrid gdi and dpl

## V.RIPPLE BORROW SUBTRACTOR

Considering the full circuit as bench mark circuit for designing the ripple borrow subtractor. Therefore to implement a 4- bit subtractor we can divide the operation in each column as a 1-bit subtraction operation, Full subtractor works similar to the subtraction performed by hand, as shown in Fig 5. It has 3 inputs and 2 outputs respectively and B are the binary inputs we intend to subtract, D is the resulting binary output. Subtraction starts from right most digit,in this case if  $B > A$ ,we require the borrow from left digit of B, thus Bout indicating the borrow operation. In case when latter columns requires a borrow operation, Cin is set to 1.

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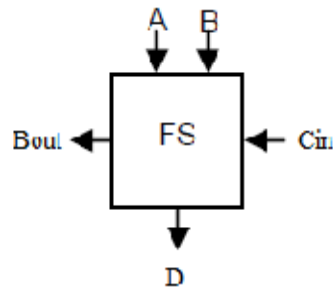


Fig 5: Full subtractor block diagram.

Consider subtracting two 4-bit binary numbers, 1010 – 0111, as shown in example. We first start by considering the right-most column (first column). A is less than B (0 < 1), thus we must borrow from the second column resulting in 10 – 1 = 1 (in base 10, two minus one equals one). In the second column, A = 0 because of the aforementioned borrow. Thus we must borrow from the third column, which intern must borrow from the fourth column. Again, once we have borrowed, the second column results in 10 – 1 = 1. In the third column, A = 01, resulting from the borrow operation generated by the second column. The third column results in 01 – 1 = 0. Lastly in the fourth column, A = 0 resulting in 0 – 0 = 0.

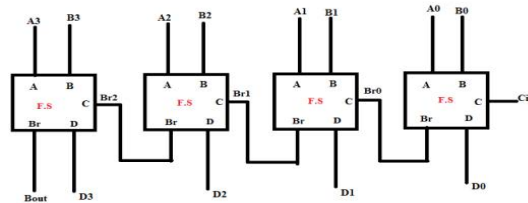


Fig.6: 4-bit ripple borrow subtractor.

**Example:**

<p>First Column</p> $\begin{array}{r} 1010 \\ -0111 \\ \hline 1 \end{array}$	<p>Second Column</p> $\begin{array}{r} 1010 \\ -0111 \\ \hline 11 \end{array}$
<p>Third Column</p> $\begin{array}{r} 1010 \\ -0111 \\ \hline 011 \end{array}$	<p>Fourth Column</p> $\begin{array}{r} 1010 \\ -0111 \\ \hline 0011 \end{array}$

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## VI. RESULTS AND DISCUSSION

The given schematics were designed in TSMC 0.18  $\mu\text{m}$  CMOS technology using TANNER tool.

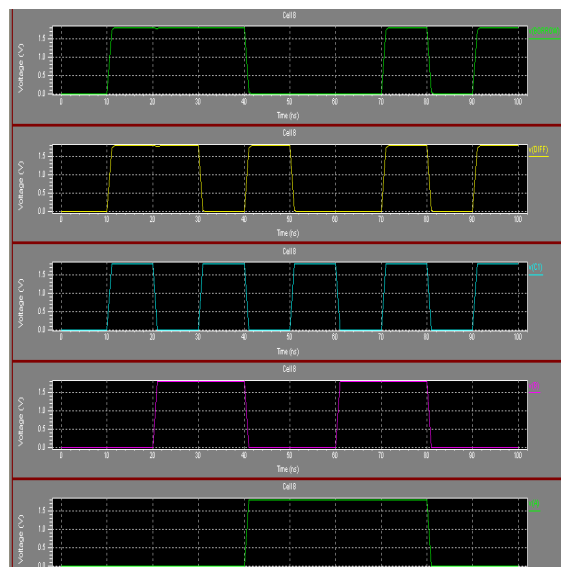


Fig.7:Full Subtractor waveform.

Figure shows the simulation output waveform of the modified full subtractor. The waveform show the difference and borrow output of the modified full subtractor for the various combinations of the input.

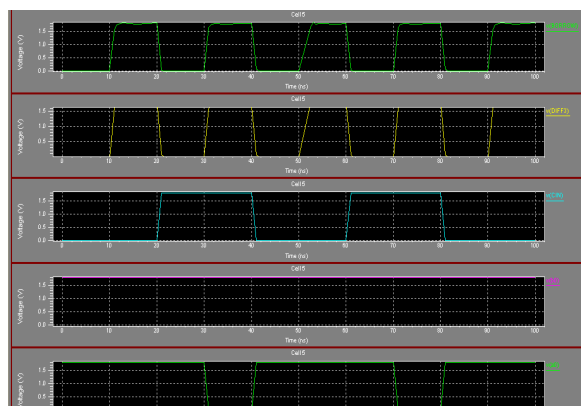


Fig.8:Ripple Borrow Subtractor waveform.

The above figure shows the output waveform of Rippele Borrow Subtractor. It contains three inputs A, B, CIN and two outputs DIFF and BORROW.

Table II shows the performance comparison of proposed full subtractor with conventional full subtractor. The full subtractor was operated with 1.8 V supply voltage. The proposed full subtractor requires only 45% of transistor area of

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the conventional full subtractor. This factor can also be considered for presenting very less leakage current and reduced power consumption.

Parameter	Conventional full subtractor	Proposed full subtractor
Average power consumption	$2.203787e^{-005}$	$8.6063e^{-006}$
Number of transistor	32	14

TABLE II: COMPARISON OF PROPOSED WORK WITH CONVENTIONAL FULL SUBTRACTOR

## VII. CONCLUSION

The modified full subtractor design was introduced using hybrid DPL-PTL logic to get the advantages of both. The circuits were implemented using 0.18 $\mu$ m CMOS technology and were simulated. The simulation results showed that the proposed circuit reduces the power consumption and area requirement. The area requirement of the proposed full subtractor is 40% of the conventional full subtractor by maintaining proper functionality. Further, for higher bit operations, the modified full subtractor can be cascaded or connected in parallel to enhance the performance. This full subtractor is applied to ripple borrow subtractor and seen the results.

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