

Routing Scheme for Network On-Chip (NOC) based Fuzzy logic

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ABSTRACT: Network on chip is an emerging technology which provides data reliability and high speed with less power consumption. With the technological advancements a large number of devices can be integrated into a single chip. So the communication between these devices becomes vital. The network on chip (NoC) router is used for such communication. This project presents the simulation and synthesis of a fuzzy logic-based adaptive routing scheme for Network-on-Chip (NoC) using Xilinx ISE software. The routing scheme takes into account the dynamic traffic load and power consumption on neighboring router links to select the output port of an incoming flit. Specifically, fuzzy logic control is used to build a simple, generic, and efficient nonlinear control law that dynamically calculates the input link cost. Basing the link cost on traffic load and power consumption and not on empty buffer slots, makes the proposed algorithm applicable to both buffered and bufferless NoCs. Furthermore, since the fuzzy control logic is not in the router critical path, it imposes no additional latency.

KEYWORDS: Fuzzy logic, Network on Chip (NoC), Router, Verilog, Xilinx ISE 14.4.

I. INTRODUCTION

The vision for the development of a totally pervasive computing environment from smart home and smart cities to, ultimately, a smart planet requires the continuation of Moore's law through more Moore, more-than-Moore and beyond Moore technologies. Cumulative exponentially increasing integration already enables the manufacturing of many-core computing architectures comprising hundreds of heterogeneous IP cores. Efficient utilization of these resources in terms of performance, power consumption and thermal distribution in order to accommodate increasingly demanding applications is a complex design problem encompassing all design aspects. Furthermore, dependability of such complex systems in the face of challenges such as the increasing unreliability of state-of-the-art nanometer VLSI processes and their use in, among others, IoT applications such as smart cities, e-health etc. is essential. Such efficient and reliable utilization requires, in turn, efficient and reliable communication infrastructure connecting the processing and memory cores. Network-on-Chip (NoC), after years of academic and industrial research, has been established as an architecture that is able to accommodate such a high number of cores, satisfying the needs for efficient communication and bandwidth, due to its scalability. For these reasons, NoCs have become the dominant communication paradigm for Systems-on-Chip (MP SoCs), and are supported from the industry (A Ethereal NoC from Philips, STNoC from STMicroelectronics and an 256-core NoC from Intel), and are also available as silicon-proven IP cores already present in both high-performance and IoT solutions.

NoC design requires the careful examination of a number of parameters that impact the network performance in terms of performance, area, and power consumption. Such a critical design parameter is the routing technique for on-chip communications that determines the path selected by a packet to reach its destination. The effectiveness of the routing technique directly influences the network latency, while indirectly affecting power consumption and thermal distribution, since it determines the switching of wires and flit storing in buffers in the lower layers.

An often desirable feature of a routing algorithm is being minimal or shortest-path, meaning to select the path with the least number of hops between source and destination. However, this does not necessarily guarantee

minimum latency, since under heavily congested network conditions flits may remain stored in router buffers for a long time before they are allowed to progress, while another path may be available. Therefore, increasingly important is adaptivity, meaning the algorithm can select among multiple paths to destination, depending on network conditions such as congestion and transient or permanent faults.

The insight that buffers are the greatest component of power consumption in NoCs, led to approaches that try to eliminate buffers in routers altogether. The fundamental idea behind bufferless routing is to route a packet (or a flit) to an output port of router, regardless of whether or not that output port results in a lower distance to the destination of the packet. Since there is no control about to which port the packet should be forwarded to, it is possible for packets to be deflected or “misrouted” when the output port that reduces the distance to the destination node is not available. In order to ensure freedom from livelock due to perpetual deflections, the decisions about packet switching in bufferlessNoC architectures are based on prioritizing packets by some metric.

From the above, it can be seen that routing algorithm design and implementation is not a straightforward task. First of all, the efficiency of the algorithm must be proven through extensive simulation for a number of design metrics such as latency and power consumption. Then, the hardware overheads required for the implementation of the algorithm must be taken into account by designing and implementing a router. The ideal case of a fully adaptive, topology-agnostic and fault-tolerant routing algorithm with excellent performance and minimal overhead is not feasible and various trade-offs between the above metrics must be examined.

In this paper we present the hardware design of an adaptive routing scheme that can support both buffered and bufferlessNoC architectures. The output port assignment and therefore the routing path is determined by a fuzzy logic controller, taking into account the dynamic traffic and power consumption in the links between each router and its neighbors. The proposed routing scheme that measures incoming traffic in the links and not the buffer slots, was originally proposed by the authors for bufferlessNoCs and its effectiveness was proven through simulation in . In this paper we extend the proposed routing scheme to buffered NoCs and we thoroughly examine its hardware cost through both ASIC and FPGA implementations. Experimental results demonstrate low overhead in terms of area (cost), performance and power consumption in both ASIC and FPGA technologies.

The key features of the proposed routing algorithm are the following:

- Full adaptivity: Any possible routing path can be chosen, depending on network congestion and power consumption.
- Congestion awareness: Congestion metrics obtained by monitoring the incoming traffic load and obtaining similar metrics from neighboring routers when deciding the routing path.
- Power consumption awareness: Link dynamic power consumption is considered, by measuring the input link switching activity.
- Support for both buffered and bufferless router architectures: By using the incoming traffic requests instead of the empty buffer slots for measuring congestion, the proposed algorithm can be used by both buffered and bufferless routers.
- No additional traffic: By introducing additional dedicated links to send the link costs to the neighbors there is no need for additional control packets.
- No additional latency: With the link cost calculation and transmission logic not being in the packet receive-transmit path, no packet latency overhead is introduced.

Neighbor-to-neighbor communication: No centralized global routing technique, which is difficult to scale.

II. PROPOSED FUZZY LOGIC ROUTER

The proposed routing scheme, aimed at, but not limited to, bufferlessNoC, is based on fuzzy logic control techniques. Its principal goal is to enhance the communication efficiency, in terms of throughput and latency. Due to the highly dynamic network conditions, the proposed scheme needs to operate in a decentralized way, i.e.

locally at each router. Since the proposed router obtains congestion and power consumption information, it would be possible to be used in combination with task mapping algorithms, which minimize latency and power consumption. In any case, the two approaches are orthogonal and the proposed router operates independently of task mapping.

III. FUZZY LOGIC ROUTING ALGORITHM

An intelligent controller, based on fuzzy logic, was originally proposed by the authors for bufferlessNoCs. In this paper we extend the proposed routing scheme to buffered NoCs and we thoroughly examine both its hardware cost through both ASIC and FPGA implementations, and also its efficiency through simulative evaluation.

We used fuzzy logic control principles to design a simple, effective and efficient nonlinear control law, in order to offer inherent robustness with effective control of the system. Due to the highly dynamic network environment, the proposed control mechanism needs to operate in a decentralized way, i.e. locally at each router. Using linguistic rules that describe the behavior of the environment in widely differing operating conditions, the proposed fuzzy logic controller dynamically calculates the cost of each input link of the router based on two network state inputs: the switching activity (taken as approximation for power consumption) and the traffic load, both taken at the end of each sampling period. The philosophy behind the knowledge base of the proposed scheme is that of being aggressive when the switching activity is getting bigger and the traffic load is high, but on the other hand being able to smoothly respond in the case of adequate conditions in the environment. Due to computational simplicity, we select trapezoidal and triangular shaped membership functions in the proposed control scheme to describe the linguistic values of the fuzzy input and output variables. The amount of overlapping between the membership functions areas is chosen so as to have at most two membership functions overlapping, thus we will never have more than four rules activated at a given time. This offers computational simplicity on the implementation of the proposed scheme, a design objective. Further, there is no need for a fuzzy inference engine to be built in each NoC router. After the linguistic rules have been found and the linguistic values are tuned by a simulator, the control surface is known and can be stored as lookup table (size of $n * n$) for selected sampling points. In order to keep the size of the memory required in each router reasonable, n is equal to 12, therefore the lookup table has 144 possible combinations of values that had firstly transformed into integer values.

The first metric used in the proposed controller is dynamic power on the links, which is estimated by counting the switching activity on the data_in input of each port. The second metric is traffic load, obtained simply by counting how many times the valid_in signal is asserted, signifying an incoming flit, over the sampling period.

A. Switching Activity

Power consumption in the links can be divided into the dynamic and static power consumption. Dynamic power is the most significant power component. Dynamic power consumption. We use the switching activity as a proxy for dynamic power consumption in our methodology, since the other factors are technology and design parameters that cannot be directly influenced by the routing decision.

Specifying fuzzy sets for switching activity is not a straightforward task. To the best of the authors' knowledge there are no published studies of actual switching activity measurements in NoC. In the case of a different average switching activity value, this can be determined by profiling the application and simply adjust the ranges for low, medium and high switching activity. The discuss switching activity in detail. From VLSI design, it is known that for random signals propagating in logic gates, the switching activity is approximately 10%. However, switching activity for NoC flits is likely considerably higher.

Since most packets carry address and data between memory and processing cores, the payload is essentially address and data bus transactions. Switching activity for address buses has been investigated, among others. The authors report switching activities of about 25% for 32 bit internal buses for both data and control intensive application benchmarks.

Regarding correlated data in a shared bus the switching activity is also similar or a dedicated bus and significantly higher for a multiplexed bus. Taking into account the head and tail portions of a packet that contain

address and control fields, the average switching activity may be even higher. In any case, it is likely to be application as well as dependent on the number of virtual channels that share the physical channel. A full exploration of switching activity for NoC is outside the scope of this paper, however, obtaining a fairly accurate estimation of expected switching activity for a given application domain through profiling applications is advisable for a NoC tailored for a specific application domain.

B. Routing Decision

The proposed controller, as described, dynamically calculates the cost of the input links of each router, based on network conditions. Then, each input link cost status is transmitted to the neighboring routers, in a distributed manner. In this way, while monitoring incoming traffic, each router is aware of output congestion, by receiving this information from its neighbors. This information is used to update the corresponding routing table at each router with the least-cost path to the nearby¹ destinations (i.e., the least-cost path towards all nearby destinations is constructed in an iterative manner). This technique is based on the Distance Vector algorithm developed in computer networks.

A major advantage of using such technique is the neighbour-to-neighbour communication, rather than having a centralized, global technique where all routers need to exchange routing information to all routers belonging to the same network. Also, we have modified the generalized Distance Vector algorithm, so that each NoC router is able to calculate the least-cost path to the nearby destinations, and not to all possible destinations. In the NoC framework this is not scalable, since it will create a large overhead both on the router hardware and on the network. Thus, we have taken a simpler approach, as discussed above, to create a simple but effective technique, based on the insight that traffic tends to be more localized in NoCs, in fact traffic between cores is taken into account for core placement.

IV. FUZZY LOGIC BASED ROUTER HARDWARE DESIGN

The NoC architecture considered is a typical mesh topology. The proposed fuzzy logic based router (FLR) design. It is a 5-port crossbar router. More specifically, four router ports are connected to four neighboring routers, one in each direction, while the fifth is connected to the host IP (processing element, memory, etc). The proposed FLR is based on a baseline router design, which can be either buffered or bufferless. In either case, however, there are three fundamental differences. Firstly, the output port allocation logic is different, in order to implement the proposed routing scheme. Secondly, there is added logic in the data input lines in order to obtain the metrics required for the proposed scheme, and thirdly there are additional lines for transmitting and receiving the status of and to the neighboring

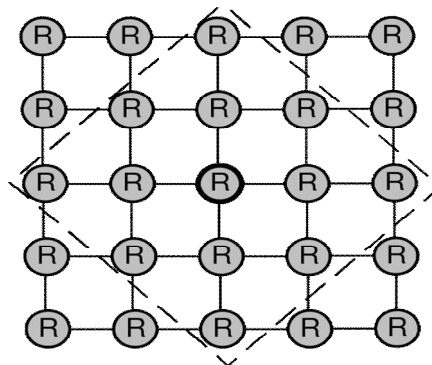


Figure 1.1. Mesh topology and link cost subnet for central node

routers respectively. The network is divided into overlapping subnets, each centered around each router. The router knows the cost for transmitting to any router in the subnet.

Traffic is measured by polling the data_valid_in signal and incrementing a counter, while switching activity is measured by an edge detection circuit on each data_in line which is asserted when there is a switch in the corresponding data_in signal, followed by a circuit that counts the number of logic ones (and therefore the number of switching events) in the vector created by the edge detection lines. Finally, an accumulator counts the total number of bit switches in the sampling period. The traffic and switching activity metrics are the inputs to the link cost lookup table that gives the link cost value that is transmitted to the neighbouring routers. The above logic is not in the flit path from input to output port, and therefore, does not impose any additional latency

V. SIMULATIVE PERFORMANCE EVALUATION

Wormsim simulator is used, which is a high-level NoC simulator that includes a power model (ebit) and also uses the ORION power mode. We consider a 4x4 mesh network architecture

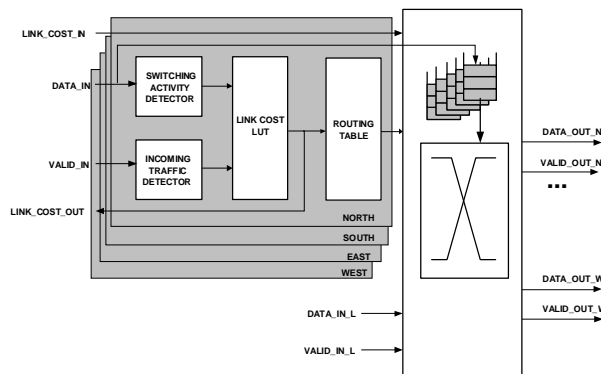


Figure 1 2. Buffered FLR Router Block Diagram

Switching activity is simulated by adding to each flit an activity factor variable that is between 0 and 1 with a mean of 0.3. This is normalized to be in the range [0, 10] with a mean of 3 (assuming a 30% average switching activity) and multiplied by the value given by the Wormsim power model in order to obtain statistically the same value.

VI. RESULT ANALYSIS

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A. SYNTHESIS IS DONE IN XILINX ISE 14.4

TOOL

Family	Spartan3e
Part	xc3s500e
Package	fg320
Temp Grade	Commercial
Process	Typical
Speed Grade	-4
Characterization	PRODUCTION, v1.2.0 6-23-09

B. POWER ANALYSIS

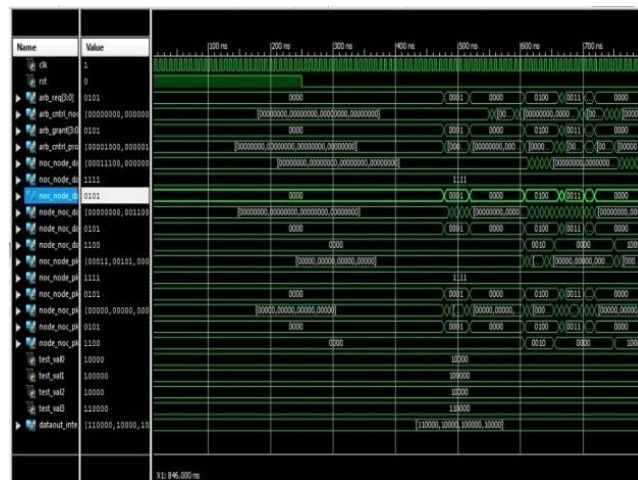
Table 1 DEVICE	
Family	Spartan6
Part	Xc6slx25
Package	Csg324
Temp Grade	C-Grade
Process	Typical
Speed Grade	-3
Characterization	Production v1.3.2011-05-04

Table 2 On-Chip Power Summary				
On-Chip	Power (W)	used	Available	Utilization (%)
Clocks	0.001	1	----	----
Logic	0.000	6819	15032	45
Signals	0.000	7856	-----	----
Ios	0.000	190	226	84
Leakage	0.029			
Total	0.029			

Table 3 Power Supply Currents				
Supply summary		Total current	Dynamic current	Quiescent current
Source	Voltage			
Vccint	1.200	0.012	0.001	0.011
Vccaux	2.500	0.004	0.000	0.004
Vcco25	2.500	0.002	0.000	0.002

Table 4 Power Supply Summary			
Supply Power(W)	Total	Dynamic	Quiescent
	0.029	0.029	0.029

VII. SIMULATION RESULTS



VIII. CONCLUSION

The proposed design of Fuzzy logic based routing scheme for Network On-Chip is simulated and synthesized in Xilinx ISE 14.4 software and the source code is written in Verilog. This proposed design has less delay, less power. This proposed Fuzzy logic based routing scheme router has delay 60 μ s and power 100mW. The delay and power is minimized by using Fuzzy logic.

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