

# Fault Tolerance Techniques for Combinational Circuits

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**ABSTRACT:** Increasing in soft error rates, the multiple faults is needed to be considered while modeling circuit sensitivity and evaluating fault tolerance techniques. This paper proposed a design of combinational circuits for soft error tolerance with minimal area overhead. This is based on analyzing random pattern testability of faults in a design and protecting sensitive transistors, whose probability of soft error is relatively high. Transistors are protected by duplicating and sizing a subset of transistors for the protection of sensitive transistors. The proposed method compares the power and output accuracy using Quad technique and STR (Selective Transistor Redundancy) algorithm.

**KEYWORDS:** STR algorithm, Soft Error, Quad algorithm, Triple Modular Redundancy (TMR), Combinational Circuits, Tanner Tools.

## I. INTRODUCTION

Soft errors are transient errors that cause incorrect operation of a digital circuit. To reduce the error algorithms are used. In this paper, STR and quad algorithms are used to compare the power analysis. Shrinking of device size leads to soft error increase. Fault tolerance techniques cannot be designed with 100% accuracy without increasing design cost. The TMR is the most popular SET mitigation. The SET have a major impact on circuit operation, and they should be treated properly. Triple modular redundancy is one of the possible fault tolerance technique that can be applied to a each logic element is triplicated.

## II. RELATED WORK

Kartik Mohanram, *et al* [1] presents a new methodology for designing logic circuits with partial error masking. This paper targeting the error masking capability towards the nodes with the highest soft error susceptibility to achieve cost-effective tradeoffs. Two reduction heuristics, cluster sharing reduction and dominant value reduction, are used to reduce the soft error failure rate significantly with a fraction of the overhead required for conventional TMR. Drew C. Ness, *et al* [2] states that the application of triple modular redundancy (TMR) to a non-branching (no fan-out) circuit with permanent faults. The need for a model that captures logical masking. This is provided by modifying a soft error rate (SER) estimation algorithm to handle multiple faults and gate input interdependence. It is conclude that the simple non-branching model can predict a trade-off threshold for when TMR can benefit a circuit. Using CMOS transistors is quickly becoming a critical design challenge as sensitivities to soft errors are increasing. Warin Sootkaneung, *et al* [3] presents the studies thorough the effect of device size on circuit soft error rate and identifies methods to reduce soft error rate in combinational circuits. There are three novel methods that upsize only selected gates or transistor networks. In order to obtain the most appropriate technique for soft error rate reduction in small technology node circuits, and compare the results for several upsizing techniques including all gates, selected gates and transistor networks. The soft error rate about 20% with a very small area overhead of 2% for benchmark circuits using our technique. John Teifel, *et al* [4] presents the Dual-modular-redundancy (DMR) architectures use duplication of transistors and self-voting asynchronous circuits to mitigate single event transients (SETs). The area and performance of DMR circuitry is evaluated against conventional triple-modular-redundancy (TMR) logic. Benchmark ASIC

circuits designed with DMR logic show a 10–24% area improvement for flip-flop designs, and a 33% improvement for latch designs.

### III. SOFTWARE USED

Tanner 13.0 is used for the proposed method. Tanner tools is a Spice Computer Analysis programmed for Analogue Integrated Circuits. Tanner tool consists of the following Engine Machines:

- S-EDIT(Schematic Edit)
- T-EDIT(Simulation Edit)
- W-EDIT(Waveform Edit)
- L-EDIT(Layout Edit)

Using these engine tools, spice program provide facility to the use to design & simulate new ideas in Analogue Integrated Circuits before going to the time consuming & costly process of chip fabrication.

#### Schematic edit tools (S-EDIT)

S-Edit is hierarchy of files, modules & pages. It introduces symbol model & schematic modes.

#### Circuit simulator (T-SPICE)

T-Spice Pro's waveform probing features integrats S-Edit ,T-spice & W-Edit to allow individual points in a circuit to be specified and analyzed. The heart of T-spice operation is the input file.

#### Waveform edit (W-EDIT)

The ability to visualize the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding & improving these circuits. W-Edit is a waveform viewer that provides ease of use, power & speed in a flexible environment designed for graphical data representation.

#### Layout (L-EDIT)

It is a tool that represents the masks that are used to fabricate an integrated circuit. It describes a layout design in terms of files, cells & mask primitives. On the layout levels, the component parameters are totally different from schematic level.

### IV. FLOW DIAGRAM

The flow diagram of the proposed technique is shown in Fig.1. The CMOS circuit is designed for the respective logic gates using STR and Quad algorithm and then the power analysis is made at the output.

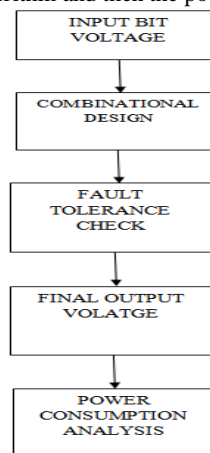


Fig 1 Flow diagram of the proposed algorithm

**Combinational Circuit Design in Tanner**

Combinational logic is a type of digital logic which is implemented with Booleans circuit, whose outputs is the pure function of present inputs. The basic NAND gate CMOS structure is represented in the Fig 2(a). NAND and NOR gates are universal gates. NAND gate is more efficient and low leakage circuit when compared to NOR.

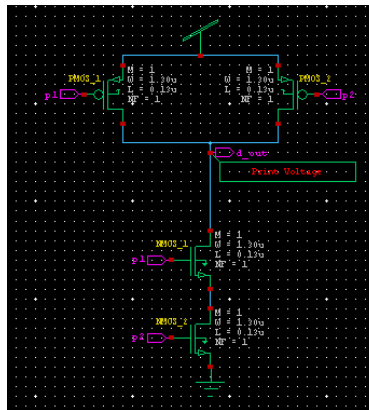


Fig 2 Basic CMOS NAND structure

**STR Algorithm**

The Selective Transistor Redundancy technique(STR) is applied to protect the transistor that have relatively high Probability Of Failure(POF) different arrangement of nMOS and pMOS transistors are designed for each gate for various transistor protection.

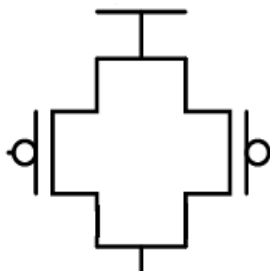


Fig 3 Basic STR structure for a transistor

The Fig 3 shows the basic STR structure for a transistor. To protect the NAND gate, all the transistors are duplicated. The Fig 4 shows the STR NAND structure in the Tanner tool.

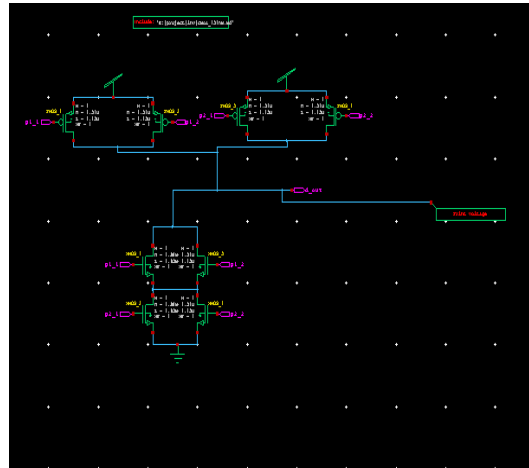


Fig 4 STR NAND structure

### QUAD Algorithm

The quadded algorithm uses four transistors for the function of the single transistor. An error in a single transistor can be stood by the quadded transistor. Many double errors can be tolerated as they do not occur in transistors placed in parallel the quadded transistor makes the circuit slower with an area overhead.

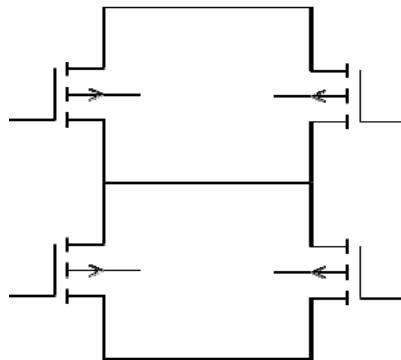


Fig 5 Basic Quadded structure for a transistor

The Fig 5 shows the basic Quad structure for a transistor. For the circuits having shorter paths for the primary input to the primary output quadded are not very effective. The Fig 6 shows the quadded NAND structure in the Tanner tool.

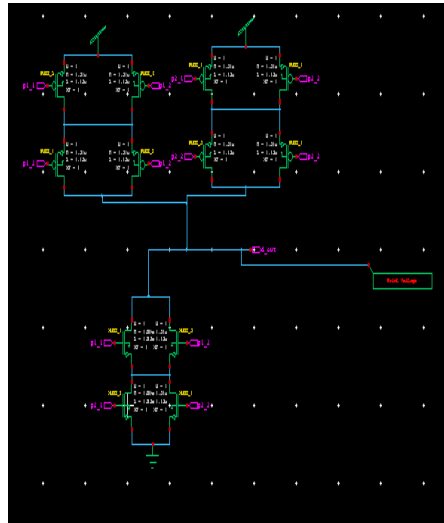


Fig 6 Quadded NAND structure

### V. EXPERIMENTAL RESULTS

The results obtained using the proposed algorithms is analyzed and tabulated in the fig.3. The quadded structure improves the reliability. The power analyze is done for both the algorithm.

Table 1 Power analyses of the algorithms

Fault Tolerance Algorithm	Power analyze (watt)	
STR algorithm	$P1 = 1.45e^{-8}$	$P2 = 4.852e^{-8}$
Quadded algorithm	$P1 = 1.05e^{-8}$	$P2 = 4.36e^{-8}$

### VI. CONCLUSION

The results of this algorithm shows that the STR algorithm consumes more power when compared to Quad algorithm. But when we comes to area overhead STR algorithm is efficient than Quad algorithm and Quad is not effective for simple primary circuits.

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