

# An Implementation of Full Adder Circuit using Modified Gate Diffusion Input Technique

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**ABSTRACT:** Full adder circuit is an essential component for designing of various digital systems. It is used for different applications such as Digital signal processor, microcontroller, and microprocessor and data processing units. Due to scaling trends and portability of electronic devices there is a high demand and need for low power and high speed digital circuits with small silicon area. So, design and analysis of low power and high performance adders are of great interest and any modification made to the full adder circuit would affect the performance of the entire system. This paper describes the design and analysis of MGDI based 1-bit full adder circuit for low power applications. This technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. This paper focuses two main design approaches. The former presents the implementation of modified primitive logic cells and its performance issues were compared with GDI and CMOS logic. The simulation results reveal better delay and power performance for the proposed modified GDI full adders when compared with the existing GDI technique, this paper presents low power high performance multiplexer based full adder design in Tanner EDA Tools using 45nm Technology. The power consumption comparison is also made based on CMOS and GDI design technique.

**KEYWORDS:** GDI (Gate Diffusion Input), Low Power Design, Full adder, modify GDI.

## I. INTRODUCTION

Binary addition is the basic operation found in most arithmetic components. Computation needs to be achieved by using area efficient circuits operating at high speed with low power consumption. Addition is the fundamental arithmetic operation and most fundamental arithmetic component of the processor is adder. Full Adder circuit plays an important role in low power applications. Hence the realization of full adders with low power and high performance is very essential. Obviously increasing the performance of 1-bit full adder circuit shows a great impact on increasing the performance of the entire system [1]-[2]. These adder cells commonly aimed to reduce power consumption, area and increase speed. To meet the growing demand a low power GDI based 1-bit full adder circuit has been designed which uses 10-T as compared to conventional 28-T full adder circuit. So the circuit reduces the MOS Transistor count, considerably decreasing the power consumption and improvement in power delay product. Designing low-power and high speed VLSI systems has emerged as highly in demand because of the fast growing technologies in communication and other battery power applications. Different design styles have been proposed to implement 1-bit adder cells [5]-[6]. One of the efficient low power technique known as Gate Diffusion Input (GDI) [7] is proposed by Morgenstern.

The rest of paper is organized as follows. Section 1 describes the conventional 1 bit full adder design. A Multiplexer performs the main function in high-speed data communication systems. A Multiplexer is the heart of Arithmetic and logic Unit [4] and used effectively in a number of applications including processors, processor bus, network switches and DSPs with resource sharing. A Multiplexer is also called as data selector as it selects one of the analog or digital inputs and forwarded to single output line [3]. The multiplexer of  $2^n$  inputs has  $n$  selection lines. This Paper analyzes 2x1 multiplexer using CMOS, GDI and Modified GDI with full swing.

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Performance characteristics of these technologies compared based on power consumption, delay and logic swing.

## II. PREVIOUS WORK

### CMOS DESIGN

CMOS logic Style have been used to implement the low power 1-bit adder cells. In general, they can be broadly divided into two major categories: the Complementary CMOS and the pass transistor circuits.

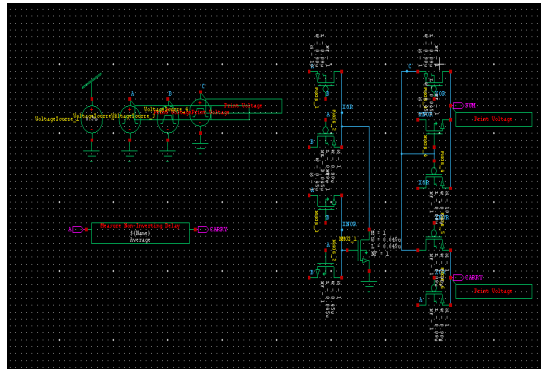


Fig 1: Full adder using CMOS

The disadvantages are:

1. Substantial number of transistor results in high input loads
2. More power consumption
3. Larger silicon area

### BASIC GDI CELL

The basic GDI cell consist of two transistors NMOS and PMOS with four terminals –G(common Gate Input), P(outer diffusion node of PMOS),N(outer diffusion node of NMOS) and D(common diffusion node)( see figure 1) .

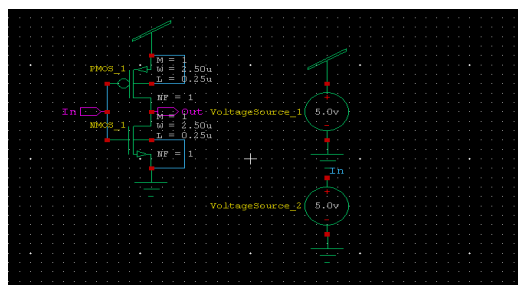


Fig 2: Basic GDI cell

The disadvantages of GDI are:

1. The circuit exhibits threshold drop and variation in  $V_t$  due to improper biasing of bulk terminals.
2. Increases the cost of fabrication due to floating bulk terminals.

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3. More static power dissipation.
4. The main limitation is output degraded when logic0 is transmitted by PMOS and similarly logic 1 transmitted by NMOS.

### GDI BASED DESIGN

The basic GDI cell shown in Fig.2 was proposed by Morgenstern. It is a new technique for low power digital combinational circuit design. This technique reduces power consumption, propagation delay and area of digital circuits

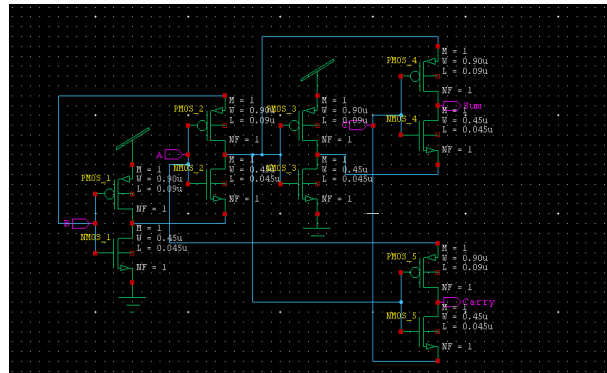


Fig 3: GDI based 10T Full Adder

In fig 2. M1, M3, M5, M7, and M9 are the PMOS transistor whereas M2, M4, M6, M8, and M10 are the NMOS transistors. A, B and Cin are taken as input and output of the circuit is drawn from the Sum and Cout.

### III. PROPOSED WORK

#### DESIGN OF MODIFIED GDI FULL ADDERS

A full adder is a combinational circuit that performs the arithmetic sum of three bits: A, B and a carry in, C, from a previous addition produces the corresponding SUM, S, and a carry out, CARRY. The various equations for SUM and CARRY are given below

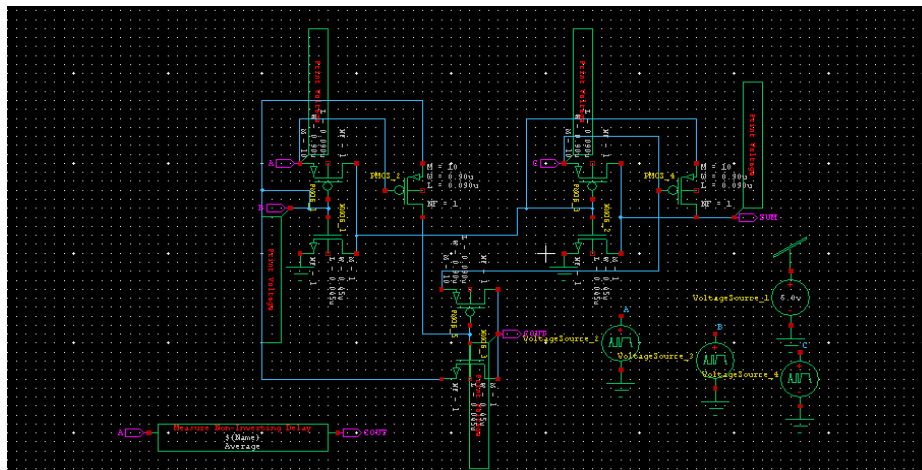


Fig 4: Modigy gate diffusion method using 8T

$$SUM = A \oplus B \oplus C$$

$$CARRY = \overline{(A \oplus B)}B + (A \oplus B)C$$

Finally 8T MGDI full adder from the figure, it has been realized using 3-input XOR for sum expression and for carry expression 2-to-1 MUX have been used. The proposed 5 different MGDI full adders are simulated using Tanner EDA with 45nm technology with supply voltage ranging from 1V to 5V in steps of 0.5V. All the full adders are simulated with multiple design corners (TT, FF, FS, and SS) to verify that operation across variations in device characteristics and environment. The design of 5 different full adders using MGDI method.

#### IV. COMPARISION & ANALYSIS

The entire simulations of GDI based 10-T full Adder circuit has been done using Tanner EDA tool on 180nm, 90nm, 65nm and 45nm technology. Here a detail analysis of average power consumption and delay of GDI based

adder on different technologies is presented so that it can be used for low power and high speed applications. clearly shows that as technology decreases average power of the circuit also reduces up to certain extent. The average power of the circuit reduces from 180 to 90 nm technology. So these results can be used for various low power and high speed applications. To establish an unbiased testing environment, the simulations have been carried out using a comprehensive input signal pattern, which covers every possible transition for a 1-bit full adder. The three inputs to the full adder are A, B, C and all the test vectors are generated and have been fed into the adder cell. Supply level to the moment the latest of the SUM and CARRY signals reach the same voltage level. All transitions from an input combination to another (total 8 patterns 000, 001, 010, 011, 100, 101, 110, 111) have been tested, and the delay at each transition has been measured. The average has been reported as the cell delay. The power consumption is also measured for these input patterns and its average power has been reported.

#### V. SIMULATION AND RESULT

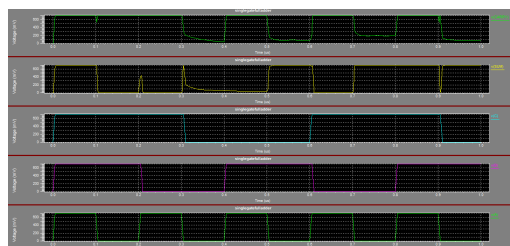


Fig.5. Output wave form Full adder using cmos

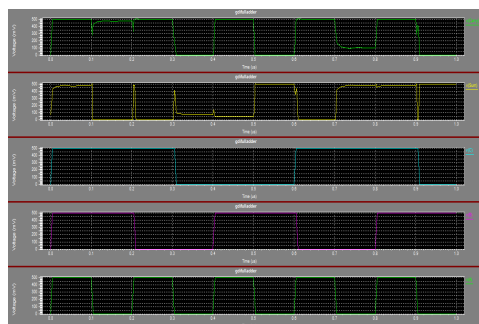


Fig.6. Output wave form Full adder using gdi

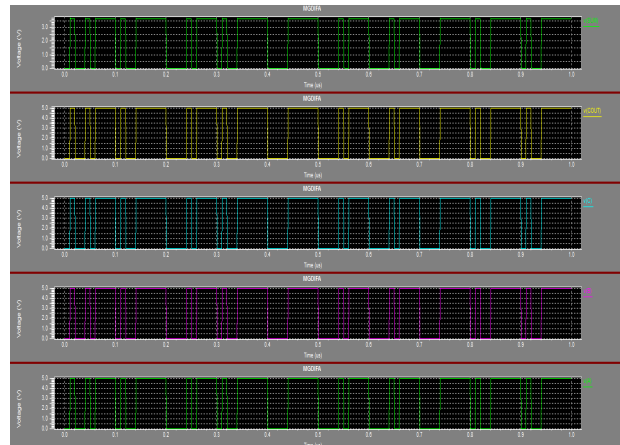


Fig 7: Output waveform of 8T MGDI

## VI. CONCLUSION

An extensive performance analysis of modified primitive cells of AND, OR, NAND, NOR, XOR and XNOR has been presented. The performance of these MGDI was analysed in terms of transistor count, delay and power dissipation using Tanner EDA 45nm technology and it is compared with conventional GDI and CMOS logic. The simulation results reveal better delay and power performance of proposed primitive cells as compared to existing GDI cell and CMOS at 0.90 $\mu$ m technologies. Subsequently different 1-bit full adder cells have been presented. From this analysis it is observed that the full adder cells designed with MGDI has the transistor count of In GDI the number of transistor to implement XOR will take 4 transistors whereas in modified GDI it is implemented with 3 transistors. In case of CMOS the transistor count is approximately double that of MGDI adders.

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