

Design of Adders and 4-2 Compressors for Approximate Multipliers

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ABSTRACT: Approximate computing can decrease the design complication with an increase in performance and power efficiency for error tolerant applications like multimedia signal processing and data mining which can tolerate error, exact computing units is not always necessary. They can be replaced with their approximate counterparts. A new design approach for approximation of multipliers based on partial products is altered to introduce varying probability terms. Logic complexity of approximation is usually varied for the accumulation of modified partial products. Adders and multipliers form the key components in these applications. In Existing system, Implementation of multiplier comprises three steps generation of partial products, partial products reduction tree, and vector merge addition to produce final product from the sum and carry rows generated from the reduction tree. Second step consumes more power. To reduce power and improve approximate difference, a novel compressor based approximate multiplier is proposed. Approximate compressor is proposed to further increase performance as well as reducing the error rate.

KEYWORDS: Approximate Computing, Compressor, Partial Products, Multipliers.

I. INTRODUCTION

In applications like signal processing and data mining that can be able to tolerate error, exact values are not always needed [1][2]. They can be replaced with approximate counterparts. Study on approximate computing for error resilient applications is on the rise. Adders and multipliers are the key components in these applications [3]. The approximate full adders are proposed at transistor level and they are utilized in multimedia signal processing applications. Their proposed full adders are used in accumulation of partial products in multipliers [4]. To reduce hardware of multipliers, round off is widely employed in fixed-width multiplier designs. Then a variable or constant correction term is added for the quantization error introduced in the truncated part. Approximation techniques in multipliers focus on accumulation of partial products, which is crucial in power consumption[5][6]. In two designs of approximate 4-2 compressors are presented and then used in partial product reduction tree of four variants of 8×8 multiplier [7]. The major drawback of the proposed compressors is that they produce nonzero output for zero inputs, which largely affects the mean relative error (MRE). The approximate design which is proposed overcomes the existing drawback. In 2×2 approximate multiplier based on changing an values in the Karnaugh map is proposed and used as a building block to form 4×4 and 8×8 multipliers [8]. The inaccurate counter design has been proposed for application in Wallace tree multiplier. A new approximate half and full adder is proposed which is utilized in the accumulation of partial products of multiplier [9]. Lowering supply voltage creates paths failing to meet delay constraints which lead to error. Reduced arithmetic units (half-adder, full-adder, and 4-2 compressor) are proposed for approximation. The proposed multipliers are better since it reduces the area, power, and error [10]. The rest of this process is described as follows. Section II details the existing architecture. The architecture of proposed system is explained in the section III. Section IV provides the result analysis of the proposed and existing approximate multipliers. Section V describes the conclusion.

II. RELATED WORK

Implementation of multiplier generally comprises of three steps. They are generation of partial products, partial products reduction tree, and vector merge addition to produce final product from the sum and carry rows generated from the reduction tree [11]. In this second step consumes lots of power. In this process, approximation is applied in second stage [12].

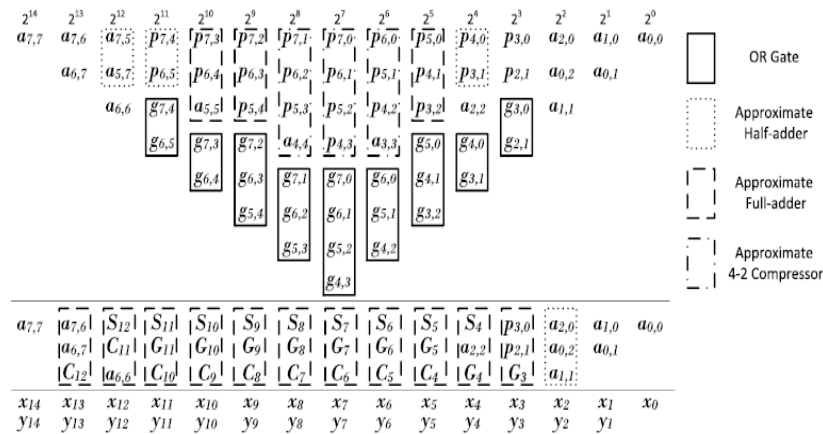


Fig. 1. Reduction of partial products of multiplier.

Two approximate 4-2 compressors in produce nonzero output even for the zero inputs [13][14]. This results in high ED and high degree of precision loss especially in cases of zeros in all bits or in most significant parts of the reduction tree [15]. The fig 2 shows the existing 4-2 compressor. The equations for existing compressor are given as,

$$\text{Sum} = (X_1 \oplus X_2) \cdot (X_3 \oplus X_4) + (X_1 \oplus X_2)' \cdot (X_3 \oplus X_4) \cdot C_{in}' + [(X_1 \oplus X_2) \cdot (X_3 \oplus X_4)' + (X_1 \oplus X_2)' \cdot (X_3 \oplus X_4)] \cdot C_{in}$$

$$C_{out} = (X_1 \oplus X_2) \cdot X_3 + (X_1 \oplus X_2)' \cdot X_4$$

$$\text{Carry} = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot C_{in} + (X_1 \oplus X_2 \oplus X_3 \oplus X_4)'$$

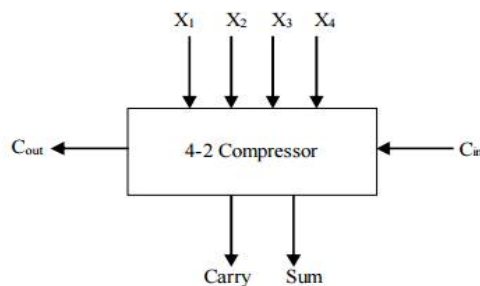


Fig 2: Existing 4-2 compressor

III. PROPOSED WORK

Approximate half-adder, full-adder, and 4-2 compressor are used. In adders and 4-2 compressors, EXOR gates tend to contribute high amount of area and power. For the process of approximating half-adder, EXOR gate of the *Sum* is changed with OR gate. This results in one error in the *Sum* output.

$$Sum = x1 + x2$$

$$Carr y = x1 \cdot x2.$$

In the process of approximation of full-adder in the multiplier, one of the two EXOR gates is replaced with OR gate to reduce hardware complexity. This results in change of values of output in last two cases out of eight cases. *Carry* is altered in such a way it has one error. This process provides more simplification, while maintaining the difference between original and approximate value as one in the carry. But the absolute difference is two in case of sum.

$$W = (x1 + x2)$$

$$Sum = W \oplus x3$$

$$Carr y = W \cdot x3.$$

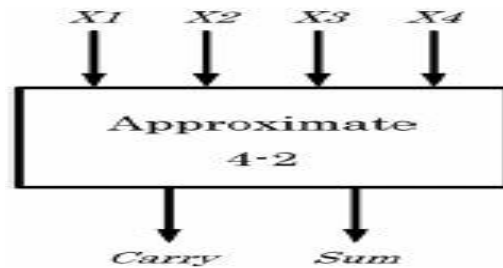


Fig. 3. Proposed compressor design.

The proposed 4-2 compressor in fig overcomes this disadvantage. In 4-2 compressor, three bits are needed for the output only when the four inputs are equal to 1. This brief has been accepted in a future issue. For *Sum* computation, one of three XOR gates is replaced with one OR gate. Also, to make the *Sum* corresponding to the case where all inputs are ones as one, an additional circuit $x1 \cdot x2 \cdot x3 \cdot x4$ is added to the *Sum* expression. This results in reduction of number of absolute difference. Sum and carry for proposed compressor is simplified as

$$SUM' = \overline{(x1 \oplus x2 + x3 \oplus x4)}$$

$$CARRY' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

The approximate 4-2 compressor in the fig 4 can be explained in the form logic diagram shown in the below fig 5.

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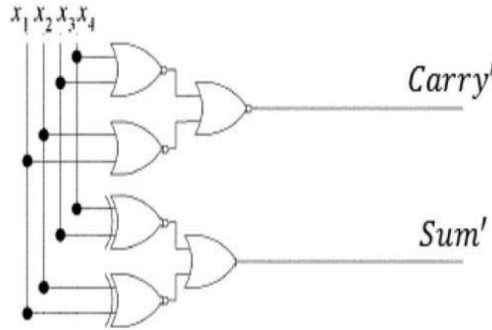


Fig 5: logic diagram of proposed approximate 4-2 compressor.

IV. EXPERIMENTAL RESULTS

For the proposed multipliers, the altered partial products are generated and compressed using approximate half-adder, full-adder, and 4-2 compressor structures to form final two rows of partial products. The efficiency of the proposed multipliers is then compared with the existing approximate multipliers. The truth table for the proposed adders and 4-2 compressor along with the simulated output are shown below.

Table 1: Truth table for half adder

INPUTS		EXACT OUTPUTS		APPROXIMATE OUTPUTS		ABSOLUTE DIFFERENCE
X1	X2	CARRY	SUM	CARRY	SUM	
0	0	0	0	0✓	0✓	0
1	0	0	1	0✓	1✓	0
0	1	0	1	0✓	1✓	0
1	1	1	0	1✓	1*	1

Table 2: Truth table for full adder

INPUTS			EXACT OUTPUTS		APPROXIMATE OUTPUTS		ABSOLUTE DIFFERENCE
X1	X2	X3	CARRY	SUM	CARRY	SUM	
0	0	0	0	0	0✓	0✓	0
0	0	1	0	1	0✓	1✓	0
0	1	0	0	1	0✓	1✓	0
0	1	1	1	0	1✓	0✓	0
1	0	0	0	1	0✓	1✓	0
1	0	1	1	0	1✓	0✓	0
1	1	0	1	0	0*	1*	1
1	1	1	1	1	1✓	0*	1

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Table 3: Truth table for 4-2 compressor

INPUTS				EXISTING OUTPUTS		PROPOSED OUTPUTS		ABSOLUTE DIFFERENCE	
X1	X2	X3	X4	CARRY	SUM	CARRY	SUM	EXISTING	PROPOSED
0	0	0	0	0✓	0✓	0*	1*	0✓	1*
0	0	0	1	0✓	1✓	0✓	1✓	0✓	0✓
0	0	1	0	0✓	1✓	0✓	1✓	0✓	0✓
0	0	1	1	1✓	0✓	0*	1*	0✓	1*
0	1	0	0	0✓	1✓	0✓	1✓	0✓	0✓
0	1	0	1	0*	1*	1✓	0✓	1*	0✓
0	1	1	0	0*	1*	1✓	0✓	1*	0✓
0	1	1	1	1✓	1✓	1✓	1✓	0✓	0✓
1	0	0	0	0✓	1✓	0✓	1✓	0✓	0✓
1	0	0	1	0*	1*	1✓	0✓	1*	0✓
1	0	1	0	0*	1*	1✓	0✓	1*	0✓
1	0	1	1	1✓	1✓	1✓	1✓	0✓	0✓
1	1	0	0	1✓	0✓	0*	1*	0✓	1*
1	1	0	1	1✓	1✓	1✓	1✓	0✓	0✓
1	1	1	0	1✓	1✓	1✓	1✓	0✓	0✓
1	1	1	1	1*	1*	1*	1*	1*	1*



Fig 6: simulated output for half adders.

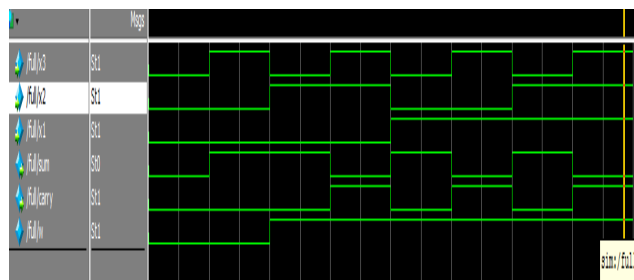


Fig 7: Simulated output for full adders.

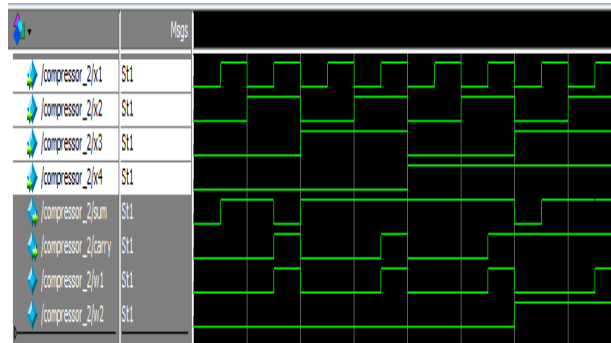


Fig 8: Simulated output for existing compressor.

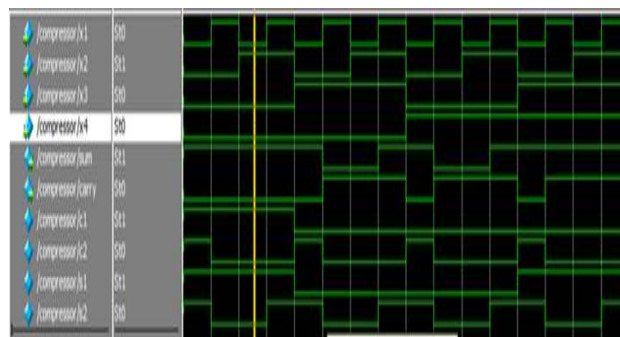


FIG 9: SIMULATED OUTPUT FOR PROPOSED COMPRESSOR.

V. CONCLUSION

In this procedure, to propose efficient approximate multipliers, partial products of the multiplier are altered using generate and propagate signals. Approximation is applied using simple OR gate for altered generate partial products. Approximate half-adder, full-adder, and 4-2 compressor are proposed to reduce remaining partial products. Two variants of approximate multipliers are proposed. They also have good precision when compared to existing approximate multiplier designs. The proposed 4-2 compressor consists of only four absolute differences whereas the existing consists of five absolute differences. This results in the reduction of area and power consumption. The proposed multiplier designs can be used in applications with minimum loss in output quality while reducing significant power and area.

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