

Analysis of Stuck on and off Fault in SRAM based FPGA

Chitra.A¹, Vijay Murugan.S²

PG Scholar, Department of ECE, Adhiyamaan College of Engineering, Hosur, TN, India¹

Associate Professor, Department of ECE, Adhiyamaan College of Engineering, Hosur, TN, India²

ABSTRACT: A new scan-based Built-In Self-Test (BIST) architecture is designed with Low-Power (LP) for weighted pseudorandom test pattern generation (WPTPG) and reseeding, that is possible for the pseudorandom testing and deterministic BIST. The proposed technique of a BIST design for fault detection and fault diagnosis of Static-RAM (SRAM) based Field Programmable Gate Array (FPGAs) can detect and diagnose the stuck on and stuck off in the local interconnect resources. The test pattern generator and output response analyzer are configured by CLBs in FPGAs. The testing technique takes place in three major test blocks. They are Test Pattern Generator (TPG), Output Response Analyzer (ORA) and Block Under Test (BUT) in each test block. The stuck on and off faults are detected using SRAM based FPGA which are observed in this paper.

KEYWORDS: Low-power, BIST, CLBs, FPGA.

I. INTRODUCTION

An FPGA consists of logic and interconnect resources that permit to configure an uncommitted chip into the desired functions for different applications[1][2]. The common FPGA architecture consists of a two dimensional array of Configurable Logic Blocks (CLBs), a programmable interconnect (made of nets and switches) and programmable Input/Outputs (IOs). Currently, the programmable interconnect accounts for more than 80 percent of the FPGA programmable resources (usually stacked up in eight metal layers)[3]. Therefore, nets in the interconnect resources are very vulnerable to faults both at manufacturing as well as run time. For interconnect resources, FPGA testing methodologies are broadly classified as application-dependent and application independent. Application independent testing (also known as manufacturing test) utilizes nearly exhaustive test sets such that all programmable resources are tested for faults.

In contrast, conventional Built In Self-Test (BIST) approaches introduce both area overhead (typically between 10% and 30%) and delay penalties[4]. The BIST approach can be applied to any in-circuit reprogrammable SRAM-based FPGAs. The only cost will be the additional memory for storing the data required to reconfigure the FPGA. This paper is categorized as follows. Section II is related works of the project. Section III consists of proposed system with the fault structure. Section IV is categorized with results and finally concluded the paper in section V.

II. RELATED WORK

This method generates the degraded sub-circuits for all subsets of scan chains in the following way. All PPIs related to the disabled scan chains are randomly assigned specified values (1 and 0)[5]. For any gate, the gate is removed if its output is specified; the input can be removed from a NAND, NOR, AND, and OR gates if the input is assigned a no controlling value and it has at least three inputs. For a two-input AND or OR gate, the gate is removed if one of its inputs is assigned a no controlling value. For a NOR or NAND gate, the gate degrades to an inverter if one of its inputs is assigned a no controlling value[6].

For an XOR or NXOR gate with more than three inputs, the input is simply removed from the circuit if one of its inputs is assigned value 0[7]; the input is removed if it is assigned value 1, an XOR gate changes to an

NXOR gate, and an NXOR gate changes to an XOR gate. For an XOR gate with two inputs, and one of its inputs is assigned value 0, the gate is deleted from the circuit[8]. For a two-input NXOR gate, the gate degrades to an inverter[9]. If one of its inputs is assigned value 1, a two-input XOR gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input NXOR gate can be removed from the circuit[10].

Usually, a small LFSR constructed by a primitive polynomial is sufficient when a well-designed PS is adopted in the pseudorandom testing phase. In our method, a combination of a small LFSR and the PS from is used to generate test patterns in the pseudorandom testing phase.

LOW-POWER DETERMINISTIC BIST AND RESEEDING

An effective seed encoding scheme is used here to reduce the storage requirements for the deterministic test patterns of the random-pattern-resistant faults. The encoded seed is shifted into the LFSR first. A deterministic test vector is shifted into the scan trees that are activated by the gating logic, where each scan-in signal drives a number of scan trees, and only one of the scan trees driven by the same scan-in signal is activated. The extra variables are injected into the LFSR when the seed is shifted into the activated scan trees. The gating logic, partitions scan trees into multiple groups. The first group of scan trees is disabled after they have received the test data. The second group of scan trees is activated simultaneously, and all other scan trees are disabled. The seed can be stored in an extra shadow register, which is reloaded to the LFSR in a single clock cycle. The scan shift operations are repeated when the extra variables are injected into the LFSR. This process continues until all scan trees have received test data.

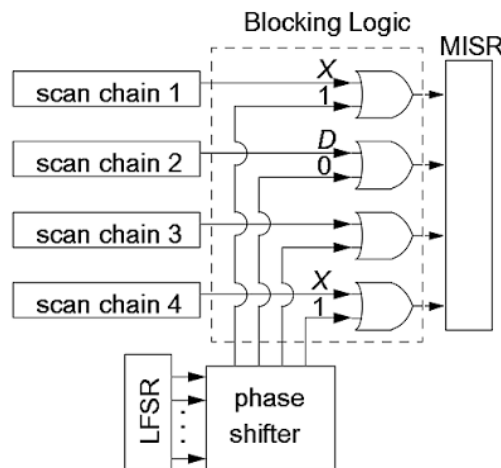


Fig 1: Block diagram for reseeding

The outputs of all scan chains, which are driven by the same clock signal, are connected to the same response compactor during the deterministic BIST phase. This offers additional flexibility for test encoding. The test responses of the previous test vector can be shifted out with only a few clock cycles (corresponding to the depth of the scan trees in the pseudorandom testing phase). For scan chain architecture, the number of clock cycles needed to shift-out test responses of the previous deterministic test vector is much larger. The proposed LP tree-based architecture makes the reseeding scheme much easier to implement.

III. PROPOSED ARCHITECTURE

BIST techniques in general are associated with high performance; they are also associated with high area overhead incurred by on-chip test hardware. However, the BIST overhead is not an issue for FPGA BIST because the test hardware is easily reconfigured by inserting and removing test pattern generators (TPGs) and

ORAs. This is particularly important for the testing of FPGAs. The testing strategy of the proposed FPGA BIST structure is to configure groups of ten CLBs into a test block, as illustrated in Fig.2

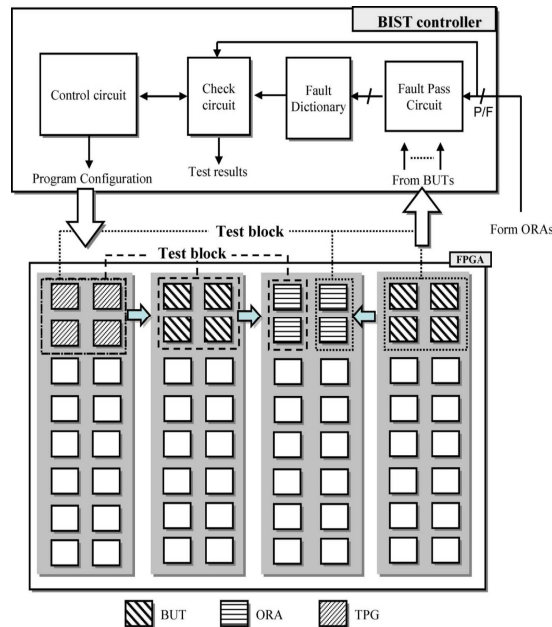


Fig 2: FPGA BIST Architecture

TEST PATTERN GENERATOR (TPG)

TPG is an address generator, which consists of eight MUXs, eight LUTs, and eight DFFs .To continuously generate the addresses (0–15) in the LUTs to produce the corresponding test patterns. According to the MUX selections, the LUTs addresses can be figured out in sequence, and the test patterns can be generated by repeatedly checking the contents.

OUTPUT RESPONSE ANALYZER (ORA)

The two-input XOR gate and three-input OR gate in the ORA are used to test the global interconnect open and short faults, respectively. The faults presented in the LUTs and local interconnects are detected by using the 4-input parity checker. The P/F checker in the ORA circuit is designed to generate a P/F signal to trigger the fault pass circuit to deliver the faults from the primary outputs of a BUT to the fault dictionary for fault diagnosis.

LOCAL INTERCONNECT FAULT

Fig MUX-PSs with stuck on/off faults in the local interconnects. Note that a stuck-on/off fault causes the pass transistor in MUX-PSs to be permanently on/off, regardless of the value of the SRAM cell controlling the pass transistor in MUX-PSs. An open fault in the global interconnect is a disconnection of any wires, while a short fault indicates a bridging between two wires.

Organized by

Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

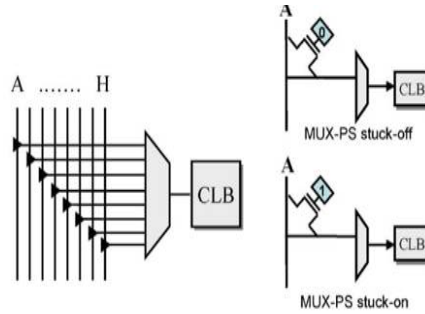


Fig 3.3.3 Local interconnect fault

IV. RESULTS AND DISCUSSIONS

The simulation results are shown below. The stuck-on fault occurs when the circuit is short circuited instead of open circuit and vice-versa for stuck off fault. It can be identified using 0 & 1. The stuck on is represented as 1 and stuck off is given as 0. In table 1, the stuck on fault is occurred at B and the stuck off fault is occurred at F.

TABLE 1: RESULTS OF STUCK ON AND OFF FAULTS

	INPUTS	Stuck on fault	Stuck off fault
A	0	0	0
B	0	1	0
C	0	0	0
D	0	0	0
E	1	1	1
F	1	1	0
G	1	1	1
H	1	1	1

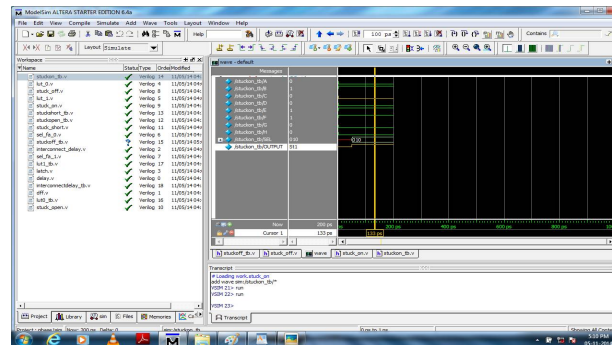


Fig 3: Simulation result of stuck on fault

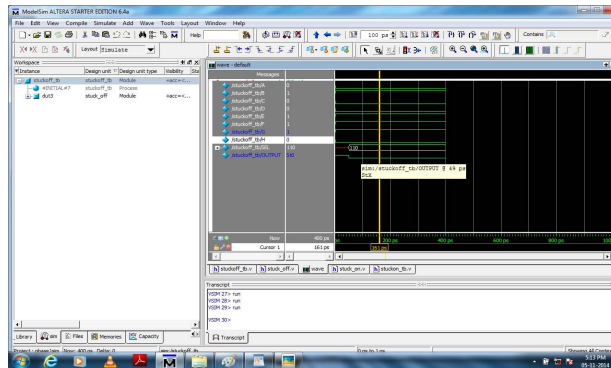


Fig 4: Simulation result of stuck off fault

V.CONCLUSION

There are two major complexities are faced in the existing design. They are, BSF detects each possible wire faults by the all zero vector. It is not guaranteed to identify the open faults. Thus, this is rectified in this paper using SRAM-based FPGA design. The faults analysed in the proposed BIST structure are stuck on and stuck off faults. In future, interconnect delay faults, LUT faults can be analysed using this same technique in SRAM based FPGA. Hence, this paper gives a clear idea for high fault coverage in low power with SRAM based FPGA.

REFERENCES

- [1] Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding Dong Xiang, Senior Member, IEEE, Xiaoqing Wen, Fellow, IEEE, and Laung-Terng Wang, Fellow, IEEE.2016.
- [2] A Reconfigurable Scan Architecture With Weighted Scan-Enable Signals for Deterministic BIST Dong Xiang, Senior Member, IEEE, Yang Zhao, Krishnendu Chakrabarty, Fellow, IEEE, and Hideo Fujiwara, Fellow, IEEE.2008.
- [3] M. Chatterjee and D. K. Pradhan, "A BIST pattern generator design for near-perfect fault coverage," *IEEE Trans. Comput.*, vol. 52, no. 12, pp. 1543–1558, Dec 2003.
- [4] A. S. Abu-Issa and S. F. Quigley, "Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 28, no. 5, pp. 755–759, May 2009.
- [5] S. Banerjee, D. R. Chowdhury, and B. B. Bhattacharya, "An efficient scan tree design for compact test pattern set," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 26, no. 7, pp. 1331–1339, Jul. 2007.
- [6] P. H. Bardell, W. H. McAnney, and J. Savir, *Built in Test for VLSI: Pseudorandom Techniques*. New York, NY, USA: Wiley, 1987.
- [7] N. Z. Basturkmen, S. M. Reddy, and I. Pomeranz, "A low power pseudorandom BIST technique," *J. Electron. Test., Theory Appl.*, vol. 19, no. 6, pp. 637–644, Dec. 2003.
- [8] V. D. Agrawal, C. R. Kime, and K. K. Saluja, "A tutorial on built-in selftest.I. Principles," *IEEE Des. Test Comput.*, vol. 10, no. 1, pp. 73–82, Mar. 1993.
- [9] R. Kapur, S. Patil, T. J. Sneath, and T. W. Williams, "A weighted random pattern test generation system," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 15, no. 8, pp. 1020–1025, Aug. 1996.
- [10] G. Kiefer and H.-J. Wunderlich, "Deterministic BIST with multiple scan chains," *J. Electron. Test.*, vol. 14, no. 1, pp. 85–93, Feb. 1999.
- [11] R. Kapur, S. Patil, T. J. Sneath, and T. W. Williams, "A weighted random pattern test generation system," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 15, no. 8, pp. 1020–1025, Aug. 1996.
- [12] C. Zhang, W. Yu, Q. Wang, and Y. Shi, "Fast random walk based capacitance extraction for the 3-D IC structures with cylindrical intertier-vias," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 34, no. 12, pp. 1977–1990, Dec. 2015.
- [13] X. Zhang, W. Shan, and K. Roy, "Low-power weighted random pattern testing," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 19, no. 11, pp. 1389–1398, Nov. 2000.
- [14] D. Xiang, M. Chen, and H. Fujiwara, "Using weighted scan enable signals to improve test effectiveness of scan-based BIST," *IEEE Trans. Comput.*, vol.56, no. 12, pp. 1619–1628, Dec. 2007.
- [15] X. Wen *et al.*, "Low-capture-power test generation for scan-based at speed testing," in *Proc. Int. Test Conf.*, Nov. 2005, pp. 1018–1028, paper 39.2.