

An Efficient Implementation of Multiplier Using Modified Carry Select Adder

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ABSTRACT: Multipliers are the fundamental components in all digital processing systems. Multiplier is a circuit used to perform arithmetic operation which computes multiplication of binary numbers. Several techniques involve computing a set of partial products, and then summing the partial products together. Multiplier is a key element of many high performance systems like FIR filters, Microprocessors, ALU, DSP applications and it is a vital component to examine the performance of the system. Here we are going to design and analyse various multiplier circuits. Generally multiplier uses adders for fast computation process. In that criteria, modified Carry Select Adder is used as it is fast and efficient when compare to other type of adders. The Carry Select Adder (CSLA) is used in computational systems which separately generates multiple carries and then select the carry to generate the sum. The analysis is to be performed and expecting the efficiency in terms delay and area.

KEYWORDS: Adders, Area, Computation, Speed.

I. INTRODUCTION

The design of arithmetic circuits using conventional gates consumes more power and area occupied by the design is also large, in order to reduce the power consumed by the gates various fast adders are used. Multiplier is a circuit used to perform arithmetic operation which computes multiplication of binary numbers. Multiplier is a key element of many high performance systems like fir filters, microprocessors, ALU, DSP applications. An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. Although adders can be constructed for many number representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder-subtractor. Other signed number representations require more logic around the basic adder.

II. MULTIPLIER

Multipliers are the fundamental components in all digital processing systems. Multiplier is a circuit used to perform arithmetic operation which computes multiplication of binary numbers. Several techniques involve computing a set of partial products, and then summing the partial products together. Multiplier is a key element of many high performance systems like FIR filters, Microprocessors, ALU, DSP applications and it is a vital component to examine the performance of the system. Here we are going to design and analyze various multiplier circuits. Generally multiplier uses adders for fast computation process.

III. MULTIPLIER USING RIPPLE CARRY ADDER

Multiplier design consists of number of ripple carry adder and cascading the multipliers. Ripple carry adder consists of inputs [A (3 down to 0), B (3 down to 0)] and outputs [sum and carry]. Implementation of full adder circuit using conventional gates. It is used to add N bit number by cascading number of full adders in parallel. To design 8-bit multiplier using ripple carry adder, the design consists of four 4x4 multipliers and three 8-bit ripple carry adders.

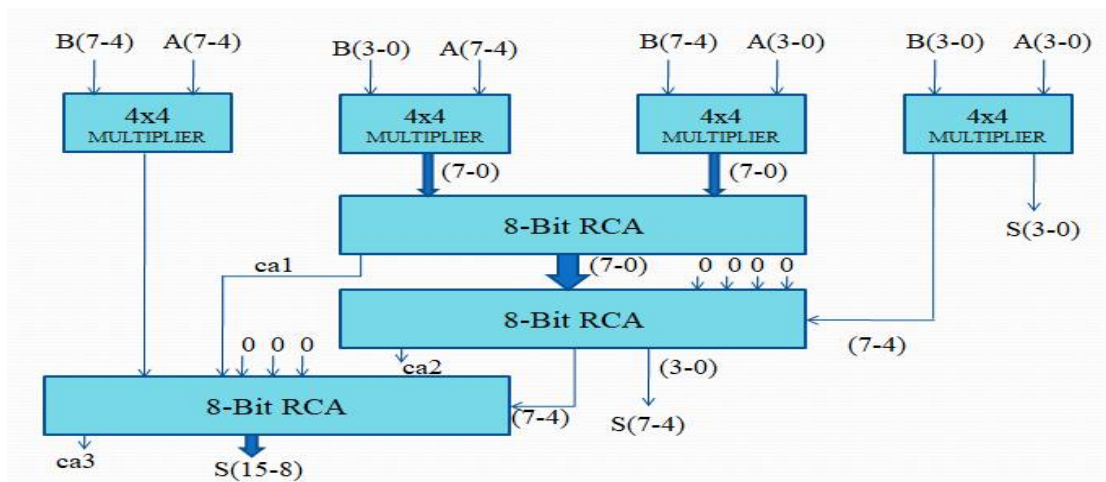


Fig 1: Design of 8-bit multiplier using ripple carry adder

IV. MULTIPLIER USING CARRY LOOKAHEAD ADDER

Multiplier using carry lookahead adder consists of ripple carry adder and partial full adders. In carry lookahead adder to determine carry output bits it improves the speed by reducing the amount of time required. Usually carry look ahead is slower than the normal ripple carry adder. The circuit diagram consist if four 4x4 multiplier and a carry look ahead adder

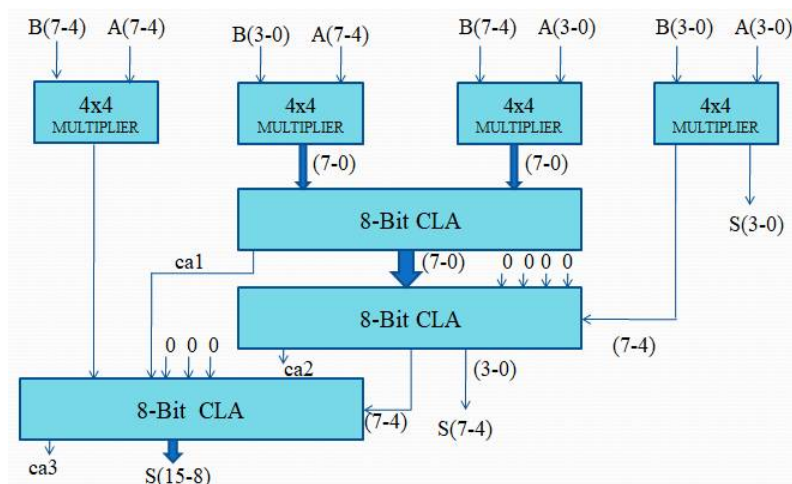


Fig 2: Design of 8-bit multiplier using carry lookahead adder

V. MULTIPLIER USING CARRY SELECT ADDER

Multiplier using carry select adder consists of multiplexer and number of full adders. The fastest adder of conventional adder is carry select adder. In a carry-select adder addition of two ripple carry adders with a two n-bit numbers, in order to perform the calculation and analyse the carry bits of the carry select adder.

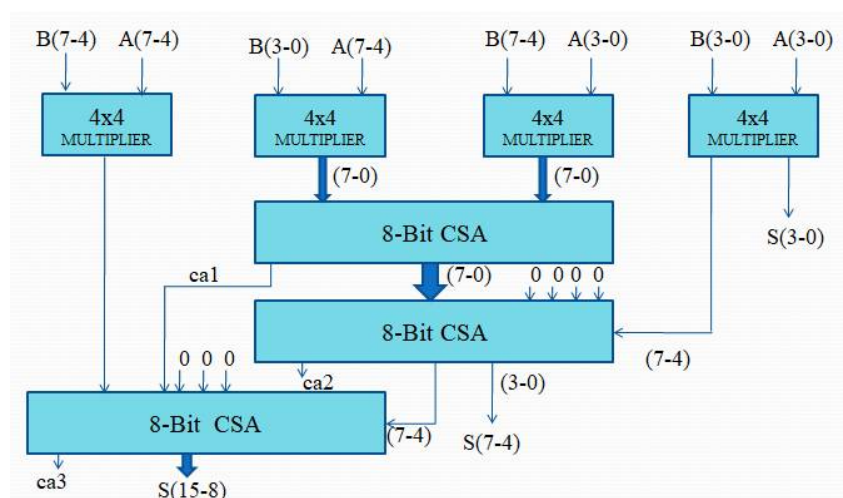


Fig 3: Design of 8-bit multiplier using carry select adder

VI. MULTIPLIER USING MODIFIED CARRY SELECT ADDER

Multiplier using modified carry select adder consist of four 4x4 multiplier and three 8-bit modified carry select adder.

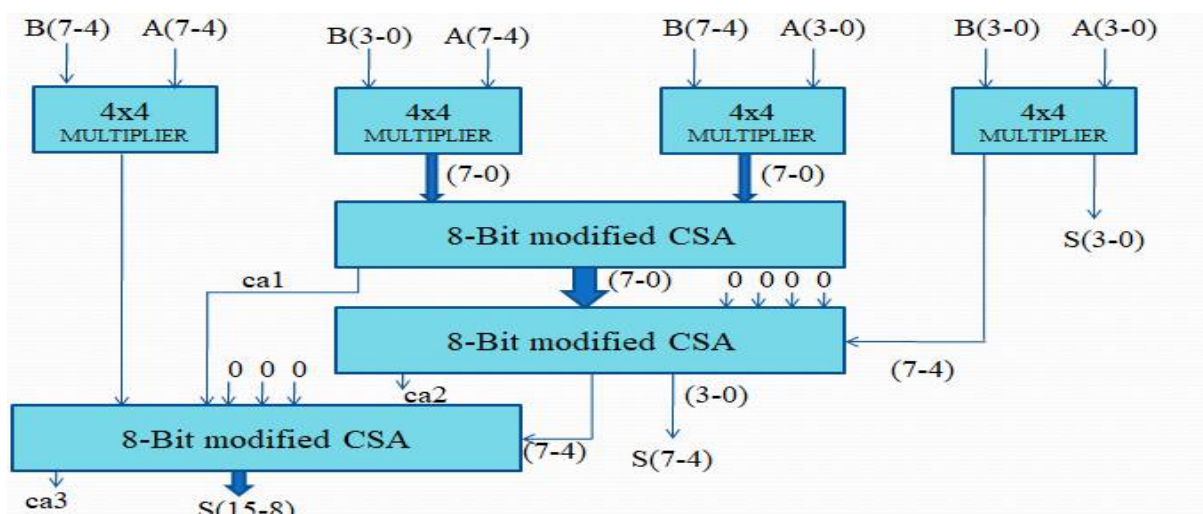


Fig 4: Design of multiplier using modified carry adder

The modified carry select adder consist of combination of 16-bit ripple carry adder and a half adder it is given to the 16-bit basic unit which contains the logic gate functions like NOT gate and XOR gate which it is given to the multiplexer .The multiplexer producing the outputs like 16-bit sum and carry bits.

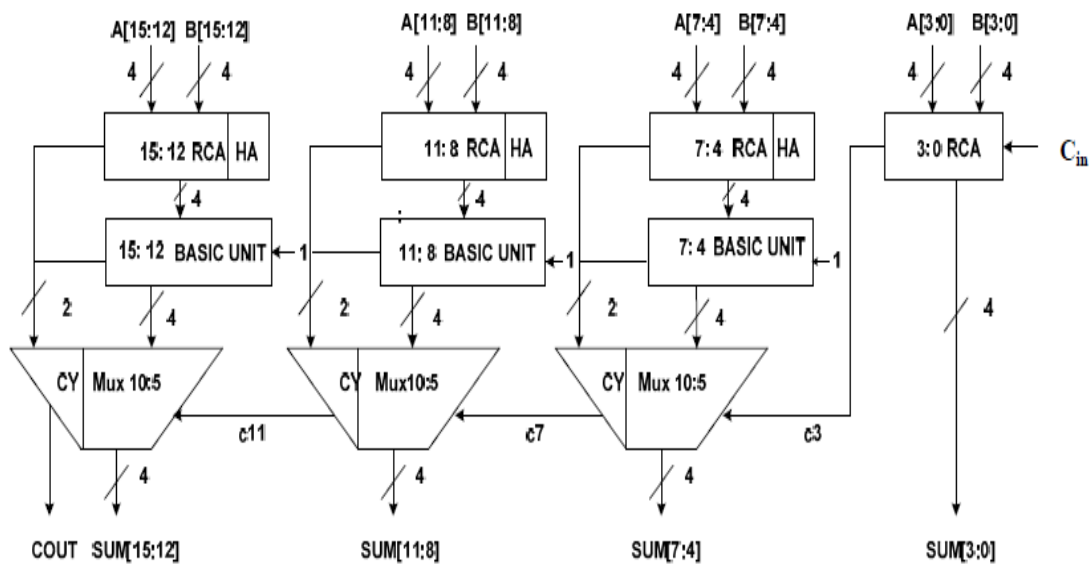
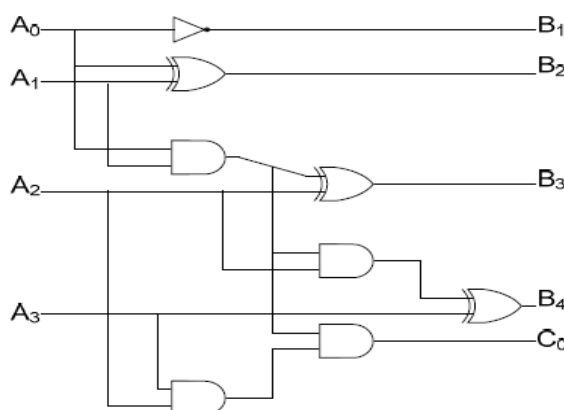


Fig 5: Functional Block

The basic unit of carry select rights consist of inputs A0,A1,A2,A3 and outputs B1,B2,B3,B4 ,C0.It has the basic logic functions like Not gate and XOR gate



$$\begin{aligned}
 B1 &= \sim A0; \\
 B2 &= A1 \wedge A0; \\
 C1 &= A1 * A0; \\
 C2 &= A2 * A3; \\
 C0 &= C1 * C2; \\
 B3 &= A2 \wedge C1; \\
 B4 &= A3 \wedge C3;
 \end{aligned}$$

Fig 6: Basic unit of modified carry select adder

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VII. RESULTS AND DISCUSSIONS

1. The output waveform of multiplier using ripple adder



Fig 7: Output waveform of 16-bit multiplier using ripple carry adder

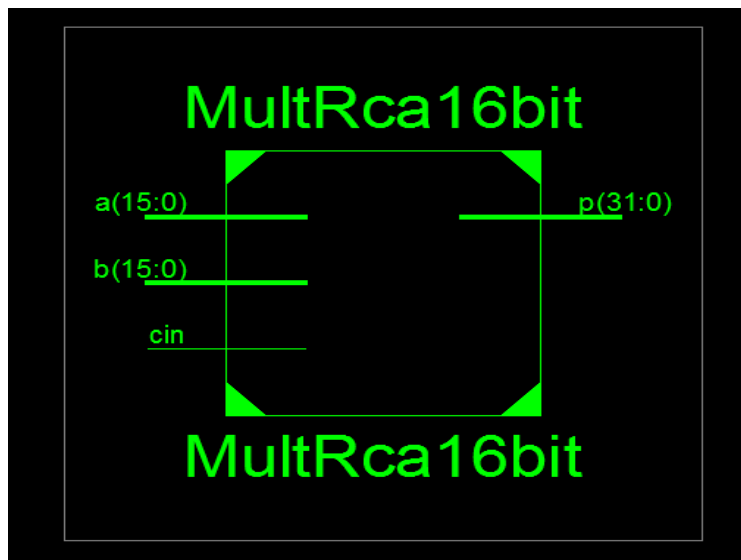


Fig 8: RTL schematic of multiplier using ripple carry adder

2. The output waveform of multiplier using carry lookahead adder

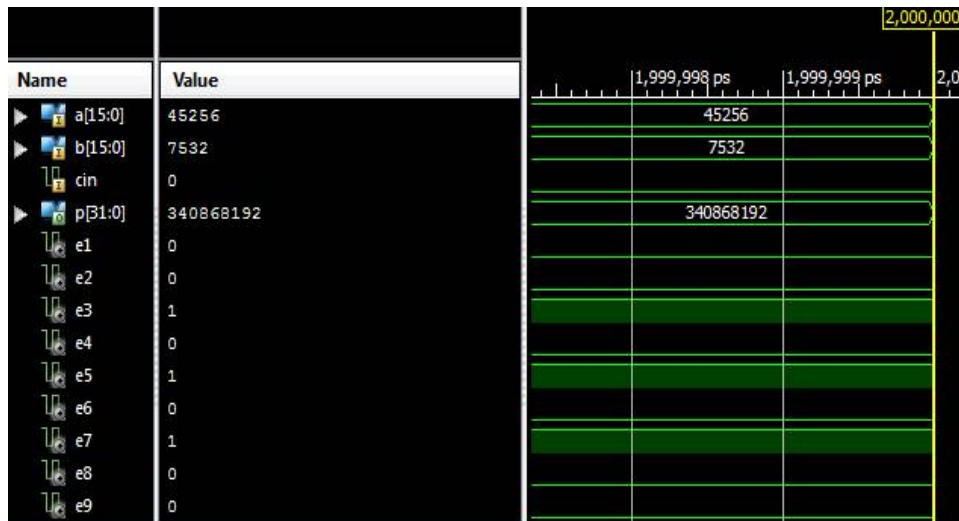


Fig 9: Output waveform of multiplier using carry look ahead adder

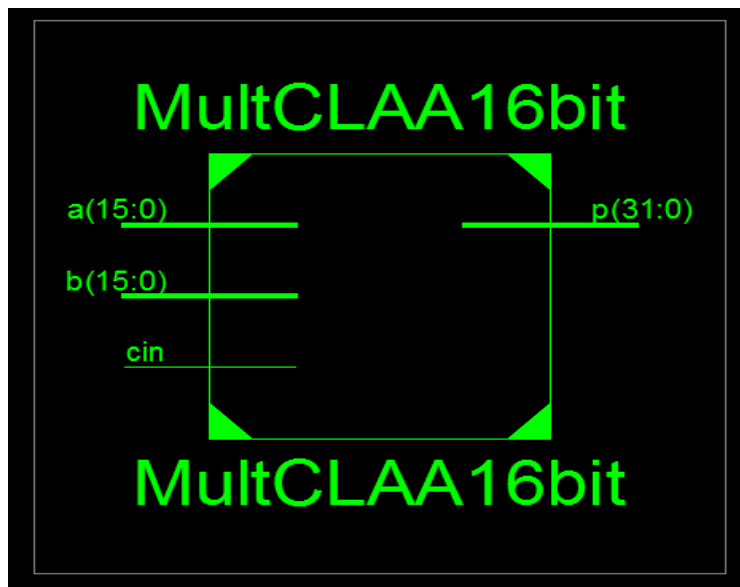


Fig 10: RTL schematic of multiplier using carry lookahead adder

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3. The output waveform of multiplier using carry select adder

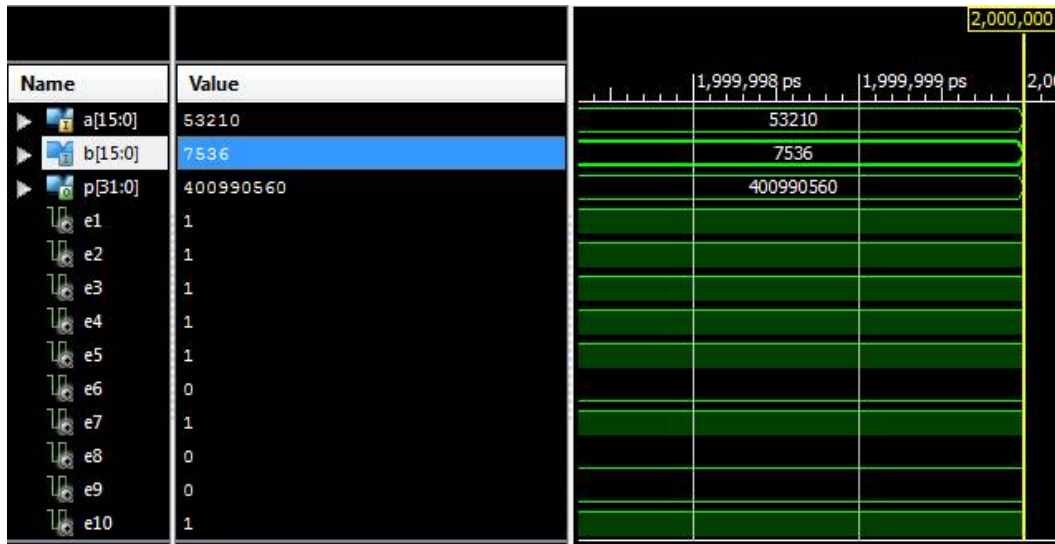


Fig 11: Output waveform of 16-bit multiplier using carry select adder

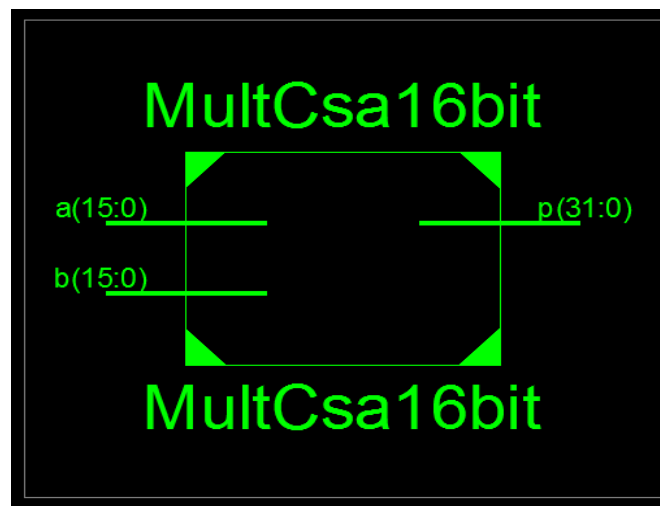


Fig 12: RTL schematic diagram of multiplier using carry select adder

4. The output waveform of multiplier using modified carry select adder

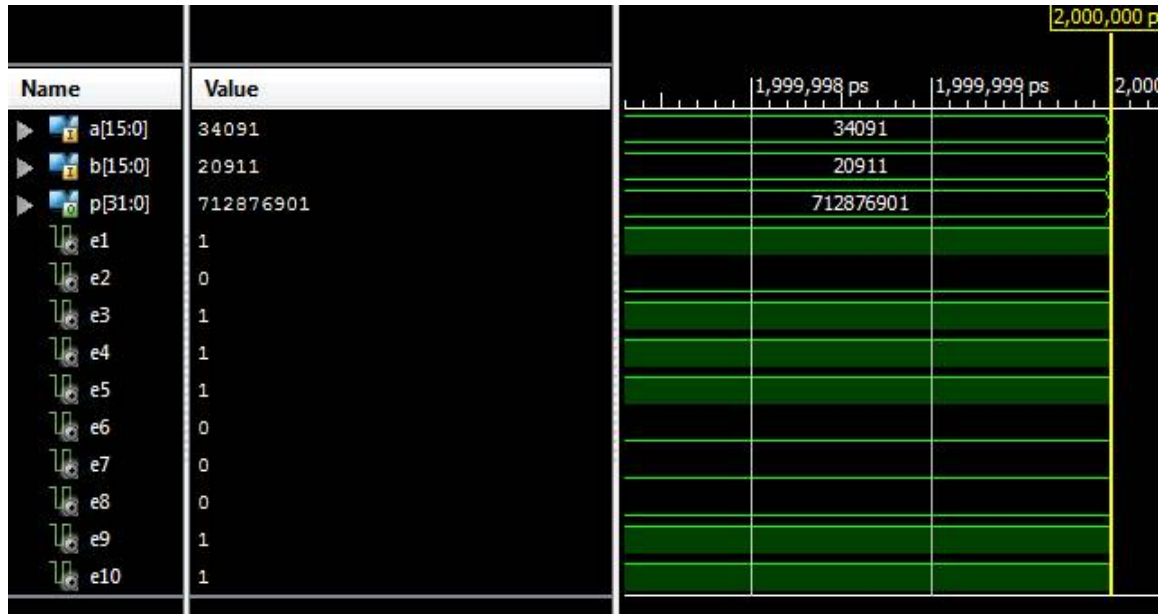


Fig 13: output waveform of multiplier using modified carry select

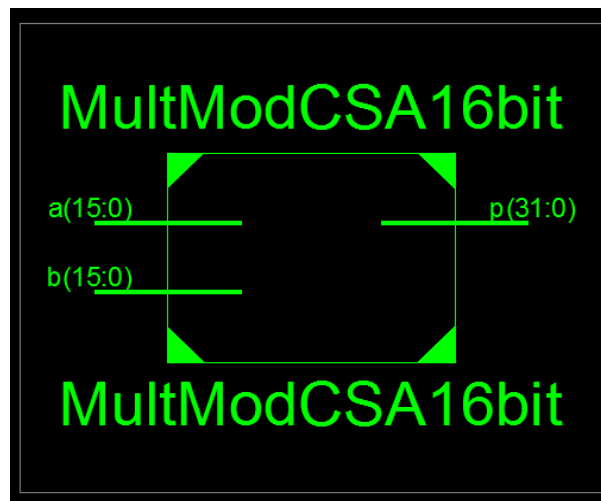


Fig 14 :RTL schematic diagram of multiplier using modified carry select adder

VIII. COMPARISON TABLE FOR MULTIPLIER USING VARIOUS ADDERS

Sl. n	DEVICE USED	SPARTAN 3		SPARTAN 6		VIRTEX 5	
	MULTIPLIERS	DELAY(ns)	NO. OF LUT's	DELAY(ns)	NO: OF LUT's	DELAY(ns)	NO: OF LUT's
1	Multiplier using Ripple Carry Adder	58..817	678	33.501	571	18.873	557
2	Multiplier using Carry look Ahead Adder	58.807	678	32.624	570	19.553	555
3	Multiplier using Carry Select Adder	55.224	708	29.085	566	16.187	556
4	Multiplier using Modified carry select adders	40.589	774	25.587	586	15.536	582

IX. CONCLUSION

The easier solution for improving the speed of carry select adder is the proposed structure. It also found to be consuming less power compare to normal adder design. The proposed carry select adder can be used to speed up the final addition in parallel multiplier circuits and other architectures which uses adder circuits. In multiplier using various fast adders like ripple carry adder, carry lookahead adder, carry select adder, modified carry select adder are analyzed and compared in different devices like **SPARTAN 3** , **SPARTAN 6** , **VIRTEX 5** with respect to speed and area. Multiplier using modified carry select adder is efficient in terms of delay when compared to other fast adder.

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