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Power Quality Alleviation in Distribution Networks with Single DC Link Capacitor based DSTATCOM

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ABSTRACT: This paper proposes a DSTATCOM based on three leg single dc link capacitors for TPFW systems. In this topology, the DSTATCOM is coupled to the line using an interfacing inductor that also functions as a filter. The primary drawback of the single dc link capacitor-based DSTATCOM is the voltage unbalance issue at the front end of the system. The aforementioned voltage unbalance issue is resolved using a neutral inductor. The single dc link capacitors are combined into a single dc link capacitor in this topology to prevent the voltage unbalancing issue that is related to split capacitor-based DSTATCOM. These topologies' simulation study findings are presented.

KEYWORDS: Distribution Static Compensator (DSTATCOM), Voltage Source Inverter (VSI), Hysteresis Band Current Controller (HBCC), Proportional Integral (PI) Controller.

I. INTRODUCTION

Our load systems tend to be unbalanced and non-linear in nature. When these loads are used, an excessive amount of neutral current begins to flow through the neutral conductor. This causes the system to overheat and shortens its lifespan by overloading the neutral conductor and distorting the source currents. On the distribution systems, it will have additional negative effects. DSTATCOM, a compensating device, is employed to prevent such power quality problems. Simply put, DSTATCOM is an inverter that adds reactive power to the line where the load is connected. Reactive power compensation is the usual term for this. Because DSTATCOM is connected parallel to the line and has an interfacing inductor that serves as a filter, it functions essentially as a shunt compensator. DSTATCOM is capable of carrying out tasks like neutral current compensation, power factor correction, harmonic compensation, and load balancing. Load balancing entails producing a balanced sinusoidal source current from a distorted one that results from the use of non-linear loads. Non-linear loads are used, which distorts the source currents. As a result, the neutral current that forms from the difference between the source currents begins to flow through the neutral conductor, overloading it. Additionally, DSTATCOM must be capable of adjusting for the system's neutral current.

The source currents are distorted when non-linear loads are employed. As a result of the source current difference beginning to flow through the neutral conductor as a neutral current, it becomes overloaded. DSTATCOM must also be able to calculate the neutral current of the system. There are many different types of DSTATCOM topologies. It is primarily categorised according to the kinds of control algorithms that are employed and how they are composed structurally. All of the reported DSTATCOM topologies have undergone in-depth analysis. Inverter-based topologies and transformer- or magnetic-based topologies are the two primary categories of DSTATCOM topologies.

A single DC link capacitor is used in the following DSTATCOM topology. This topology is completely explained. To prevent the voltage unbalancing issue associated with the split capacitor-based DSTATCOM, the split capacitor is changed into a single dc link capacitor. In order to account for the neutral current, a second tiny ac capacitor is simultaneously connected between the system neutral and the dc bus negative.

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II. STRUCTURE OF THREE LEG SINGLE DC LINK CAPACITOR BASED DSTATCOM

The three-legged, single-dc-link, capacitor-based DSTATCOM is shown in Figure 2. In this topology, a single dc link capacitor is used in place of split capacitors before the DSTATCOM. A small ac capacitor is simultaneously connected between the negative of the dc bus and the system neutral in order to balance the neutral current. The structural difference between the two topologies is represented by this.

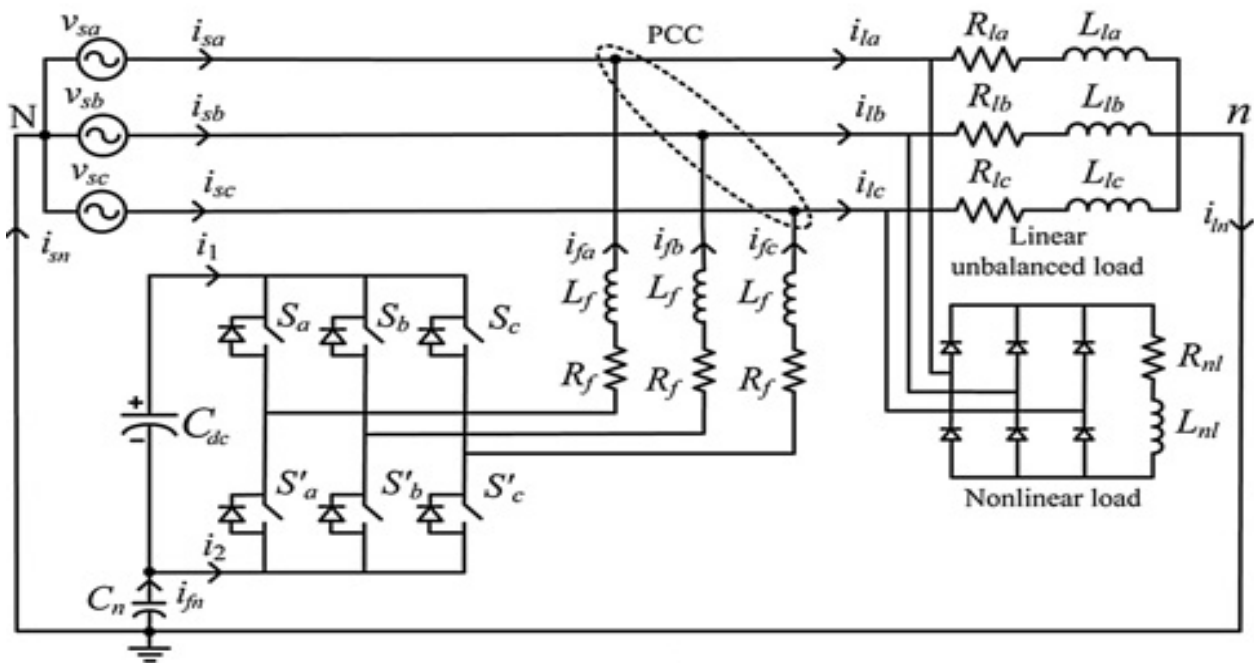


Fig. 1: Three leg single dc link capacitor based DSTATCOM

III. DESIGN OF PROPOSED TOPOLOGY

A. Design of single dc link capacitor based DSTATCOM

The variables to be taken into account are: (i) the neutral capacitor (C_n); (ii) the DC link voltage; (iii) the DC link capacitor; (iv) and the interacting inductance (L_f).

A.1 Neutral Capacitor (C_n)

Phase 'a' filter current and phase 'a' load current must be equalized in order to determine C_n . To balance the load, the filter sends a compensating current into the line, causing the source current to become balanced and sinusoidal.

The load current for 'a' phase is given by,

$$i_{1a} = \frac{V_{sa}}{(R_{1a} + jX_{1a})} \quad (1)$$

The filter current for 'a' phase is given by,

$$i_{fa} = \frac{V_1 - V_{sa}}{R_f + j(X_f - X_{cn})} \quad (2)$$

where, V_{sa} is the phase 'a' source voltage, R_{1a} and X_{1a} is the phase 'a' load resistance and reactance, R_f and X_f is the filter resistance and reactance, V_1 is the fundamental inverter output voltage, X_{cn} is the reactance of neutral capacitor.

By equating the imaginary parts of equations

$$\frac{(V_{sa}X_{1a})}{(R_{1a}^2 + X_{1a}^2)} = \frac{(V_1 - V_{sa})}{R_f^2 + (X_f - X_{cn})^2} (X_f - X_{cn}) \quad (3)$$

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By applying all the known values in equation (7), the value of neutral capacitor (Cn) can be found out.

A.2 DC link voltage (V_{dc})

As mentioned in the split capacitor-based DSTATCOM topology, a dc link voltage of 1.6Vm must be maintained. There is only one dc capacitor used in this topology. Consequently, the capacitor's reference voltage (Vdcref) must be maintained at (2*1.6Vm).

A.3 DC link capacitor (C_{dc})

The DSTATCOM's DC capacitor serves two purposes: (i) steady-state dc voltage maintenance with the least amount of ripple; and (ii) energy storage for the load's reactive and harmonic power.

It is given by,

$$C_{dc} = \frac{2(2X - \frac{X}{2})nT}{(1.8V_m)^2 - (1.4V_m)^2} \quad (4)$$

A.4 Filter inductance (L_f)

It influences (i) switching frequency (ii) rate of change of filter current.

It is given by,

$$L_f = \frac{1.6V_m}{4hF_{max}} \quad (5)$$

where, The maximum switching frequency is Fmax, and the hysteresis band's width is h. For better tracking performance, a suitable hysteresis band (h) must be chosen. The band width is typically chosen to be 5% of the compensator current.

IV. CONTROL ALGORITHM

The following are the steps:

(i). Create the reference filter currents (i*fab) in step By contrasting the reference filter currents (i*fab) with the actual filter currents (ifab), (ii) generate the pulses for VSI switches.

Use PI controllers to maintain the DC link voltage (Vdc) at the desired level (Vdcref).

*Step 1: Generate reference filter currents (i*fab)*

It is created using Instantaneous Symmetrical Component Theory (ISCT). It is written as,

$$i^*_{fa} = i_{la} - \frac{V_{sa} + \beta(V_{sb} - V_{sc})}{\sum_{j=a,b,c} V_{sj}^2} (P_l + P_{loss}) \quad .$$

$$i^*_{fb} = i_{lb} - \frac{V_{sb} + \beta(V_{sc} - V_{sa})}{\sum_{j=a,b,c} V_{sj}^2} (P_l + P_{loss}) \quad (6)$$

$$i^*_{fc} = i_{lc} - \frac{V_{sc} + \beta(V_{sa} - V_{sb})}{\sum_{j=a,b,c} V_{sj}^2} (P_l + P_{loss}) \quad (7)$$

where, (i_{la} , i_{lb} , i_{lc}) represents the three phase load currents, (V_{sa} , V_{sb} , V_{sc}) represents the three phase source voltages, P_l is the average load power, P_{loss} represents the switching and ohmic losses in the actual compensator. $\beta = \frac{\tan \phi}{\sqrt{3}}$. ϕ is the desired phase angle between source voltage and current. In order to obtain unity power factor (UPF), the value of β was chosen as zero.

Average load power (P_l) is given by the equation,

$$P_l = \frac{1}{T} \int_{t_1-T}^{t_1} (V_{sa}i_{la} + V_{sb}i_{lb} + V_{sc}i_{lc}) dt \quad (8)$$

P_{loss} is given by the equation,

$$P_{loss} = K_p e_{vdc} + K_i \int e_{vdc} dt \quad (9)$$

where, $e_{vdc} = V_{dcref} - V_{dc}$. (i.e) the error difference between reference dc link voltage and actual dc link voltage, K_p is the proportional gain, K_i is the integral gain.

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Step 2 : Generate the pulses for VSI switches

The pulses for VSI switches are generated using a Hysteresis Band Current Controller (HBCC) technique. The switching control law states that

(i) If $i_{fa} \geq i_{fa}^* + h$, then bottom switch is turned ON whereas the top switch is turned OFF. ($U_a = 0, \overline{U_a} = 1$).

$\overline{U_a}$ denotes all the VSI top switches.

U_a denotes all the VSI bottom switches.

(ii) If $i_{fa} \leq i_{fa}^* - h$, then bottom switch is turned OFF whereas the top switch is turned ON. ($U_a = 1, \overline{U_a} = 0$).

Only the 'a' phase is covered by the control law previously stated. The final two phases also employ the same control strategy.

The HBCC, where the value of hysteresis bandwidth is set, receives the error value between the three phase actual filter currents (i_{fabc}) and the reference filter currents (i_{fabc}^*). To produce the pulses for the VSI switches, any switching control technique may be used in the HBCC.

Step 3: To maintain the dc link voltage (V_{dc}) at a reference value with the help of PI controller.

The DC link capacitor's voltage is maintained constant by a PI controller. To keep the average dc voltage across the capacitor constant, the average value of dc current through the capacitor must be zero. DC link voltage (v_{dc}) is calculated as follows:

$$V_{dc} = \left(\frac{1}{C_{dc}}\right) \int i_{dc} dt \tag{10}$$

Equation (9) makes it clear that V_{dc} is only maintained constant if i_{dc} is zero. The DC link capacitor's average DC current is represented by the symbol I_{dc} . The small difference between V_{dc} and the reference value V_{dcref} at the end of each cycle causes a small difference between i_{dc} and zero. In order to prevent V_{dc} deviation, a small proportional-integral controller is employed. The PI controller is designed utilising equation (10).

V. SIMULATION RESULTS

The DSTATCOM topology's performance is using the same kind of unbalanced load and non-linear load.

V.A.1 Steady state performance of proposed the DSTATCOM topology.

When it runs in steady state, the load is constant throughout the simulation. The DSTATCOM topologies maintain V_{sabc} , the three phase source voltage.

Table I: System parameters

Parameters	values
	Single DC link capacitor based DSTATCOM
Grid voltage	400 V L-L (rms), 50 Hz
DC capacitor	$C_{dc} = 3300 \mu F$
DC-link voltage	$2V_{dc} = 1040$
Neutral capacitor	$C_n = 10 \text{ mF}$
Interfacing inductor	$L_f = 45 \text{ mH}$
Interfacing resistance	$R_f = 0.5 \Omega$
Hysteresis band	$\pm h = 5\%$ of the compensator current
Voltage controller PI gains	$K_p = 50, K_i = 0.05$

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Linear load	$Z_{1a} = 17.5 + j7.8 \Omega$, $Z_{1b} = 27.5 + j12.5 \Omega$, $Z_{1c} = 37.5 + j31.4 \Omega$
Non-linear load	3 ϕ diode bridge rectifier

V.A.2 Steady state performance of three leg single dc link capacitor based DSTATCOM

The load currents and source currents for single dc link capacitor based DSTATCOM are measured before compensation because the same type of loads are used in both topologies. Additionally shown in Fig. 3 is the single dc link capacitor-based DSTATCOM's steady state performance prior to compensation.

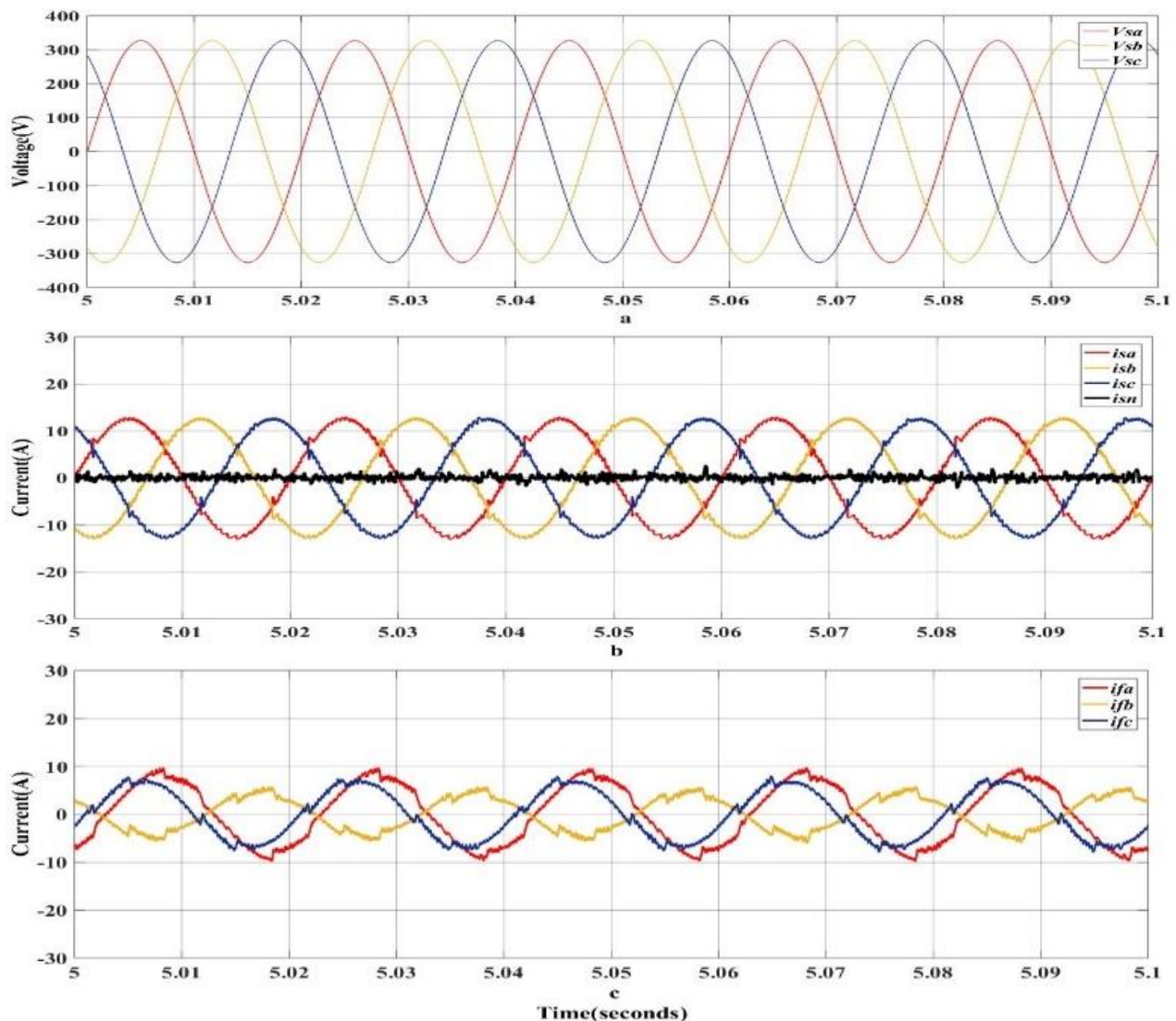


Fig. 2: Steady state performance of single dc link capacitor based DSTATCOM

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- a) source voltages (V_{sabc})
- b) source currents (i_{sabc}) and source neutral current (i_{sn}) after compensation
- c) filter currents (i_{fabc})

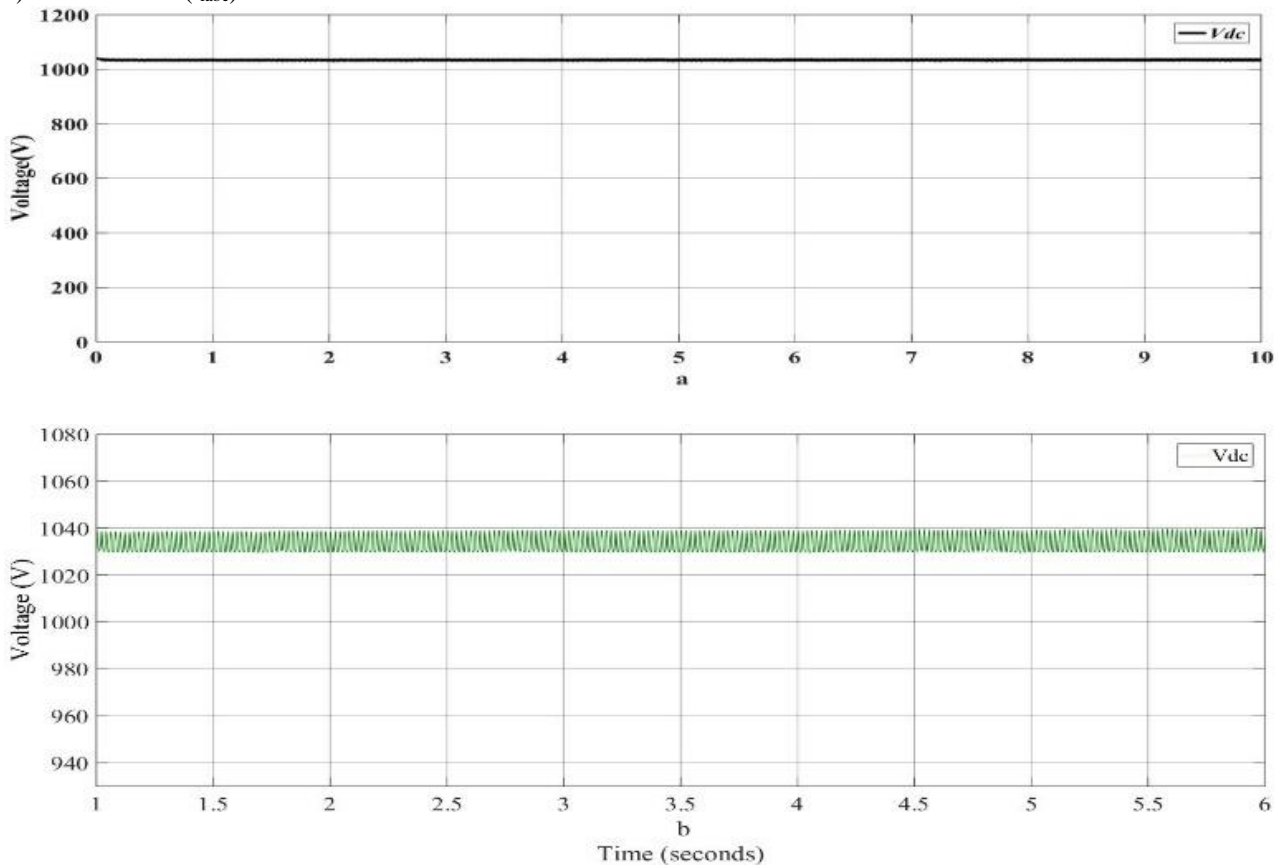


Fig. 3:DC link voltage (V_{dc}) across the dc link capacitor in single dc link capacitor based DSTATCOM

- a) DC link voltage (V_{dc}) across dc link capacitor (C_{dc})
- b) Zoomed view of dc link voltage across dc link capacitor

The voltage across the dc link capacitor (V_{dc}) is kept at 1040 V with the aid of the PI controller. The voltage unbalancing problem with the split capacitor based DSTATCOM topology is not present here because this topology only uses a single dc link capacitor.

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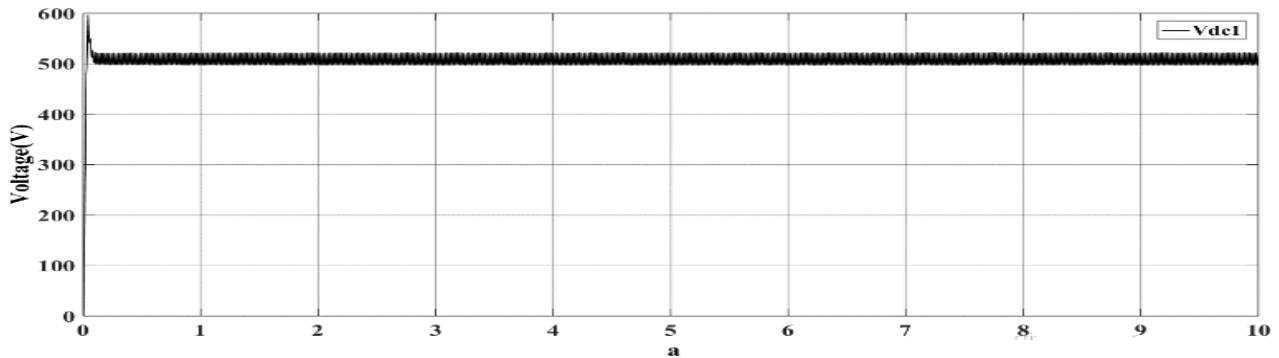


Fig. 4: DC link voltage (Vdc) across the dc link capacitor in single dc link capacitor based DSTATCOM

a) dc link voltage across the first capacitor (V_{dc1})

PI controllers help to maintain the voltage nearly at 520 V. The main drawback of this topology is the voltage unbalance issue. The voltage imbalance is shown in Fig. 4-c. The system's performance will suffer as a result of the increased strain this voltage will put on the VSI switches.

A significant voltage unbalance issue across the capacitors will result from the load having a higher proportion of dc components.

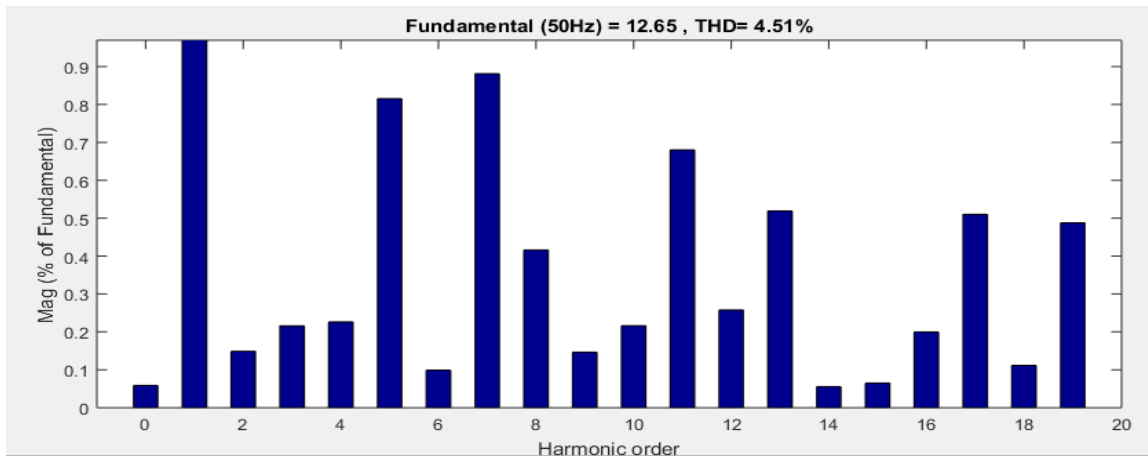


Fig. 5: Harmonic spectrum of phase 'a' in single dc link capacitor based DSTATCOM

VI. CONCLUSION

The effectiveness of the suggested topology for power factor correction, load balancing, harmonic compensation, and neutral current compensation is demonstrated through a number of simulation studies. The split capacitor-based DSTATCOM topology has a lot of dc components and voltage unbalance, which is a big problem. On the plus side, it has a low dc component in source currents, a small ac neutral capacitor to eliminate source neutral current, and no voltage unbalance problems. As a result, split capacitor based DSTATCOM functions well in general.

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