

An ISO 3297: 2007 Certified Organization

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Comparison between Baugh Wooley Multiplier, Array Multiplier and Wallace Tree Multiplier

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ABSTRACT: A multiplier is one of the key hardware blocks in most digital signal processing(DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis. Many current DSP applications are targeted at portable, battery-operated systems, so that the power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operated at a high system clock rate, reducing the delay of multiplier is an essential part of satisfying the overall design. Multiplications are very expensive and it slows the overall operation. The performance of many computational problems are often dominated by the speed at which a multiplication operation can be executed. In this paper, the following three important types of multipliers (Baugh Wooley,Array,Wallace tree) are constructed using different types of adders cells presented in (shalem.R et al (1999)),we then find out the best one in the performance characteristics like power dissipation, speed and area.

KEYWORDS: Multiplication of long bits, Baugh Wooley Multiplier, Array Multiplier and Wallace Tree Multiplier.

I. INTRODUCTION

BAUGH WOOLEY MULTIPLIER:

Baugh Wooley algorithm for the unsigned binary multiplication is based on the concept shown in figure 1. The algorithm specifies that all possible AND terms are created first, and then sent through an array of half-adders and full-adders with the carry-outs chained to the next most significant bit at each level of addition. Negative operands may be multiplied using a Baugh Wooley multiplier.

Charles R.Baugh and Bruce A.Wooley, member of IEEE presents "A Two's complement parallel array multiplication algorithm" in 1973. In this two's complement, m-bit by n-bit parallel array multiplication is described. As multiplication is an essential function in digital system due to its necessity in operation of digital filters and Fourier Transform Processor. This paper presents an algorithm for parallel two's complement multiplication. The advantage of the algorithm is the sign of all the partial products bits are positive, which need for the complement of each multiplier and multiplicand bit.Baugh Wooley algorithm is used in high performance multiplier (HPM) tree, which inherits regular and repeating structure of the array multiplier. Baugh Wooley multiplier exhibits less delay, low power dissipation and the area occupied is also small compared to other array multiplier.



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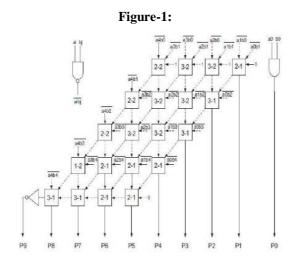
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II. ARRAY MULTIPLIER

The composition of an Array multiplier is as shown in figure 3. There is a one-to-one topological correspondence between this hardware structure. The generation of n partial products requires N*M two bit AND gates. Most of the area of the multiplier is devoted to the adding of n partial products, which requires N-1, M-bit address. The shifting of the partial products for their proper alignment's performed by the routing and does not require any logic. The overall structure can be easily be compacted into rectangle, resulting very efficient layout.

III. WALLACE TREE MULTIPLIER

The partial-sum adders can also be rearranged in a tree like fashion, reducing both the critical path and the number of adder cells needed. The presented structure is called the Wallace Tree structure. It realizes substantial hardware savings for larger multipliers. The propagation delay is reduced. Wallace Tree has the disadvantage of being very irregular, which complicates the task of an efficient layout design.



A=a3 a2 a1 a0

				B=b3 b2 b1 b0				
			1	a3b0	a2b0	a1b0	а0Ъ0	
			a3b1	a2b1	a1b1	a0b1		
		a3b2	a2b2	a1b2	a0b2			
1	a3b3	a2b3	a1b3	a0b3				
p 7	рб	p5	p4	p 3	p2	p1	p0	
E:).								





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Output:

Name	Value	0 ns	1 ns	2 ns	3 ns
🕨 🃑 a[3:0]	1111	0000	0101	1101	1111
🕞 📑 Ь[3:0]	1111	0000	0110	0111	1111
▶ 📑 p[7:0]	11100001	00000000	00011110	01011011	11100001

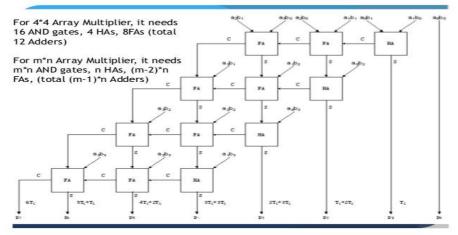
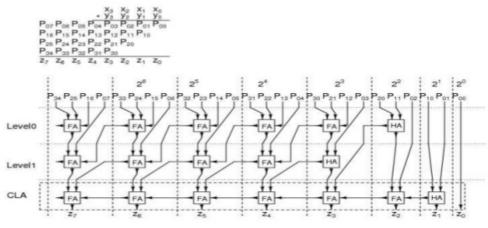


Figure-3:

Output:

Name	Yalue	0 ns	1 ns	2 ns	3 ns
🕨 📑 ×[3:0]	1111	0000	0101	1101	1111
🕨 📑 y[3:0]	1111	0000	0110	0111	1111
🕨 🃑 z[7:0]	11100001	00000000	00011110	01011011	11100001
🕨 🏹 w[39:0]	11111011111011101	0000000000000	0000010001010	0100011001011	1111101111101

Wallace tree multiplier







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Output:

Name	Value	0 ns	1 ns	2 ns	13 ns
🕨 📑 a[3:0]	1111	0000	0101	1101	1111
🕞 📑 Ь[3:0]	1111	0000	0110	0111	1111
▶ 📑 prod[7:0]	11100001	00000000	00011110	01011011	11100001

IV. CONCLUSION

Different parameters obtained from simulation that is useful for determining the efficiency of the multiplier includes power consumed and number of slices used. The delay of each multiplier is also mentioned below. Power Consumption:

- Wallace Tree less
- Baugh Wooley more
- Array most

Number of slices used:

- Wallace Tree 17
- Baugh Wooley 18
- Array 18

Delay:

- Wallace Tree 14.204
- Baugh Wooley 12.340
- Array 13.231

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