

Design of Low Power CMOS Based PTAT/R Circuit for TDC (Temperature-to-Digital Converter) Applications

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ABSTRACT: This paper presents a low power CMOS based PTAT/R circuit design for TDC (Temperature-to-Digital Converter) applications. A BGR (Bandgap reference) circuit is a temperature independent voltage reference circuit broadly used in integrated circuits that provides a fixed (constant) voltage irrespective of variations in power supply, circuit loading from a device and change in temperature. In 45nm CMOS technology, this BGR circuit for low power applications is designed using Cadence software which produces a constant reference voltage. In order to obtain reference voltage constant, two voltages PTAT (Proportional-To-Absolute-Temperature) and CTAT (Complementary-To-Absolute-Temperature) are required, which should have same potential. The characteristics for noise are provided for implemented BGR circuit. The overall circuit of BGR implemented in 45nm technology provides a reasonable area of $10.69\mu\text{m}^2$ and consumes 150.6nW power in the temperature range of -20°C to 100°C and it behaves as a constant voltage source for sensing frontend circuit applications. The sensing frontend circuit along with implemented BGR used in TDC, which is proposed CMOS based PTAT/R circuit consumes $147.1\mu\text{W}$, for ultra low power (ULP) applications.

KEYWORDS: Bandgap reference, voltage reference, PTAT, CTAT, sensing frontend, microwatt, PTAT/R, ultralow-power (ULP).

I. INTRODUCTION

Now a days integrated temperature sensors are used extensively in industries, control systems, instrumentation and measurements. Moreover, a temperature sensor fabricated in IC technology can be combined on a single chip with interface electronics. Therefore, integrated smart sensors have several advantages over conventional smart sensors: direct communication with a microcomputer in a standardized digital format. Thus, minimized system modularity and complexity can be improved for which these are applied. The most recent work on these smart sensors has been performed in industries, laptops and PCs applications. For voltage reference generation, BGRs have been used widely. A BGR is a voltage reference circuit used to provide constant, stable voltage irrespective of supply voltage, variations in temperature, and process parameters. In general, an output voltage nearly 1.25 V (approximately equal to theoretical 1.22 eV (0.195 aJ) silicon band gap at 0 K) is obtained. In 1964, David Hilbiber first published the concept of BGR circuit. Static and dynamic are two types of BGRs. Static BGRs require large area whereas dynamic BGRs designed for reduction of power using switched capacitor circuit. Since static BGR requires more area, the area and cost are considered. This area is due to the presence of the resistors, which suppresses the operating current. Therefore, BGR suffers a tradeoff limitation between area and consumed power.

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This paper provides a design analyses on sensing frontend, which is a TDC design part with an implemented BGR which occupies less area of $10.69\mu\text{m}^2$ and consumes 150.6nW power. Design considerations are described for tradeoff between area and power consumption. Section II discusses the related work. Section III describes the implementation of BGR and section IV discusses the basic PTAT/R circuit and sensing frontend used in TDC. Section V and VI describes replacement with the implemented BGR circuit in existing PTAT/R biasing circuit and their results of simulation respectively. Section VII concludes the paper.

Bandgap references [1] have been widely used in LDO, Buck converters/ Boost converters, ADCs and DACs, any regulators. BGR is used to fix the output voltage and Figure 1 shows the block diagram.

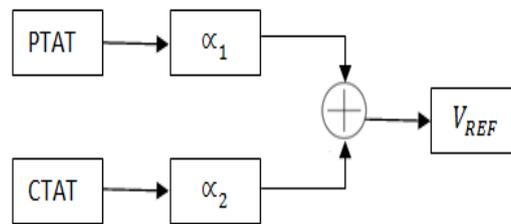


Figure 1. Block diagram for Bandgap Reference Circuit

The equation from the block diagram can be written as:

$$V_{REF} = \alpha_1 V_{PTAT} + \alpha_2 V_{CTAT} \quad (1)$$

For every circuit, required fixed voltage which need to be maintained like in mines/ fridges. Firstly, temperature developed at every stage in any IC, i.e. when an IC is fabricated, initial temperature is different and when internal working in an IC, temperature increases and vary by which V_{REF} changes. But V_{REF} should be constant respective to temperature and supply. Industrial standard of temperature is -40°C to 125°C . Voltage or current (V or I) varies with temperature. If V or I raises with temperature, then this type of voltage or current is said to be proportional-to-absolute temperature (V_{PTAT}) and if it falls with temperature, it is said to be complementary-to-absolute temperature (V_{CTAT}). Voltage is either increasing or decreasing but the voltage is not fixed. So as shown in Figure 2, by cancellation of V_{PTAT} and V_{CTAT} effect, constant voltage is produced.

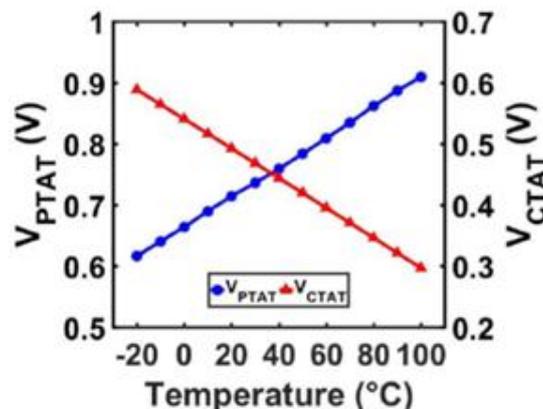


Figure 2. Average of PTAT and CTAT voltage

Sometimes V_{REF} may not be constant, it may vary. To make the voltage constant, two extra values α_1 and α_2 are required. Therefore, $\alpha_1 V_{PTAT} + \alpha_2 V_{CTAT} = \text{constant voltage}$. By adjusting α_1 and α_2 values, a constant voltage is obtained.

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Mathematically, change α_1 and α_2 values to get a fixed voltage. But when coming to circuit design, it is different. The three important factors affect the BGR performance i.e. V_{REF} are supply variation, current through the diode and α_1 and α_2 values.

II. LITERATURE SURVEY

In Reference [1], Byungsub Kim, Senior Member, IEEE, Youngwoo Ji, Jae-Yoon Sim, Senior Member, IEEE and Hong-June Park, Senior Member, IEEE, presented a paper on “A Study on Bandgap Reference Circuit With Leakage-Based PTAT Generation” in which leakage based BGR circuit for ULP (ultralow-power) applications is analyzed in detail. Design considerations for characteristics of noise are obtained. For verification, a test BGR circuit in 0.18- μm CMOS technology is implemented. For resistance reduction to generate CTAT, the BGR uses two voltages of PTAT, so that it alleviates tradeoff limitation between area, cost and power consumption. In Reference [2], T. Hirose, N. Kuroki, Y. Osaki, and M. Numa informed and analyzed on 1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V sub BGR circuits for nanowatt CMOS LSIs and deals with BGR and sub-BGR circuits, used for nanowatt LSIs. The proposed circuits neglect the usage of resistors and has only one BJT and MOSFETs. For BGR and sub-BGR circuits, power dissipations are obtained. In Reference [3], J. Mu, L. Liu, Z. Zhu, and Y. Yang analyzed and gave information on a 58-ppm/ $^{\circ}\text{C}$ 40-nW BGR at supply from 0.5 V for energy harvesting IoT devices, gives 0.24V output reference low supply voltage reference minimizes power consumption of the whole circuit and harvester efficiency enhancement is done. The PNP transistor V_{BE} is divided by switch capacitor circuit that is presented to obtain reference of low output using PTAT circuit without resistor. The proposed BGR implemented in a 0.18 μm technology which occupies an area of 0.058mm².

III. IMPLEMENTATION OF BGR

To implement a BGR circuit which produces constant voltage, PTAT voltage and CTAT voltages, two approaches [1] needed to be combined. They are namely, conventional approach of BGR and a BGR with a leakage based PTAT voltage generator that produces output as CTAT (complementary-to-absolute temperature) and PTAT (proportional-to-absolute temperature) respectively. This BGR as shown in Figure 3 requires two PTAT voltages V_{PTAT1} and V_{PTAT2} [5]. No startup circuit is needed to implement this BGR circuit. Since both reference of voltage and current are obtained, it is said to be CMOS current reference circuit. By placing a resistor between V_{PTAT1} and V_{PTAT2} [5], it gives I_{REF} (current reference). By stacking a CTAT voltage which is provided by Q_1 with a pn-diode on V_{PTAT1} , V_{REF} (voltage reference) can be obtained.

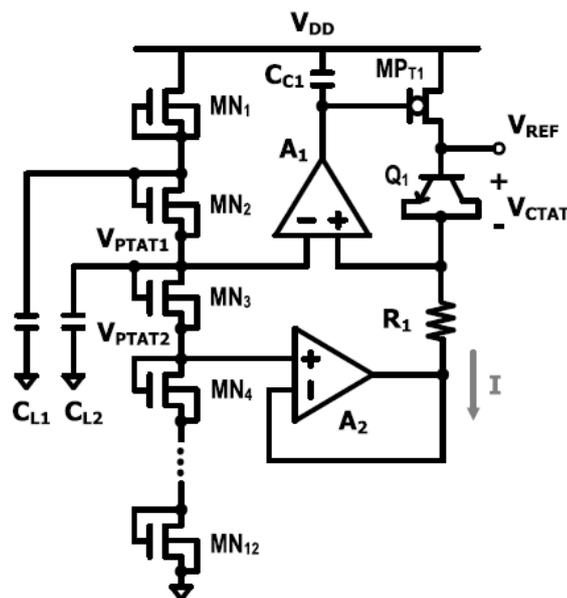


Figure 3. Design of Overall BGR circuit

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PTAT voltage present in the BGR is independent of resistor R_1 and R_1 varies according to current change. CTAT voltage is a logarithmic function of temperature, current or process. These three parameters effect the CTAT voltage. V_{PTAT2} is decreased by a factor of slope $mV_T \ln \alpha$ using amplifier based PTAT generator. When the supply is given, all the transistors work in subthreshold region. The subthreshold current is given by,

$$I_{sub} = \mu C_{OX} \frac{W}{L} (m - 1) V_T^2 e^{\frac{|V_{GS}| - |V_{th}| + \eta |V_{DS}|}{m V_T}} \quad (2)$$

Where, I_{sub} is the subthreshold current, C_{OX} is the oxide capacitance, m is the subthreshold factor, V_T is the thermal voltage, and V_{th} is the threshold voltage. Since the PTAT generator [5], A1 and A2 dissipates power which is negligible, so that consumption of whole current dominates by the current passing through R_1 resistor. The current equation is given by,

$$I = \left(\frac{V_{PTAT1} - V_{PTAT2}}{R_1} \right) = \frac{m V_T \ln M}{R_1} \quad (3)$$

Where,

$$V_{PTAT1} = K m V_T \ln M \quad (4)$$

$$V_{PTAT2} = (K - 1) m V_T \ln M \quad (5)$$

The V_{REF} is obtained as the summation of voltages of CTAT and PTAT. Therefore, the V_{REF} can be obtained by,

$$V_{REF} = V_{CTAT} + K m V_T \ln M \quad (6)$$

Where, M is ratio of the size between M_1 (pull-up) and M_2 (pull-down) transistors. Figure 4 indicates the characteristics for noise that have been simulated for the BGR circuit. The consumed power for this BGR implementation is 150.6nW. The layout is illustrated for the implemented BGR to see how much area is occupied by this BGR. Therefore, the area is calculated and it occupied $10.69 \mu m^2$.

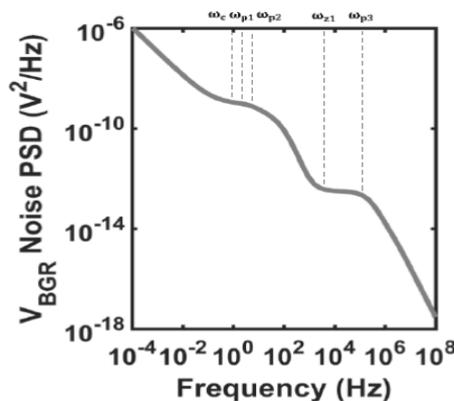


Figure 4. Noise characteristics of the implemented BGR

This BGR implementation is compared with the previous BGR works and compared parameters are tabulated as shown in the Table I. The comparison table is shown below compares the performance with the previous works of existing BGR circuits in [2], [3], [4], [5]. The less power consumption is achieved here for this BGR is 150.6nW, when previous works are compared from $-20^\circ C$ to $100^\circ C$ of temperature range. The area calculated for the BGR circuit is $10.69 \mu m^2$.

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Table I
Comparison for previous BGRs performance

	This project	[2] (a)	[3]	[4]	[5]	[2] (b)
Technology (μm)	0.045	0.045	0.045	0.045	0.045	0.045
Minimum V_{DD} (V)	0.45	0.45	0.45	0.45	0.45	0.45
Supply Voltage(V_{DD})	1.5	1.8	1.7	1.6	1.8	1.8
Power (nW)	150.6	3620	1792	547.4	6275	1086
Type	BGR	BGR	BGR	BGR	BGR	Sub-BGR
Output Voltage(V)	1.49	1.66	1.52	1.49	1.78	1.53
Temperature Range ($^{\circ}\text{C}$)	-20~100	-20~100	-20~100	-20~100	-20~100	-20~100
Active Area(μm^2)	10.69	-	-	-	-	-

This chapter concludes that an overall BGR implemented by combining the mentioned two approaches which produces PTAT and CTAT voltage and mainly a fixed output voltage.

IV. SENSING FRONTEND DESIGN USING PTAT/R CIRCUIT

The basic PTAT/R circuit used in the sensing frontend design is discussed here for TDC (Temperature-to-Digital Converter) applications. This section discusses the design of Temperature-to-Digital Converter's (TDC's) temperature sensing frontend. And for this sensing frontend shown in Figure 5, other circuits required to interface various types of sensors to an ADC, antenna or microcontroller.

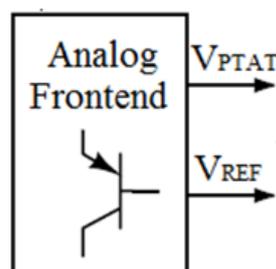


Figure 5. Block diagram of a sensing frontend

In Figure 6, a PTAT/R biasing circuit that is shown is a sensing frontend design, generating a PTAT current. And also current generated that is supply independent, the accuracy of V_{BE} can be improved. This PTAT/R biasing circuit contains two PNP to operate at a ratio of 1: p_{Eb} (emitter-current ratio). In the biasing circuit, the amplifier forces both transistors corresponding difference voltage ΔV_{BEb} across R_b (biasing resistor) that generates biasing current ($I_b = \Delta V_{BEb} / R_b$). At the biasing circuit, then current mirror copies the biasing current 1 : m to the bipolar core. After copying 1: m , this bipolar core operates similar to PNP-based TDC [6] and its output is obtained at the nodes of V_{BE1} and V_{BE2} . The difference of both V_{BE} s gives PTAT voltage. By taking finite current gain β , and an equivalent resistance of an emitter r_s , the equations of V_{BE} and ΔV_{BE} can be written as:

$$V_{BE} \approx \frac{kT}{q} \cdot \ln\left(\frac{p_E \cdot I_E}{I_S}\right) + \frac{kT}{q} \cdot \ln\left(\frac{\beta}{\beta+1}\right) + p_E \cdot r_s \cdot I_E \quad (7)$$

$$\Delta V_{BE} \approx \frac{kT}{q} \cdot \ln(p_E) + \frac{kT}{q} \cdot \left(\frac{\Delta\beta}{\beta \cdot (\beta+1)}\right) + r_s \cdot (p_E - 1) \cdot I_E \quad (8)$$

Various methods have been used in the previous TDC designs [7]–[8], [9]–[11], to minimize the effects of spread in the various terms in (7) and (8). Selecting biasing current (I_E) as small, alleviates the r_s effect (last terms in (7) and (8)) and its variation.

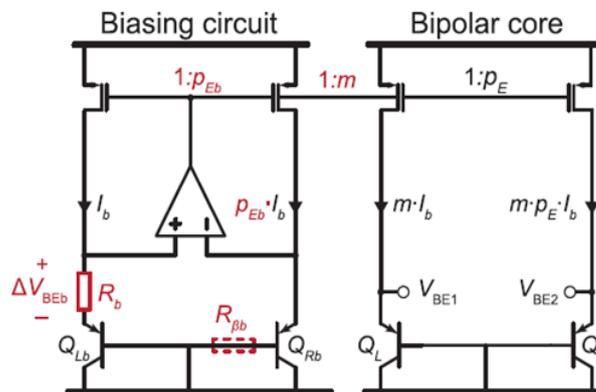


Figure 6. PTAT/R Biasing Circuit

Using a β -compensating biasing current [7], [8] effectively suppresses the β effect on V_{BE} (the second term in (7)). As shown in Figure 6, this can be designed by taking $R_{\beta b}$ (β -compensating resistor) in PTAT/R biasing circuit [12]. This proposal, therefore limited by PNP mismatch.

V. PROPOSED CMOS BASED PTAT/R CIRCUIT

Some methods are introduced to alleviate error sources for the biasing circuit to a quality level. This is the newly proposed method of placing the implemented BGR in the PTAT/R biasing circuit leads to less power consumption that provides V_{REF} and V_{PTAT} . Figure 7 shows PTAT/R circuit after placing existing BGR circuit in place of biasing circuit. This is the proposed PTAT/R circuit which produces fixed reference voltage and ΔV_{BE} . Reference voltage is obtained from existing BGR at output node of V_{REF} .

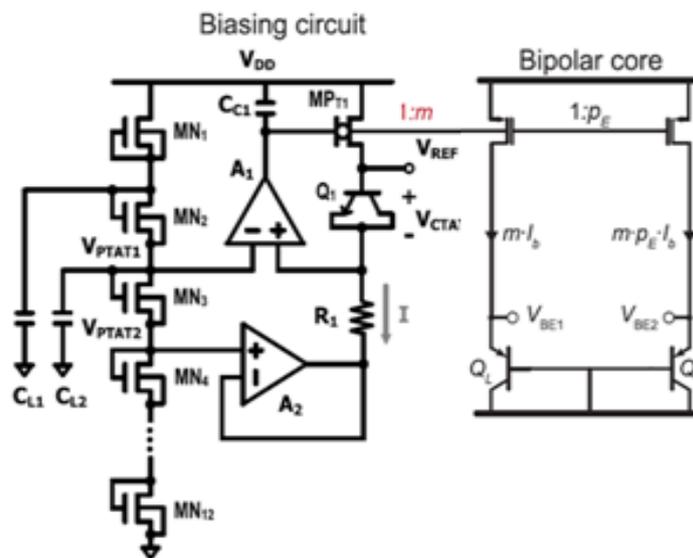


Figure 7. PTAT/R circuit after placing the implemented BGR

This circuit operates similarly to the PTAT/R biasing circuit. The MP_{T1} transistor then copies $1:m$ to the bipolar core in which current passing through these branches in the ratio of $1:p_E$ to both transistors Q_L and Q_R respectively. The output is produced at two nodes V_{BE1} and V_{BE2} for which their difference ΔV_{BE} is the output of PTAT. Therefore, in order to design CMOS based PTAT/R circuit, a sensing frontend is designed which can be used for TDC applications.

VI. SIMULATION RESULTS

Implemented in a 45nm CMOS technology, Figure 8 shows the noise produced for the overall existing BGR circuit is shown in the below graph plotted between noise PSD and frequency. The calculated power consumed for this BGR is 150.6nW and it occupies $10.69\mu m^2$ which is a reasonable area. Figure 9 shows the layout designed for implemented BGR circuit in 45nm layout λ -based rules using Virtuoso L-edit for which DRC and LVS is done using Assura. The area calculated from this layout by the multiplication of length and width.

$$\begin{aligned} \text{Area} &= \text{Length} \times \text{Width} \\ &= 6.5 \mu m \times 1.645 \mu m = 10.69 \mu m^2 \end{aligned}$$

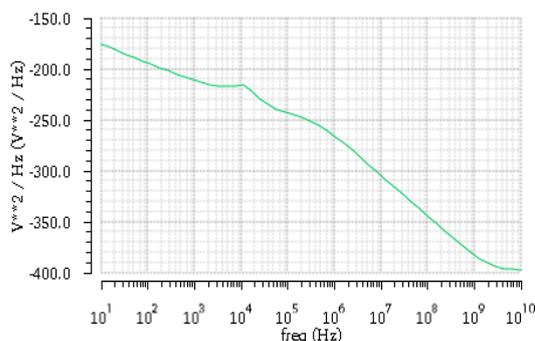


Figure 8. Noise characteristics for implemented BGR

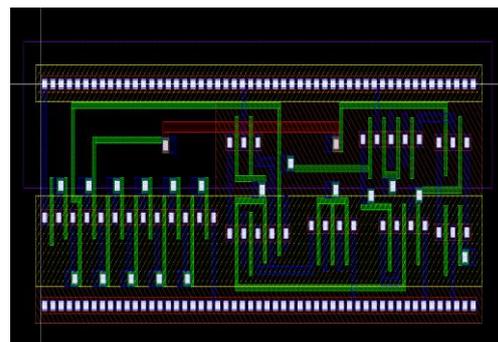


Figure 9. Layout for the implemented BGR

Practically, the designed BGR produces desired output as constant reference voltage with which both PTAT and CTAT voltages are also obtained as shown in Figure 10. And mathematically these three voltages that are plotted in the shown graph Figure 11. The PTAT and CTAT values are scaled accordingly to obtain a fixed reference voltage.

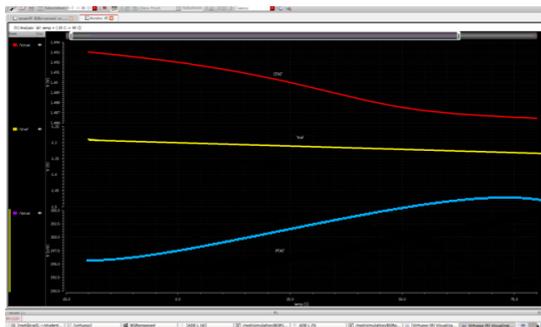


Figure 10. Implemented BGR output

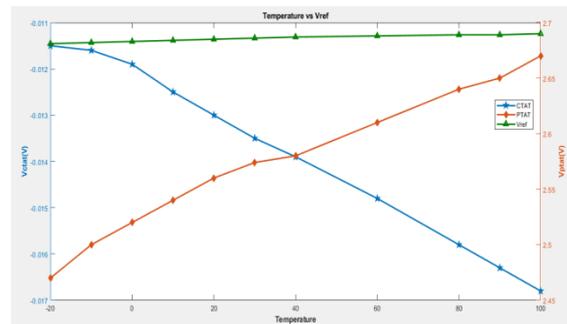


Figure 11. Mathematical Plot between V_{CTAT} , V_{REF} , V_{PTAT} and temperature for implemented BGR

Figure 12 indicates the Plot between ΔV_{BE} and temperature for a PTAT/R Circuit producing the PTAT voltage. The power consumed for this circuit is of $286.7\mu\text{W}$. Figure 13 shows when the biasing circuit is replaced with the designed BGR, then both reference voltage and PTAT voltage are produced at the output nodes. The power consumed for this circuit is $257.1\mu\text{W}$.

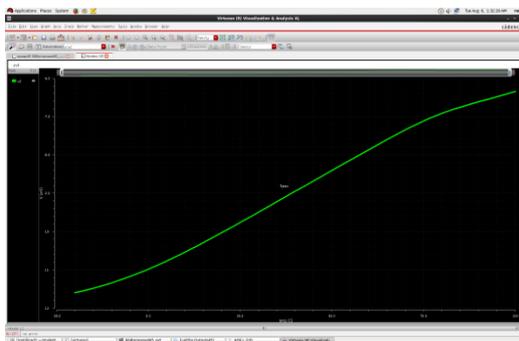


Figure 12. Output of the PTAT/R biasing circuit

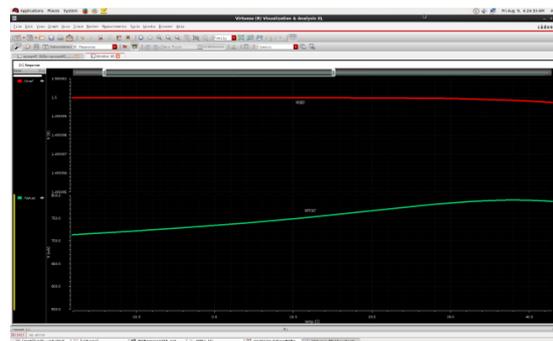


Figure 13. Plot between V_{REF} , V_{PTAT} and temperature

The power consumption further reduced when BJTs are replaced with CMOS transistors. Previously, the power consumed for existing PTAT/R circuit is $257.1\mu\text{W}$ whereas for this proposed CMOS based PTAT/R circuit the power is minimized to $147.1\mu\text{W}$, which can be used for ULP applications.

VII. CONCLUSION

This paper presents the design of low power CMOS based PTAT/R circuit for TDC applications that produces both V_{PTAT} (PTAT voltage) and V_{REF} (reference voltage). The BGR circuit is independent of temperature and supply voltage for low power applications is designed using Virtuoso S-edit (Schematic editor) in 45nm CMOS technology in Cadence software. The design of low-power BGR with a reasonable area and cost has been in the achievement of high temperature reliance on PTAT to compensate for that of CTAT is the main complication. The flow of only leakage current when adopted stacked MOSFETs is done without PTAT resistor-based multiplication. The implemented BGR in 45nm CMOS technology for which layout is illustrated using Virtuoso L-edit (Layout editor) in which DRC (Design Rule Check) and LVS (Layout Versus Schematic) are done, achieves a reasonable low area of $10.69\mu\text{m}^2$. The consumed power for this implemented BGR

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circuit is 150.6nW of low power when compared to previous works in the temperature range of -20°C to 100°C and it behaves as constant voltage source used for sensing frontend circuit applications. In this 45nm technology, power consumption for the existing PTAT/R biasing circuit is $286.7\mu\text{W}$. But the proposed CMOS based PTAT/R circuit used in TDC has been designed by placing implemented BGR in PTAT/R biasing circuit, the power consumption now reduces to $275.1\mu\text{W}$ and when BJTs are replaced with MOSFETs, this proposed PTAT/R circuit achieves low power of $147.1\mu\text{W}$. So this paper concludes that the designed BGR occupies low area and when placed into the PTAT/R biasing circuit, the proposed CMOS based PTAT/R circuit produces low power, which can be further used for ultra low power applications.

FUTURE WORK

Both V_{PTAT} (PTAT voltage) and V_{REF} (reference voltage) are obtained at output of sensing front end which can be given to ADC (analog to digital converter) and this temperature output when given to digital interface, then an integrated temperature sensor can be designed.

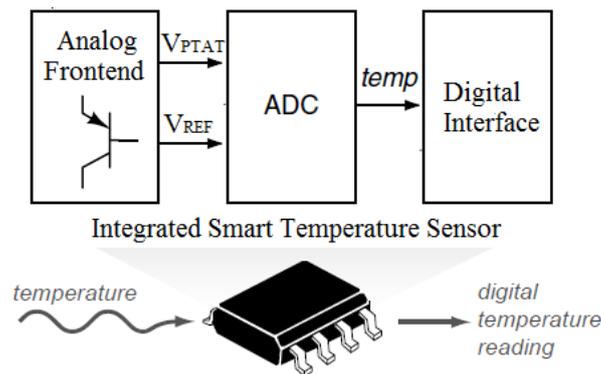


Figure 14. Block diagram of an integrated smart temperature sensor

Since integrated temperature sensors [7] extensively used in industries, control systems, instrumentation, measurements, etc. Moreover, a temperature sensor fabricated in IC technology can be merged with interface electronics on a single chip. Thus, minimized system complexity and modularity can be improved for which these are applied.

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