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An Area Efficient VLSI Design of Phase Measurement System for FPGA

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ABSTRACT: Phase measurement is required in electronic applications where a synchronous relationship between the signals needs to be preserved. Traditional electronic systems used for time measurement are designed using a classical mixed-signal approach. These cause uncertainty of phase relationship between the recovered signals. To address the need to register minute phase shift changes inside an FPGA, we propose a design for phase measurement logic core having resolution and precision in the range of a few pico seconds. The working principle is based on subsample accumulation using systematic sampling over the phase detector signal. The phase measurement logic can operate over a wide range of digital clock frequencies, ranging from a few kilohertz to the maximum frequency that is supported within the FPGA fabric. A mathematical model is developed to illustrate the operating principle of the design. We also discussed the procedure of the phase measurement system, This Proposed System Implemented using Verilog HDL and Simulated by Model sim 6.4 c and Synthesized by Xilinx tool. The proposed system implemented in FPGA Spartan 3 XC3S 200 TQ-144.

KEYWORDS: Modelsim, FPGA, Phase measurements, Verilog HDL, Phase detectors.

I. INTRODUCTION

Experiments use phase information to calibrate and synchronize signals between different circuit elements. In recent trend for compact implementation of full digital architectures, reconfigurable hardware technologies such as field-programmable gate arrays (FPGAs) play a very dominant role. It is essential that the latency critical protocols maintain constant phase differences in the recovered signals for the entire experiment's runtime. A logic design for phase monitoring capability to register phase shift changes in the range of 20–100 ps is needed inside the FPGA circuitry. This would allow to extract the relative phase information and to recalibrate the system when needed, to maintain the constant phase relationships.

It use phase information to calibrate and synchronize signals between different circuit elements. In certain experiments such as in high energy physics (HEP), preservation of phase relationship between critical signals throughout the experiment runtime is a necessary condition. In recent trend for compact implementation of full digital architectures, reconfigurable hardware technologies such as field-programmable gate arrays (FPGAs) play a very dominant role. Popular latency critical communication link standards used in HEP experiments such as gigabit transceiver and timing-trigger and control system over passive optical network technology are implemented in FPGAs directly. It is essential that the latency critical protocols maintain constant phase differences in the recovered signals for the entire experiment's runtime.

In this paper, we present a new approach for an accurate phase measurement in an FPGA using subsamples collected by the systematic sampling over XOR-based phase detector (PD) signal. The XOR-based PD introduces the least timing jitter because of the simplicity of its design.. A mathematical model is formulated to explain the operating principle of the phase measurement technique. The proposed technique is suitable to construct a logic core for relative

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phase measurement between clocks having very low to very high frequencies with precision, accuracy, and resolution in the range of a few picoseconds. The analysis and comparison developed here have been carried out in terms of speed, power consumption and power-delay product (PDP). The investigation, which also includes the most interesting recently proposed one-bit full adders, has been based on simulation runs on a modelsim environment.

II. LOGIC DESIGN

A) FIELD-PROGRAMMABLE GATE ARRAY (FPGA)

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform.

The ability to update the functionality after shipping, partial re-configuration of the portion of the design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications. In addition to digital functions, some FPGAs have analog features. The most common analog feature is programmable slew rate and drive strength on each output pin, allowing the engineer to set slow rates on lightly loaded pins that would otherwise ring unacceptably, and to set stronger, faster rates on heavily loaded pins on high-speed channels that would otherwise run too slow. Another relatively common analog feature is differential comparators on input pins designed to be connected to differential signaling channels. A few "mixed signal FPGAs" have integrated peripheral Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) with analog signal conditioning blocks allowing them to operate as a system-on-a-chip. Such devices blur the line between an FPGA, which carries digital ones and zeros on its internal.

B) Field-Programmable Device (FPD)

A general term that refers to any type of integrated circuit used for implementing digital hardware, where the chip can be configured by the end user to realize different designs. Programming of such a device often involves placing the chip into a special programming unit, but some chips can also be configured "in-system". Another name for FPDs is programmable logic devices (PLDs); although PLDs encompass the same types of chips as FPDs, we prefer the term FPD because historically the word PLD has referred to relatively simple types of devices.

C) Programmable Logic Array (PLA)

A Programmable Logic Array (PLA) is a relatively small FPD that contains two levels of logic, an AND-plane and an OR-plane, where both levels are programmable (note: although PLA structures are sometimes embedded into full-custom chips, we refer here only to those PLAs that are provided as separate integrated circuits and are user-programmable

D) Programmable Array Logic (PAL)

A programmable logic array is a kind of programmable logic device used to implement combinational logic circuits. The PLA has a set of programmable AND gate planes, which can then be conditionally complemented to produce an output. We present a new approach for an accurate phase measurement in an FPGA using subsamples collected by the systematic sampling over XOR-based phase detector (PD) signal. The XOR-based PD introduces the least timing jitter because of the simplicity of its design.

III. EXISTING METHOD

In many applications discrete phase detectors circuits are used to measure phases between different synchronous, usually high-speed, clocks. These phase detector circuits often output analog voltages that also require ADCs to be implemented in the system, adding more complexity and cost to the design. If a system also contains an FPGA with many available I/Os it would be desirable to use the FPGA as a phase detector for a cost efficient solution with simpler

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PCB design. The European XFEL timing system utilizes external phase detectors for high accuracy phase measurements on several high-speed signals. However, it may also be required to measure the phases of other clock signals and to do this in the FPGA that sits on the board. Therefore a simple FPGA based phase detector has been developed. The basic architecture of the phase detector is very simple and yet with proper considerations very accurate. A simulation tool has been developed for very realistic estimation of the performance under different conditions. The phase detection has also been verified using real hardware.

The principle sounds simple it still involves many design challenges. First of all a very stable sampling frequency is essential for optimal measurement performance. If the phase or frequency of the sampling clock is not relatively constant during measurement, the scanning of the two high-speed clocks gets distorted and could degrade the accuracy. The power supply is FPGA Based Phase Detector for High-Speed Clocks with Pico-Seconds Resolution .The principle of operation is that the high-speed clocks are sampled with an independent clock, with a lower frequency will eventually scan through the entire period of the high-speed clock. Slow DFF High-Speed DFF Low- Speed another crucial part that needs proper design.

Any disturbance on the power distribution, like noise from the DC/DC converters, could change the propagation delays in active components like the FPGA. When it comes to phase measurements this is critical because it will affect the scanning of the clock period. However, if the two measured high-speed clocks are very stable for a relatively long time it would be enough to just increase the number of samples. Eventually any noise would disappear from the measurement if the sampling is continued long enough time. This is not an optimal solution though since the measurement should converge to an accurate result as fast as possible. Therefore it is desirable to calculate the exact frequency ratio between the high-speed clocks and the sampling clock, so that the sampling clock will sweep through the high-speed clock an even number of times. The calculation of optimum sampling time vs. phase resolution and accuracy is presenting another. It is important to verify the simulation tool against a real hardware implementation, with known environment parameters, to justify the simulated results. For that purpose two phase shifted clocks, generated by a PLL inside the FPGA, was used together with the implemented phase detector. In this experiment both Xilinx has been used together with Chip Scope for communication with the phase detector. Evaluating different parameters in hardware is difficult on the other hand, simply because generation of arbitrary jitter on the clocks cannot be easily achieved.

Measurements with the phase detector in the real FPGA, with 50 MHz high-speed clocks, 33.333 MHz sampling clock and 330000 samples per measurements, indicates a time resolution of 2.4 ps. At 33000 samples the time resolution is about 8.1 ps. This is consistent with the simulation, which validate the results of the simulation tool. The simulation tool takes almost every parameter into account to give a very realistic result. Most importantly, the simulation tool confirms that the design works well, with good accuracy and linearity.

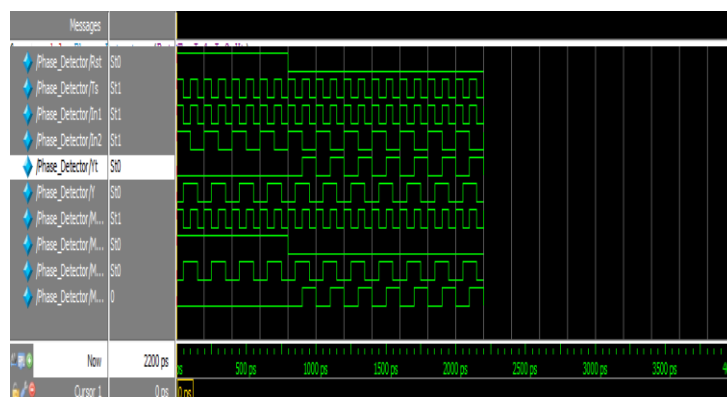


Fig.1 Existing Synchronizer output

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IV. DISADVANTAGES

- This simple FPGA based phase detector requires absolutely no special components, like an external or internal PLL, and can be used on high speed- clocks with frequencies up to the limit of the I/O ports.
- It only uses one additional independent clock, which is used to scan the high- speed clocks.

V. PROPOSED METHOD

PROPOSED SYSTEM OF PHASE MEASUREMENT

- We present a new approach for an accurate phase measurement in an FPGA using subsamples collected by the systematic sampling over XOR-based phase detector (PD) signal.
- The XOR-based PD introduces the least timing jitter because of the simplicity of its design.
- It is known that use of sub sampling technique causes spectral leakage.
- However, in our application, the use of averaging method for the phase measurement makes it less susceptible to interfere with the results. The proposed technique is suitable to construct a logic core for relative phase measurement between clocks having very low to very high frequencies with precision, accuracy, and resolution in the range of a few picoseconds.

A) TEMPERATURE AND VOLTAGE STABILITY OF THE PROPOSED SYSTEM

The temperature stability of the proposed phase difference measurement system is tested on the evaluation board. The temperature tests are performed with the use of a thermal chamber. A constant phase difference (5 ns) is measured under different temperature, with a range of 15 °C~55 °C. Measurement under a temperature is repeated 50 times. The measurement error (mean of absolute value) under different temperature is shown in Figure 8. In the figure, the largest variation in the measurement result is 5 ps. The voltage tests are performed using the DC power supply RIGOL DP832A. The nominal operating voltage of the evaluation board is 1 V (internal supply voltage of FPGA). In the tests, the supply voltage of the FPGA is changed within the range of 0.95 V~1.05 V with a step of 5 mV. A constant phase difference (5 ns) is measured under different supply voltages at an ambient temperature of approximately 25 °C. Each measurement at a given voltage is also repeated 50 times. The measurement error is shown in Figure 9, which indicates that with the change in supply voltage, the largest difference in the measurement error is less than 3.5 ps.

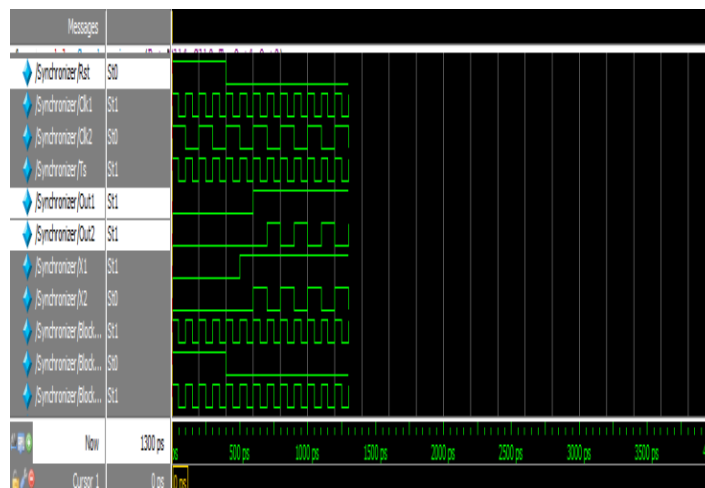


Fig.2 Existing Phase detector output

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B) MEASUREMENT ERROR

The phase calculator, like any other instrumentation technique, is subjected to certain kinds of errors. This can be listed as follows. It occurs due to clock skew $t_{skew(m)}$ between CLK1 and CLK2. The clock skew 2θ is minimized by setting proper timing constraints to instruct the fitter place and route engine to do more robust timing closure for defined paths 21 , and prevents variation of clock skew by large margin with each firmware upgrade. It occurs due to bank skew $t_{skew(p)}$ between PD block and polarity detector block. Bank skew 2θ is a type of skew that refers to the output skew between the signals with a single driving input terminal. Here, $t_{skew(p)} = \{t_{CLK1} - t_{CLK1*}\} - \{t_{CLK2} - t_{CLK2*}\}$.

Our phase estimation logic is a typical mid-tread uniform quantizer. The quantization step is equal to the sampling interval T_s and the input-output relationship for the forward quantization step is expressed as $y_k = k.T_s$. In some applications, the FIR filter circuit must be capable to operate at high sample rates.

While in other applications, the FIR filter circuit must be a low power circuit operating at moderate sample rates. FIR filters design implementation consist a large number of multiplications, which leads to excessive area and power consumption. So, the topology of the multiplier circuit also affects the resultant power consumption. Many works have focused on development to optimizing multiplications by decomposing them into simple operations such as addition, subtraction and shift or sharing common sub-expressions using different methods. Various multiplier structures and algorithms i.e. combinational, serial, add and shift and modified booth are used for FIR filters which define the consumption of resource, and its performance.

In this work, booth radix-8 multiplier is used in FIR filter and its effects on power and speed is analyzed. In this paper, we propose a fixed-latency serial transceiver based on dynamic clock phase shifting and changeable delay tuning technologies. Our solution can process all possible phase offsets between the transmitted and received clocks, so it relaxes the requirement of fanning in the same reference clock both to the transmitter and to the receiver. It also eliminates the reset- relock process in the roulette approach. The experiment results indicate that our transceiver can achieve a deterministic latency with sub-nanosecond precision. Eventually any noise would disappear from the measurement if the sampling is continued long enough time. It needs a calibration procedure to eliminate the offset due to random systematic effect. Phase measurement between clocks having very low high frequencies with precision, accuracy, and resolution in the range of a few picosecond.

Synchronizer will be form by Four D Flip flops and with Clk1, Clk2, and Sampling Clock. The sampling of CLK1 and CLK2 with SAMPLE CLK involves asynchronous clock domain crossing that can give rise to metastable output. Hence, synchronization register chain or synchronizer is used for metastable signal to settle down.

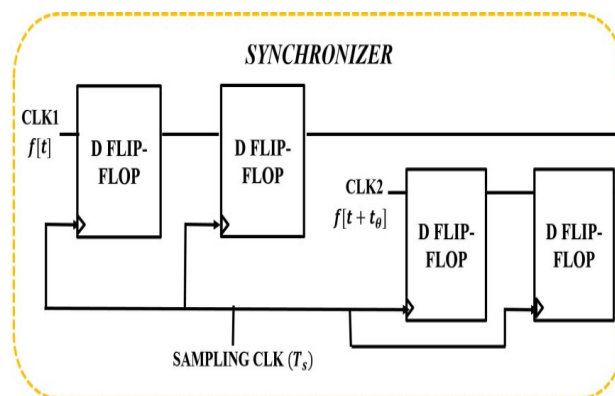


Fig.3 Synchronizer

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PHASE DETECTOR

An accurate phase measurement in an FPGA using subsamples collected by the systematic sampling over XOR- based phase detector (PD) signal. The XOR-based PD introduces the least timing jitter because of the simplicity of its design.

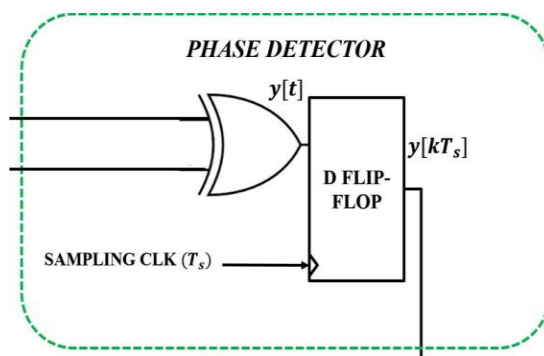


Fig.4 Phase Detector PHASE POLARITY DETECTION UNIT

It's Contains with D Flip flop and Bank Skew Operation. Dynamic phase shift method is used to detect the amount of bank skew correction needed to compensate for phase polarity offset Bank skew cancellation delay = $-t_{skew}(p)$ the effect of phase polarity offset is corrected by adding bank skew cancellation as indicated in Fig. to get linear response characteristics. In our test case, we have used -250 -ps bank skew cancellation.

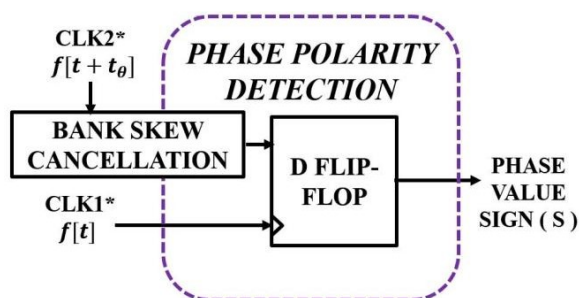


Fig.5 Phase Detector using DFF PHASE VALUE COMPUTATION UNIT

This Module Contains Registers, Multiplexers, Adders, Subtractors, Right Shift Operators and Comparators. The number of blank bits padded must be of equivalent size as divisor β . This method of successive approximation of phase value computation is illustrated in Fig. 3. The final phase value in our study, is stored in a 64-b register in little-endian format and represented in binary fractional form as

$\theta = (-1)^{\text{sign}} \times \sim \theta \times 2^{-32}$ ADDERS & SUBTRACTORS

Subtraction of binary numbers can be carried out by using the addition of 2's complement of subtrahend to the minuend. In this operation if the MSB of addition is a '0'.

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Then the answer is correct and if MSB is '1', then answer is having negative sign. Hence, by using full adders subtraction can be carried out.

Figure above the realization of 4 bit adder-subtractor. From the figure it can be seen that, the bits of the binary numbers are given to full adder through the XOR gates. The control input is controls the addition or subtraction operation

When the SUBTRACTION input is logic '0', the B3 B2 B1 B0 are passed to the full adders. Hence, the output of the full adders is the addition of the two numbers.

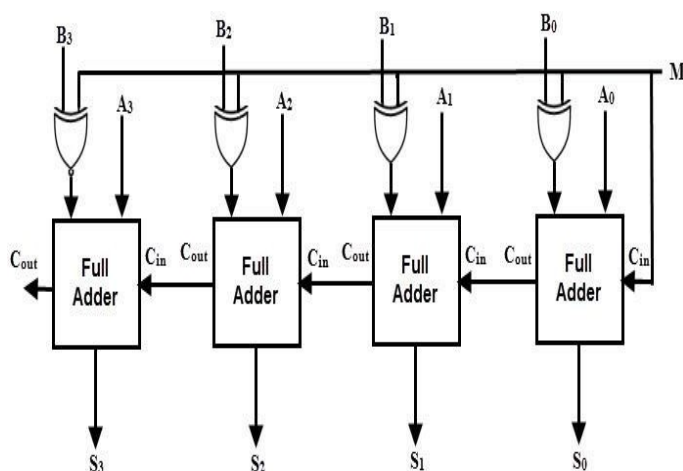


Fig.6 Adders & Subtractor

When the SUBTRACTION input is logic '1', the B3 B2 B1 B0 is complemented. Further, the SUBTRACTION logic '1' input is also work as Cin for the LSB full adder, due to which 2's complement addition can be carried out. Hence, the outputs of the full adders in this case are the subtraction of two numbers. In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. The most common type is a sequential digital logic circuit with an input line called the clock and multiple output lines. The values on the output lines represent a number in the binary or BCD number system. Each pulse applied to the clock input increments or decrements the number in the counter.

A counter circuit is usually constructed of a number of flip-flops connected in cascade. Counters are a very widely used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits.

CODING IMPLEMENTATION

```

module Dff (Clk,Rst,Din,Dout); input Clk,Rst;
input Din; output Dout; reg Dout;
always@(posedge Clk) if (Rst)
Dout <= 0; else
Dout <= Din;
End module
module Phase_Counter (Clk,Rst,En,Stop,Out,PC_Out); input Clk,Rst;
input En,Stop;
output [7:0]Out,PC_Out; reg [7:0]Out,PC_Out; always @(posedge Clk) if (Rst)
begin
Out <= 8'b0; end
else if (En) begin
Out <= Out + 1; end
else if (Stop) begin PC_Out=Out; end

```

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end module

VI. ADVANTAGES

- Optimal Operation of Adder result.
- Considerable improvement in both error and hardware cost metrics
- Improves MSE by 58% while reducing the ADP by 13.8%

VII. CONCLUSION

We have discussed the development of a sensitive phase detection logic core for FPGA, having precision, accuracy, and resolution in the range of a few picoseconds. This can be used within FPGA as a monitoring device of phase relationship between digital clock pulses, without any additional circuitry. The design is modularized in a way that allows designers to modify different components for more robustness of the design, like replace XOR-based PD with other phase comparator.

The concept of using systematic sampling for subsample collection can also be extended to map other complex analog domain problem to digital domain.

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