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Power Factor Isolated Using the Transformer Leakage Inductance to Make a Corrected Power Supply

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ABSTRACT: The widespread use of electronic devices increases the need for compact power factor corrected power supplies. This paper describes an isolated power factor corrected power supply that utilizes the leakage inductance of the isolation transformer to provide boost inductor functionality. The bulk capacitor is in the isolated part of the power supply allowing for controlled startup without dedicated surge limiting components. A control method based on switch timing and input/output voltage measurements is developed to jointly achieve voltage regulation and input power factor control. A prototype design is implemented with detailed measurements and waveforms shown to confirm the desired functionality.

KEYWORDS: AC-DC Power Conversion, Power Factor Correction, Transformer Leakage Inductance.

I. INTRODUCTION

Power factor correction techniques have been researched widely in the literature [1][2] and active PFC using high frequency switching techniques [3] are now commonly used. The overarching principle involves controlling the input current drawn from the mains input to achieve the required current shape for low THD and high-power factor. The power supply must provide a regulated DC output voltage and for many applications, galvanic isolation is also required. The basic boost or step-up converter [4] forms the core of most architectures as it has an input inductor that allows input current control to be readily achieved. The well-known flyback converter can be derived from the buck-boost converter, but with a transformer for output voltage isolation [4].

Traditionally for PFC supplies, flyback converters have been used for lower power levels (100W). For higher power levels (500W), a separate boost converter for PFC and separate DC to DC converter with transformer isolation for output DC voltage regulation is used. The widespread use of electronic devices from single phase AC supplies necessitates the increasing use of power factor corrected (PFC) power supplies in many applications including electronic equipment, computer servers and consumer products. PFC power supplies provide low total harmonic distortion (THD) in the current drawn from the line and this is an increasingly important requirement.

For lower power levels, flyback type architectures, often using a single switching element can provide PFC functionality, and use an output bulk capacitor for energy storage. A range of flyback-based power factor corrected power supplies have been developed and are described in the literature. Ref. [5] describes a 60W flyback PFC supply to achieve IEC61000 THD requirements. A 10W to 30W LED lighting supply is described in [6] and another 60W supply described in [7]. A 72W flyback design is shown in [8] and a 100W flyback PFC design is described in [9]. In these architectures, the flyback transformer initially stores energy from the input source and then releases it to the output bulk capacitor. The transformer thus provides the PFC input current control and galvanic isolation. However, the need to store all the energy in the flyback transformer, the unidirectional core excitation [4], high voltage stresses in the switching device and difficulties with the transformer leakage inductance, limit the usage of such power supplies to lower power

levels.

At higher power levels, two stage supplies with a separate boost PFC stage and isolated DC to DC stage are widespread. They typically consist of a power factor correction stage, based around a boost converter with large bulk storage capacitor to control the input line current, followed by an inverter driving a high frequency isolation transformer and finally an output stage with at least some filtering components. Such designs work well, especially



when there is a need to supply a number of different voltage rails and a long holdup time is required. Most of these architectures use one (or more) boost inductors in the active PFC stage [3], and such inductors need to handle the full supply power levels resulting in a significantly sized component. The design of such front-end PFC converters is a tradeoff between boost inductor size and high frequency losses [10]. Also, cascading multiple power stages leads to reduced overall efficiencies. The front-end boost PFC stage typically has high in-rush current on startup, or needs additional components to limit the in-rush current [11][12]. Therefore, there has been considerable research published on other architectures that attempt to eliminate or mitigate some of the disadvantages of both the flyback and two stage PFC AC/DC power supplies.

Again, only a single controlled switch is used but a number of separate magnetic cores and inductor elements are required. For higher power levels, modified two stage structures have been proposed. An architecture to improve on the existing two stage PFC is described in [10] which moves the boost inductor and bulk capacitor to the isolated side of a resonant LLC converter with the effect of improving the voltage stresses on the switching devices and providing an output power of 250W. A two-stage structure proposed in [16] uses a boost converter PFC with a resonant LLC converter. The design uses transformer coupled power transfer from the boost inductor to the output. Using two transformers (one providing the boost inductor functionality), a power output of 480W is provided

II. PROPOSED PFC ARCHITECTURE

In this paper an active power factor corrected power supply is described, whereby the leakage inductance of the high frequency isolation transformer is used to provide the functionality of the boost inductor. Minimization of the leakage inductance in high frequency isolation transformers is normally desirable in most DC-to-DC converters, although resonant and soft switching architectures do use a controlled amount of leakage inductance [17] for the purpose of reducing switching losses. The use of a controlled amount of leakage inductance is proposed in this paper to eliminate the need for two separate magnetic components in the two stage PFC converter and instead uses one magnetic component to achieve both the power factor correction and galvanic isolation. In-rush current on startup can also be controlled by implementing a soft start strategy whereby the large bulk capacitor is initially charged up in a controlled manner.

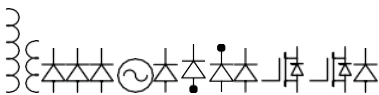


Fig. 1. Circuit diagram of the proposed power supply architecture

III. PROPOSED ARCHITECTURE

The circuit diagram of the proposed power supply is shown in Fig. 1. A conventional 4 diode full wave rectifier rectifies the input AC source voltage producing a voltage V_R . This voltage is inverted to the high frequency f_s with a half bridge inverter before being applied to a high frequency transformer T_x . The half bridge inverter consists of the two switches M_1 and M_2 operated out of phase with a 50% duty cycle at the switching frequency f_s and the capacitive divider formed by C_1 and C_2 . The capacitors C_1 and C_2 prevent DC current flowing through the transformer primary and causing saturation problems. The values of C_1 and C_2 are chosen sufficiently small such that at the mains frequency f_{ac} and low power level, they allow the rectifier output voltage V_R to follow the input mains waveform envelope. However, at the switching frequency, their values are sufficiently large to act as fixed voltage sources and not resonate with the transformer inductances or load. Fig. 2 and Fig. 3 show qualitative voltage and current waveforms for the circuit of Fig. 1. The mains input voltage is $V_M(t) = \sqrt{2}V_{AC} \sin(2\pi f_{ac}t)$, with V_{AC} being the rms input voltage and $V_R(t)$ being the input voltage fully rectified. The transformer primary voltage $V_P(t)$ switches at the high frequency rate f_s , but with an amplitude of half $V_R(t)$, due to the half bridge configuration. The symbol for the transformer in Fig. 1 is drawn to emphasize that the transformer leakage inductance is used in the circuit rather than the usual case whereby leakage inductance is minimized as much as possible. The key to the operation of the circuit is the bidirectional secondary shorting switch shown in Fig. 1 [21].

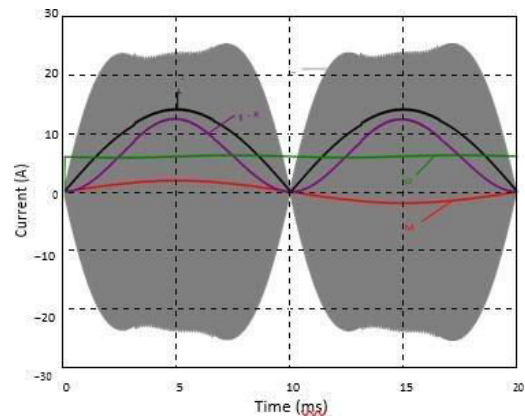
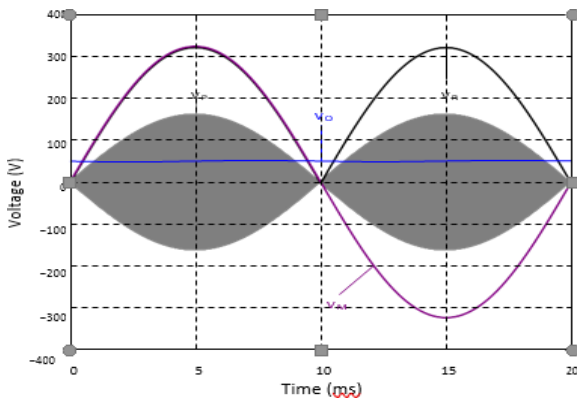


Fig. 2. Qualitative voltage waveforms for the circuit of Fig. 1 over a full AC cycle. Fig. 3. Qualitative current waveforms for the circuit of Fig. 1 over a full AC cycle.

In effect, the transformer leakage inductance and secondary shorting switch act as a step up or boost converter with the output rectifier and bulk capacitor CB. However, the input voltage polarity reverses once each cycle and the boost operation is carried out in two $T/2$ time periods, each with opposite polarity voltage and current waveforms.

IV. THEORY OF OPERATION

Fig. 4 shows a simplified circuit model for the proposed power supply. Assuming the switching frequency of the converter is very high compared to the AC source frequency, the input to the transformer can be considered to be essentially a 50% duty cycle square wave with period T and peak amplitude $\pm VI$. The model in Fig. 4 is referenced to the secondary side of the transformer and the voltage amplitude into the transformer model is the primary voltage $VP(t)$ multiplied by the turn's ratio of the transformer, at time $t = kT$.

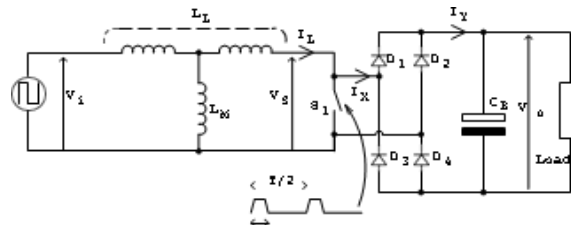


Fig. 4. Simplified circuit model for the proposed power supply.

The operation of the circuit is based on the assumption that the transformer magnetizing inductance LM has little effect on the operation of the circuit other than to add a magnetizing current to the input source. Simulations show that magnetizing currents significantly less (a factor of $1.5\times$ or less), than the currents being transferred, have little impact on the circuit overall functionality. This is verified in the experimental prototype waveforms of section V-B. The total leakage inductance of the transformer is denoted LL and the current flowing out of the transformer secondary winding is denoted $IL(t)$. The operation of the system is essentially that of a step up or boost converter and is based around the timing of shorting switch $S1$ in Fig. 4. At the beginning of a switching cycle, the input voltage switches to $+VI$ (dropping the $[kT]$ for notation for clarity) and simultaneously the shorting switch $S1$ is turned on. The current $IL(t)$ in the leakage inductance LL rises linearly while the switch $S1$ is on.

When the switch $S1$ is turned off, the current in the leakage inductance is forced through the rectifier diode bridge formed by $D1, D2, D3,$ and $D4$, and into the capacitor CB and system load, and the current in the leakage inductance falls. After a period of $T/2$, the input voltage changes sign to $-VI$ and the same operation occurs, except for a change in the sign of the inductor current. Two distinct operation modes of the circuit can be identified depending on whether the leakage inductance current starts at zero and returns to zero before time $T/2$, denoted as the discontinuous conduction mode (DCM), or when the leakage inductance current starts the cycle with a non-zero (negative) value, retains a non-zero (positive value) at time $T/2$ and returns to a non-zero (negative) value at the end of the cycle (time T), denoted as

the continuous conduction mode (CCM). To achieve unity power factor, the circuit needs to be operated in such a manner as to control the input current drawn from the supply. The two operating modes are now discussed in detail to relate the input current drawn to the timing period T_1 .

V. POWER SUPPLY CONTROL

The control objective for the power supply is to provide a constant output voltage and unity input power factor. This requires measurement of the output voltage and adjustment of the input current through the GM factor defined in section III-A. However, calculating the time parameter T_1 in section III-A and III-B also requires knowledge of the parameter L_L , the leakage inductance, which may not be accurately known. Therefore, a new control parameter K is defined as: $K = G_M L_L / T$. and K is used for control rather than G_M . The feedback loop of Fig. 5 can then be used to control the power supply. In Fig. 7, the power supply output voltage V_O is measured and compared to a reference voltage V_{REF} to produce an output voltage error $V_{ERR} = V_O - V_{REF}$. This error voltage is used by a PID controller with dynamics below the input AC frequency f_{AC} to adjust the variable K to control the output voltage V_O . The variable K , is used in the timing generator to generate the inverter timing and the secondary shorting period T_1 twice per sample period T . The timing generator uses the measured power supply output voltage V_O , and a scaled version of the input rectifier voltage V_R as $V_I = 1/2 N_s N_p V_R$. Using K , V_I and V_O , the timing generator evaluates the condition in eqn. 19 and if the result is true, the DCM is used to calculate the time period T_1 . Otherwise, the CCM is selected and eqn. 18 is used to calculate the time period T_1 .

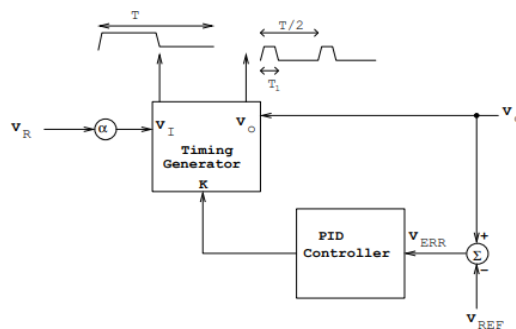


Fig 5. Feedback control for the power supply.

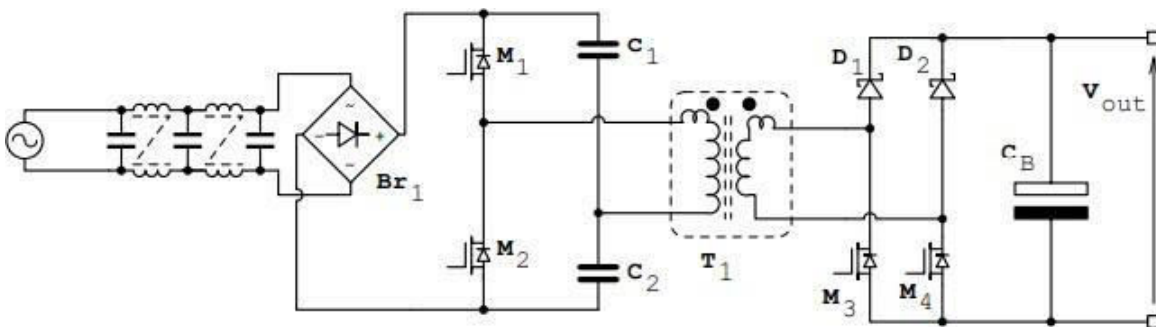


Fig. 6. Prototype power electronics schematic.

The power electronics schematic of the prototype power supply is shown in Fig. 6. A bridge rectifier Br_1 is used to rectify the input AC voltage and a half bridge inverter based on MOSFETs M_1 and M_2 drive the transformer. The prototype is based on a semi synchronous rectifier for the output rectifier [21]. In this case, two MOSFET transistors M_3 and M_4 are used to perform the secondary shorting during the T_1 period by turning on both transistors. During the remaining time, only one of the transistors is left switched on to perform the rectification function in conjunction with one of the Schottky diodes, D_1 or D_2 . The measured parameters of the constructed prototype trans former are listed in

Table I, together with the other power components used in the prototype power supply. Control of the prototype is implemented in firmware on a modern 32bit microcontroller. An internal 10-bit ADC measures the input rectified voltage and bulk capacitor output voltage. The microcontroller performs the calculations for the PID output voltage control and the timing calculations as per section IV with the timing signals generated with on-chip PWM generators.

VI. RESULTS

The efficiency of the converter is determined by the component losses and an analytical model of the relative contributions results in the distribution shown in Fig. 7. The largest contributions are given by the Schottky diodes conduction losses and the transformer core and winding losses. Fig. 8 shows an infra red thermal image of the prototype showing the highest spot temperature on the windings of the transformer. Switching losses dominate in the secondary MOSFET.

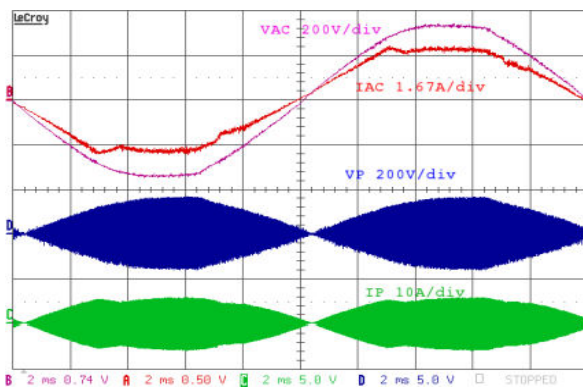


Fig. 7. Measured waveforms at 300W operation over a complete line cycle, input AC voltage (VAC) and current (IAC) and transformer primary voltage (VP) and current (IP)

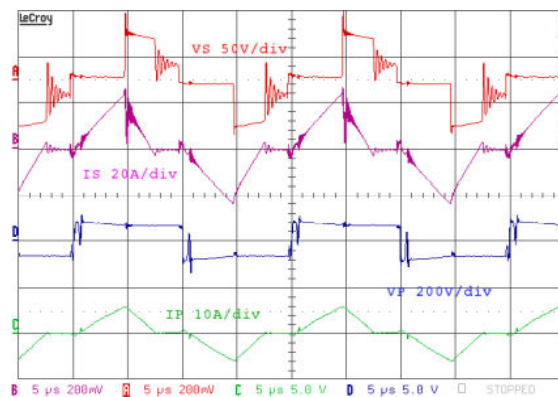


Fig. 8. Measured waveforms at 300W operation, 1.5ms from zero crossing and operating in DCM mode. Transformer primary voltage (VP) and current (IP) and secondary voltage (VS) and current (IS).

VII. COMPARISON WITH EXISTING DESIGNS

A key motivation for the work reported in this paper is the reduction of size and weight of the converter with a key component of these being the magnetic elements. Table III provides a comparison of the prototype developed with a range of PFC isolated supplies described in the literature. Flyback type architectures dominate at lower power levels (below 100W) with two stage architectures accounting for higher power levels. The prototype based on the proposed architecture in this paper compares well with the other designs and industry expectations [22], and should provide a useful topology for PFC converter designers.

VIII. CONCLUSION

This paper describes an isolated AC/DC power supply it utilizes the isolation transformer's leakage inductance to perform active power factor correction. For power levels above those of flyback type PFC supplies, the suggested architecture allows for a compact, lightweight power supply. The theory of operation with two conduction modes is discussed, and a power factor control method based on time is developed. A prototype power supply is designed and built to test the operating principle experimentally. The active power factor correction capability is verified by measurements, which show a high power factor and low THD.

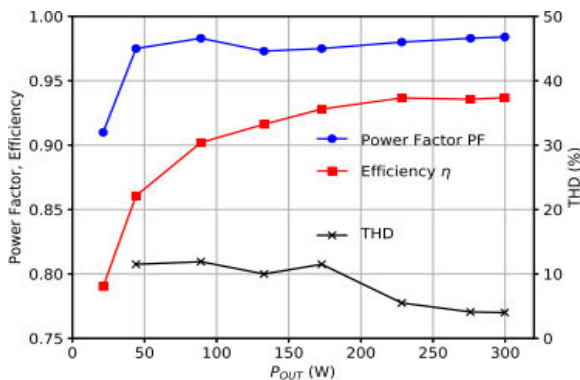


FIGURE 9. Measured efficiency and power factor for the prototype

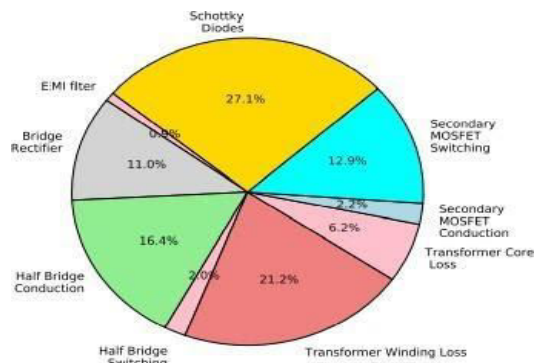


FIGURE 9. B Calculated loss contributions from the circuit elements.

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