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Review on High Speed Unsign & Sign Multiplier using Optimized Compressor based Adder

Juveria Khan¹, Prof. Rajesh Sharma², Prof. Abhishek Agwekar³

M. Tech. Scholar, Department of Electronics and Communication, T.C.S.T, Bhopal, India¹

Assistant Professor, Department of Electronics and Communication, T.C.S.T, Bhopal, India²

Head of Department, Department of Electronics and Communication, T.C.S.T., Bhopal, India³

ABSTRACT: - Explosive growth in the VLSI industry using submicron CMOS process technology, it is possible to place entire system-on-chip (SOC). As the VLSI technology is growing the computational speed of the system is also increasing, with further need of small area and lower power dissipation. Among several computational units, multiplication operation is the basic need for many applications. High speed DSP applications such as image processing, 2-D, 3-D graphics, video compression, decompression, communication systems, high speed embedded systems, supercomputers and vector processors requires high speed multipliers. Since, the multiplication operation is the more time critical, more area and more power consuming operation, the specialized design of multipliers are essential with small delay, smaller in silicon chip area and lower power consumption. This paper has studied of sign and unsign dada multiplier and will be simulated Xilinx software.

KEYWORDS:- Sign, Unsigned, Dadda Multiplier, Xilinx Software

I. INTRODUCTION

The multiplication operation is more time critical, more area and more power consuming operation, therefore, the specialized design of multipliers for less delay, smaller in area and low power consumption is essential. The multiplication operation consists of three phases: 1) generating partial products; 2) reducing the partial products to two rows; 3) and finally adding the two rows the product is obtained.

Multiplication is an imperative crucial capacity in math activities. Increase based tasks, for example, Multiply and Accumulate (MAC) unit and internal items are a portion of the every now and again utilized Computation-Intensive Arithmetic Functions right now executed in numerous Digital Signal Processing (DSP) applications, for example, convolution, Fast Fourier Transform (FFT), channel circuits and in microchips in its number juggling and rationale unit (ALU). Since duplication overwhelms the execution time of most DSP calculations, so there is a need of rapid multiplier. Right now, increase time is as yet the overwhelming element in deciding the guidance process duration of a DSP chip.

In this work we have put into impact a fast Vedic multiplier utilizing barrel shifter. The sutra was actualized by adjusted structure of "Nikhilam Sutra" because of its element of lessening the quantity of halfway items. The barrel shifter is utilized at various dimensions of structures to lessen the postpone when contrasted with regular multipliers. The equipment usage of Vedic multiplier is utilizing barrel shifter adds to satisfactory enhancement of the speed.

In numerous DSP calculations, the multiplier lies in the basic postpone way and at last decides the execution of calculation. The speed of increase activity is extraordinary significance in DSP just as by and large processor. In past increase was executed with a succession of expansion, subtraction and move activities. There have been numerous calculations recommendations to play out the duplication, and each offering distinctive preferences and having regarding speed, circuit intricacy and zone and power utilization.

The multiplier is a genuinely vast square of a processing framework. For augmentation calculations performed in DSP applications inactivity and throughput are the two noteworthy worries from postpone viewpoint. Inertness is the genuine



deferral of registering a capacity, a proportion of to what extent the contributions to a gadget are steady is the last outcome accessible on yields. Throughput is the proportion of what number of augmentations can be performed in a given timeframe multiplier isn't just a high defer square yet in addition a noteworthy wellspring of intensity scattering. That is the reason in the event that one likewise means to limit control utilization, it is of extraordinary enthusiasm to diminish the postponement by utilizing different defer advancements.

Propelled multipliers are the inside parts of all the mechanized flag processors (DSPs) and the rate of the DSP is commonly constrained by the speed of its multipliers. Two most fundamental duplication computations followed in the electronic hardware are show increment figuring and Booth enlargement estimation. The figuring time taken by the display multiplier is moderately less in light of the fact that the midway things are discovered independently in parallel. The delay associated with the display multiplier is the time taken by the signs to spread through the portals that shape the Multiplication bunch. Corner increment is another imperative enlargement figuring. Broad corner groups are required for quick duplication and exponential tasks which therefore require far reaching mostly total and inadequate pass on registers. Duplication of two n-bit operands using a radix-4 corner account multiplier requires generally $n/(2m)$ clock cycles to make the base important part of the last thing, where m is the amount of Booth recorder wind stages. Henceforth, a broad spread deferral is associated with this case.

II. LITERATURE REVIEW

Omid Akbari et al. [1], in this paper, we propose four 4:2 blowers, which have the adaptability of exchanging between the correct and inexact working modes. In the inexact mode, these double quality blowers give higher speeds and lower control utilizations at the expense of lower precision. Every one of these blowers has its own dimension of exactness in the inexact mode just as various deferrals and power dispersals in the estimated and correct modes. Utilizing these blowers in the structures of parallel multipliers gives configurable multipliers whose exactnesses (just as their forces and speeds) may change progressively amid the runtime. The efficiencies of these blowers in a 32-bit Dadda multiplier are assessed in a 45-nm standard CMOS innovation by contrasting their parameters and those of the best in class rough multipliers. The consequences of correlation demonstrate, by and large, 46% and 68% lower postponement and power utilization in the inexact mode. Additionally, the viability of these blowers is surveyed in some picture preparing applications.

G. Challa Ram et al. [2], this paper depicts the structure of fast Vedic multiplier that utilizes the methods of Vedic arithmetic dependent on 16 sutras (calculations) to enhance the execution. The proficiency of Urdhva Tiryagbhyam (vertical and across) Vedic strategy for increase which is not quite the same as the procedure of typical duplication is displayed. Urdhva - Tiryagbhyam is the most effective calculation that gives least postponement for duplication for a wide range of numbers regardless of their size. Vedic multiplier is coded in Verilog HDL and invigorated and orchestrated by utilizing XILINX programming 12.2 on Spartan 3E pack. Further the structure of exhibit multiplier is contrasted and the proposed multiplier as far as deferral, memory and power utilization.

S. P. Pohokar et al. [3], this paper quickly portrays the Urdhva-Tiryagbhyam Sutra of Vedic science and we have structured multiplier dependent on the sutra. Vedic Mathematics is the antiquated arrangement of arithmetic which has a one of a kind system of counts dependent on 16 Sutras which are found by Sri Bharti Krishna Tirthaji. In this period of digitalization, it is required to build the speed of the advanced circuits while diminishing the on chip zone and memory utilization. In different uses of computerized flag preparing, augmentation is one of the key segments. Vedic method wipes out the undesirable increase steps in this manner diminishing the proliferation delay in processor and subsequently decreasing the equipment unpredictability as far as territory and memory necessity. We execute the fundamental building square: 16 x 16 Vedic multiplier dependent on Urdhva-Tiryagbhyam Sutra. This Vedic multiplier is coded in VHDL and orchestrated and reenacted by utilizing Xilinx ISE 10.1. Further the structure of exhibit multiplier in VHDL is contrasted and proposed multiplier as far as speed and memory.

Gokhale et al. [4], in this paper, Vedic multiplier is designed using area-efficient Carry Select Adder (CSLA). As the multiplication is the process of subsequent addition, adder is important block in implementation of multiplier. Digital



adder has problem of carry propagation, thus carry select adder is used instead of simple Ripple Carry Adder (RCA). Carry select adder is known to be one of the fastest adder structures. Here Vedic multiplier is implemented instead of normal multipliers like add and shift multiplier, array multiplier etc. The goal of this paper is to design Vedic multiplier based on crosswise and vertical algorithms using area-efficient CSLA. Conventional CSLA designs like Binary to Excess one Converter (BEC) based CSLA and Modified CSLA (MCSLA) are compared with proposed CSLA design to prove its efficiency. It shows improved performance in terms of area. This renovated CSLA is used to design proposed Vedic multiplier. It has 6% less area than Vedic multiplier using MCSLA and 16% less area than Vedic multiplier using BEC-based CSLA. Proposed design is also compared with the Booth multiplier. Proposed multiplier showed more excellent results than Booth multiplier.

G. Gokhale et al [5], in this work, we are coordinating warm mindful structure approach in vitality productive Vedic multiplier on FPGA. In the start of this universe, Veda depicts warm accepting from the Sun god as Suryamrit. Presently, entire world is feeling on edge about temperature. This paper manages that question and the entire work is going in bearing to get arrangement of this issue with system of encompassing (room) temperature scaling and vitality productive LVC MOS I/O standard. LVC MOS is an abbreviation for low voltage corresponding metal oxide semiconductor. For LVC MOS25, when our Vedic multiplier configuration is moved from 40nm structure to 90nm plan, there is 87.72% decrease in power scattering of Vedic multiplier when temperature is steady 20oC.

III. MULTIPLIER

All the parallel, the pipeline and the high performance multipliers implemented in hardware is illustrated in the block diagram of Figure 1. It consists of three phases as follows.

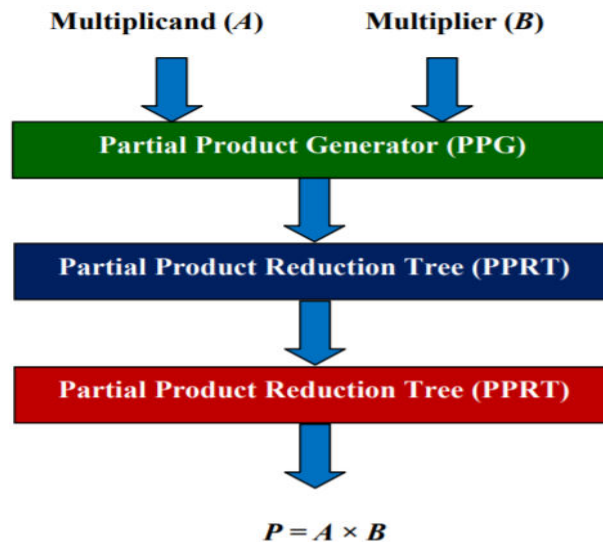


Fig. 1: Block diagram of Multiplier

- Partial Product Generator (PPG)
- Partial Product Reduction Tree (PPRT)
- Carry Propagate adder (CPA)

The PPG creates fractional items either utilizing two info OR door or by utilizing MBE strategy. The PPRT is utilized to pack the few varieties of halfway item pushes into a variety of two lines. The CSA and different kinds of blowers can

Compressor Based Adder

4:2 Compressor

A 4:2 compressor is capable of adding 4 bits and one carry, in turn producing a 3 bit output. The 4-2 compressor has 4 inputs X_1, X_2, X_3 and X_4 and 2 outputs Sum and Carry along with a Carry-in (C_{in}) and a Carry-out (C_{out}) as shown in figure 3.1. The input C_{in} is the output from the previous lower significant compressor.

The C_{out} is the output to the compressor in the next significant stage. The critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders and half adders.

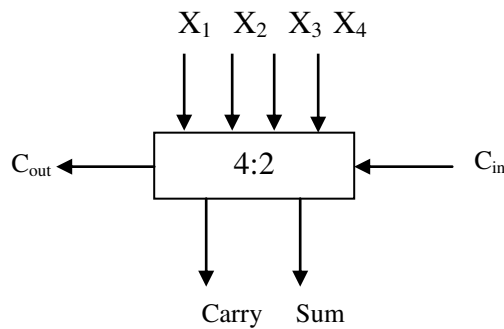


Fig. 2: Block Diagram of 4:2 Compressors

Similar to the 3-2 compressor the 4-2 compressor is governed by the basic equation

$$X_1 + X_2 + X_3 + X_4 + C_{in} = sum + 2 * (Carry + C_{out})$$

The standard implementation of the 4-2 compressor is done using 2 Full Adder cells as shown in figure 2. When the individual full Adders are broken into their constituent XOR blocks, it can be observed that the overall delay is equal to 4*XOR.

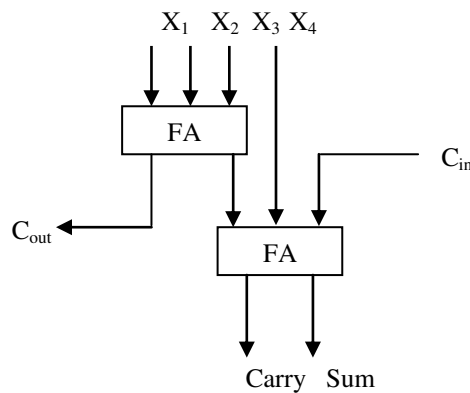


Fig. 2: Logic Diagram of 4:2 Compressors

Modified 4:2 Compressor

The block diagram in figure 3 shows the existing architecture for the implementation of the 4-2 compressor with a delay of 3*XOR. The equations governing the outputs in the existing architecture are shown below

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in}$$

$$C_{out} = (X_1 \oplus X_2).X_3 + (X_1 \oplus X_2).X_1$$

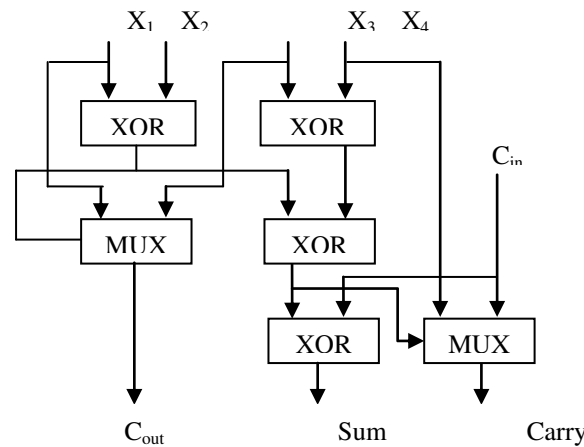


Fig. 3: Logical Diagram of Modified 4:2 Compressor

$$C_{arry} = (X_1 \oplus X_2 \oplus X_3 \oplus X_4).C_{in} + (X_1 \oplus X_2 \oplus X_3 \oplus X_4).X_4$$

In show the delay and area all the modified 4:2 compressors. 4:2 compressors replacing some XOR blocks with multiplexer’s results in a significant improvement in delay. Also the MUX block at the SUM output gets the select before the input arrive and thus the transistors are already switched by the time they arrive.

V. CONCLUSION

The multiplication operation consists of three phases: 1) generating partial products; 2) reducing the partial products to two rows; 3) and finally adding the two rows the product is obtained. Since the speed of the multiplier depends on the speed of the partial product generator (PPG), the speed of the partial product reduction tree (PPRT) and the speed of the carry propagate adder (CPA), many architectures have been developed to reduce the delay, the area and the power consumption. Proposed research work will have been the literature review on the PPG, PPRT, CPA, Signed Number Multipliers and Unsigned Number Multipliers.

REFERENCES

[1] Omid Akbari, Mehdi Kamal, Ali Afzali-Kusha, and Massoud Pedram, “Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 34, Issue 7, 2017.

[2] G. Challa Ram and D Sudha Rani, “Area Efficient Modified Vedic Multiplier”, International Conference on Circuit, Power and Computing Technologies (ICCPCT), 2016.



- [3] S. P. Pohokar, R. S. Sisal, K. M. Gaikwad, M. M. Patil and Rushikesh Borse, “Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics”, International Conference on Industrial Instrumentation and Control (ICIC) College of Engineering Pune, India, PP. No. 01-06, 2015.
- [4] Gokhale and P. D. Bahirgonde, “Design of Vedic Multiplier using Area-Efficient Carry Select Adder”, 4th IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI-2015), Kochi, pp. 10-13, August 2015, India.
- [5] G. Gokhale and Mr. S. R. Gokhale, “Design of Area and Delay Efficient Vedic Multiplier Using Carry Select Adder”, 4th IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI-2015), Kochi, pp. 10-13, August 2015, India.
- [6] Josmin Thomas, R. Pushpangadan and Jinesh, “Comparative Study of Performance Vedic Multiplier on The Basis of Adders Used”, International Conference on Electrical and Computer Engineering, pp. 01-05, 2015 IEEE.
- [7] Basant Kumar Mohanty and Sujit Kumar Patel, “Area-Delay-Power Efficient Carry-Select Adder”, *IEEE Transactions on Circuits and Systems—II: Express Briefs*, Vol. 61, No. 6, June 2014.
- [8] Pavan Kumar, Saiprasad Goud and A. Radhika, “FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter”, International Conference on Digital Circuit and System, 2013 IEEE.
- [9] Sushma R. Huddar and SudhirRao, Kalpana M., “Novel High Speed Vedic Mathematics Multiplier using Compressors”, International Conference on VLSI System, 2013 IEEE.
- [10] Abdoreza Pishvaie, Ghassem Jaberipur and Ali Jahanian, “Compressor CMOS (4; 2) reconns pour less multiplication binary number”, *Can. Journal Electronics Computation Engineering*, Vol. 36, No. 3, summer 2013.



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