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A futuristic digital interface with a glowing Earth globe in the center. The background is dark blue with various data visualizations including bar charts, line graphs, and network diagrams. Text elements like 'BUSINESS', 'NETWORK SEARCH', and 'LORDING 100%' are visible. The overall aesthetic is high-tech and data-driven.

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# Analysis and Design of Low Power Arithmetic Circuits using Reversible Logic Gates

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**ABSTRACT:**In recent years, VLSI design plays a vital role to enhance the density of integration in VLSI chips. VLSI is the process of generating an integrated circuit (IC) by merging millions of MOS transistors onto a single chip. It is considered as one of the best alternatives to work with this methodology, to help shorten power consumption and power dissipation. By using reversible logic, one correspondence mapping between input and output causes the tiniest loss of information and it scatters very low heat. Here quantum computing, optical computing, and nanotechnology devices, the reversible logic has built up a lot of absorption. Quantum computing devices hypothetically operate at ultra-high speed and consume immeasurably less power. In this project, an energy-efficient low power reversible arithmetic circuit is proposed by CMOS design using Tanner EDA.

**KEYWORDS:**VLSI, CMOS, GDI, Reversible logic gates, Full adder.

## I. INTRODUCTION

The heart of digital electronics is logic gates. An Electronic device that is used to compute a function on a two-valued signal is a logic gate. The basic building block of digital circuits is logic gate. Basically, all logic gates have two inputs and one output. Some logic gates like inverter or NOT gate has two input and one output. By receiving the voltage input the inputs of the logic gates are designed to receive only binary data (only low 0 or high 1). The high logic level represents 3 or 5 volts and low logic level represents zero volts' positive supply voltage. To design a required digital circuit, we can connect any number of logic gates. The low power dissipating circuit design has become a promising research direction using reversible logic. Fredkin gate was invented by Edward Fredkin [1]. It is the universal logic gate and also known as the CSWAP gate. Fredkin gate can be designed by using AND, OR, XOR, and NOT gates. Fredkin gate contains three inputs and three outputs. Feynman gate has 2 inputs and 2 outputs and it is also recognized as the controlled-not gate (CNOT). Ripple carry adder is the simplest form of the adder. In ripple carry adder we will use half adder and full adder. In this project, we using Fredkin and Feynman gate for designing 4- bit ripple adder. An alternative CMOS logic is introduced to GDI logic[6]. GDI is a low power design technique which offers the implementation of the logic function with fewer numbers of transistors. GDI gates provide reduced voltage in their outputs, i.e. the output high (or low) voltage is deviated from the VDD (or ground) by threshold voltage ( $V_t$ ). The reduction in voltage is useful to power consumption. At the same time, this may lead to slow switching in the case of cascaded operation. At very low VDD operation, the break down output may even cause circuit malfunction.

## II. EXISTING METHOD

### A. Conventional Full Adder

The central to most digital circuits that perform addition or subtraction is called full adder circuit[14]. Full adder circuit adds together two binary digits, plus a carry-in digit to produce a sum and carry-out digit and it has three inputs and two outputs [4]- [13].

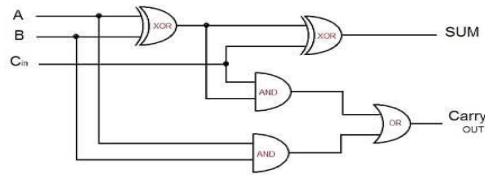


Figure 1:CMOS full adder logic diagram

Inputs			Outputs	
A	B	C <sub>in</sub>	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table1:CMOS full adder truth table

It has three inputs and the first two inputs are A and B and the third input is an input carry as C-IN. The normal output is designated as S which is SUM and the output carry is designated as C-OUT. It designed in such a manner that, it can take eight inputs at the time to create a byte-wide adder and cascade the carry bit from one adder to the another.

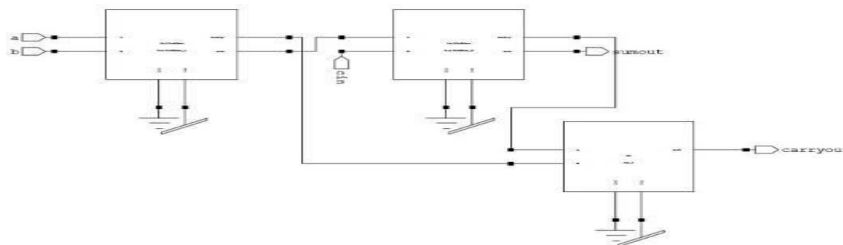


Figure 2:1-bit CMOS full adder schematic diagram

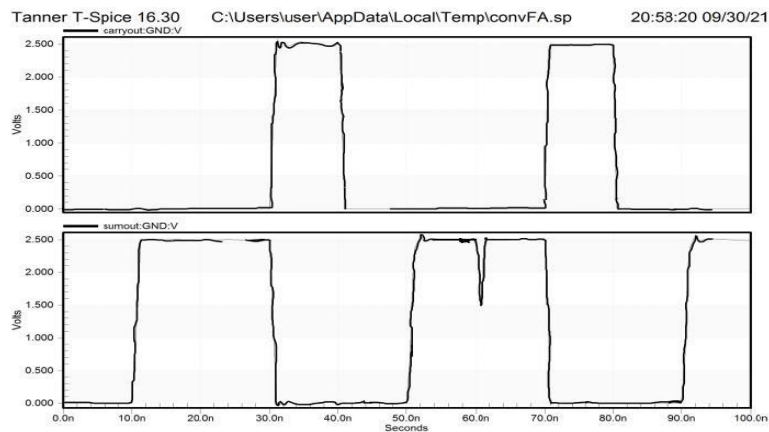


Figure 3: 1-bit CMOS full adder input and output waveform



**B.Reversible Full Adders**

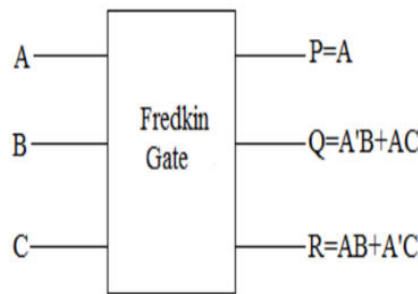
The reversible logic is a memory-less logic element that realize in injective logical function. The reversible logic operations cannot erase information and dissipate zero heat. This circuit actually operates in a background operations, allow reproducing the input from the output and consumes zero power.

The reversible logic gates are:

- 1.Fredkin gate.
- 2.Feynman gate.
- 3.Toffoli gate.
- 4.Peresgate.

**1.Fredkin gate**

The Fredkin gate was invented by Edward Fredkin, it is a computational circuit suitable for reversible computing[2]. Any logical or arithmetic operation can be constructed entirely by Fredkin gates so it is known as universal logic gate. The Fredkin gate is with three inputs and three outputs that transmits the first bit unchanged and swaps the last two bits if, and only if, the first bit is 1.



**Figure 4 :** Fredkin block diagram

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

**Table 2:** Fredkin truth table

**2. Feynman gate**

The one such reversible logic device[3], which has recently gained considerable interest in information processing and is a potential candidate for the realization of low-power photonic computational circuits is called Feynman gate (FG)9.

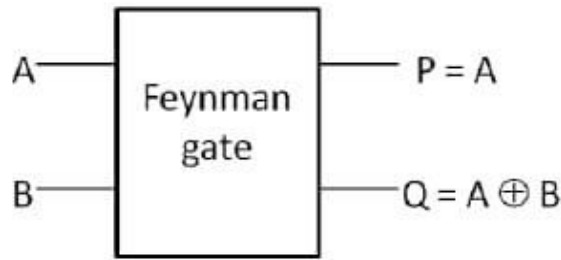


Figure 5 : Feynman block diagram

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table.3:Feynman truth table

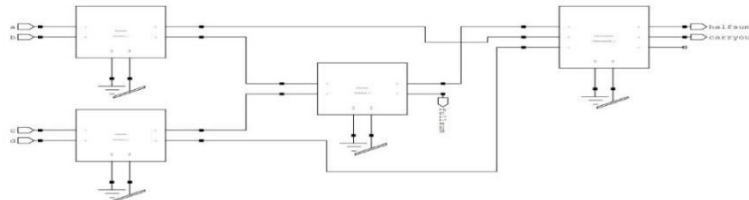


Figure 6: 1-Bit full adder using reversible logic

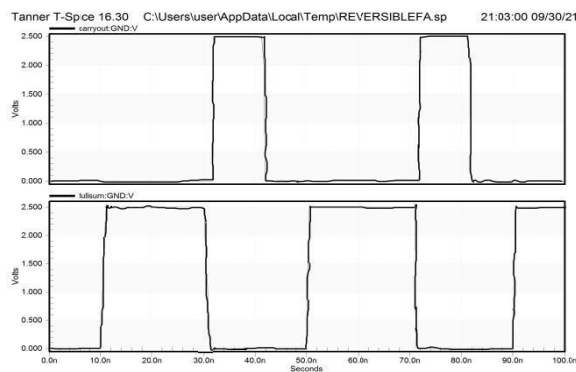


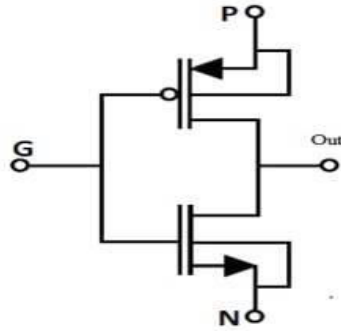
Figure 7: 1-Bit full adder using reversible logic input and output waveform





**C. GDI Logic Adder**

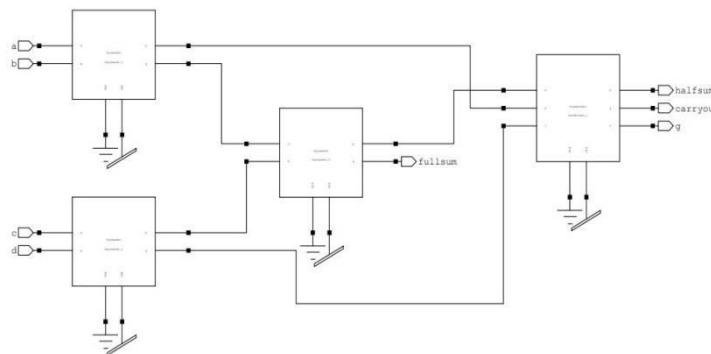
Gate diffusion input (GDI)[7] is described a new technique of low-power digital combinatorial circuit design. Reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design is allowed in GDI technique.



**Figure 8:** GDI Transistor

N	P	G	OUT	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

**Table.4:** GDI truth table



**Figure 9:** 1-Bit Full adder using GDI

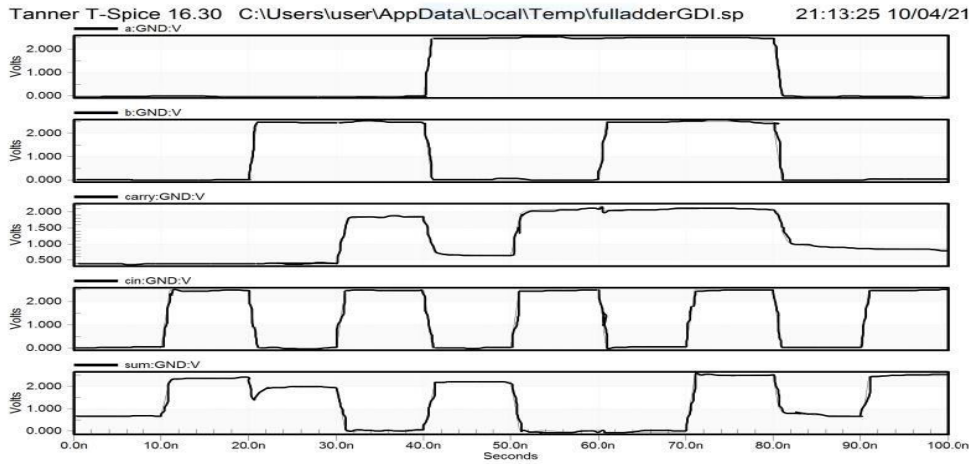


Figure 10 : 1-Bit Full adder using GDI output waveform

DESIGN/ METHODS	MOSFETS	POWER
1-BIT FULL ADDER	30	1669nW
1-BIT REVERSIBLE FULL ADDER	76	1021230nW
1-BIT GDI FULL ADDER(PROPOSED)	14	1.2457nW

Table.5: Comparison and results

III. PROPOSED METHOD

A.4-Bit ripple carry full adder using CMOS

Ripple Carry Adder or n- bit parallel adder is a combinational logic circuit. For the purpose of adding two n-bit binary numbers it is used. To adding two n-bit binary numbers it requires n full adders.

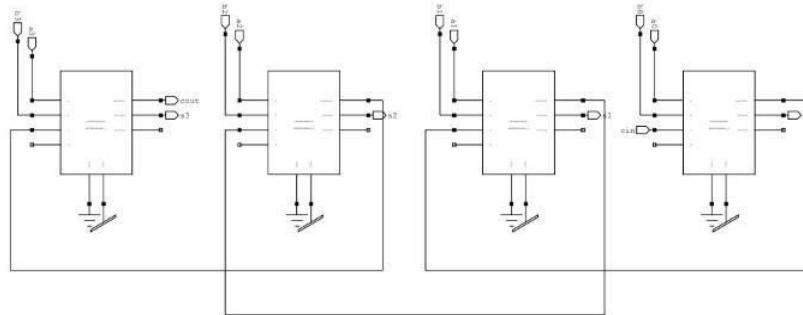


Figure 11 :4- Bit ripple carry full adder using CMOS

**B.Bit full adder using GDI(proposed)**

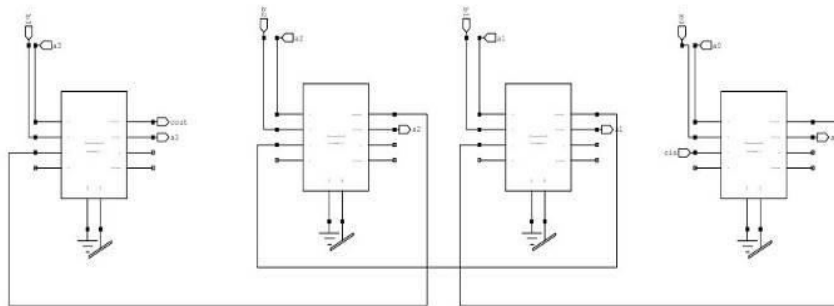


Figure 12: 4 -Bit full adder using GDI



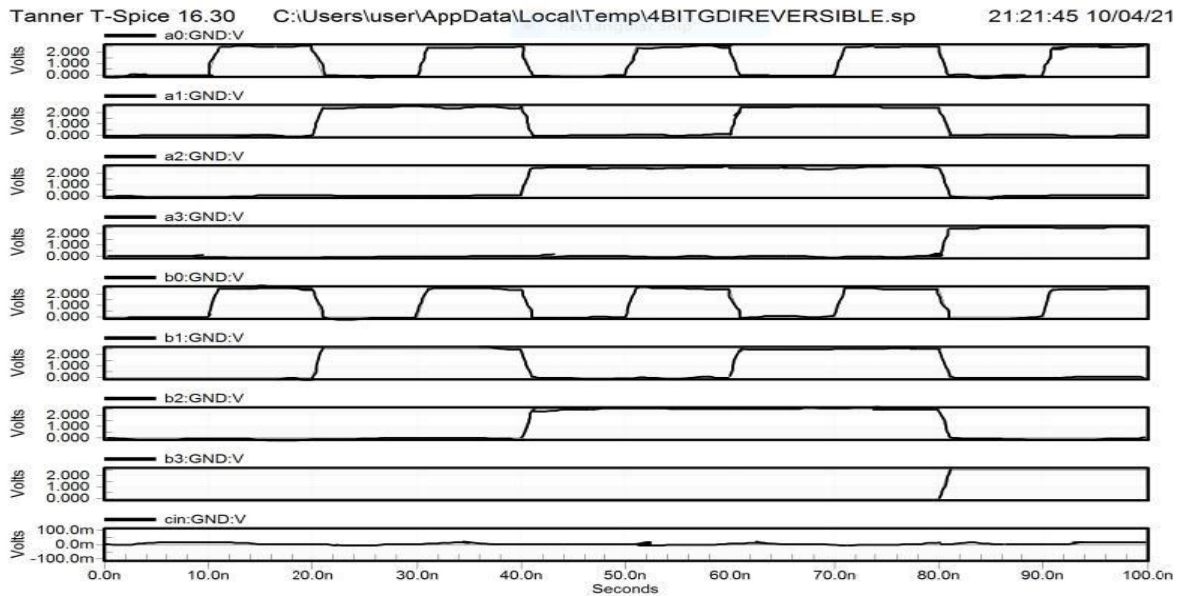


Figure 13 :4 -Bit full adder using GDI input waveform

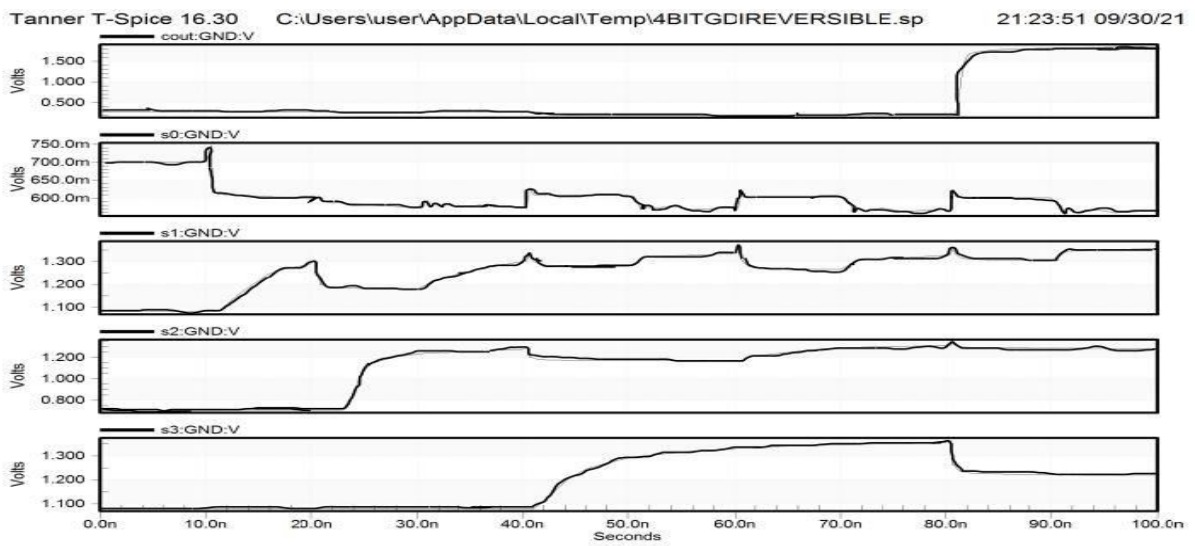


Figure 14:4 -Bit full adder using GDI output waveform

As comparing to other logic the proposed 4-bit full adder using GDI logic is more reliable[9]. The 4-bit full adder using GDI logic consumes less power and time and it uses less MOSFET'S.



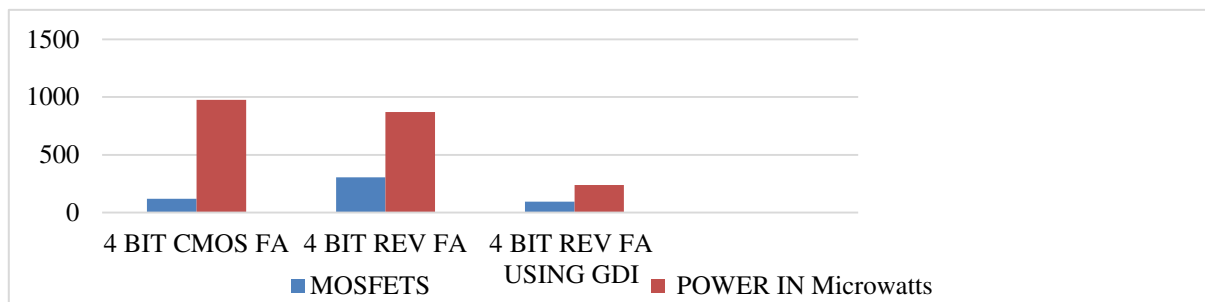
DESIGN/METHODS	MOSFETS	POWER
4-BIT FULL ADDER USING CMOS LOGIC	120	97.64nW
4-BIT FULL ADDER USING REVERSIBLE LOGIC	304	87.12nW
4-BIT FULL ADDER USING GDI LOGIC (Proposed)	96	2.37nW

Table6: Comparison and Results

IV. RESULT AND DISCUSSION

Here discussed about a detail analysis of average power consumption and delay of proposed GDI based logic gates are done by using Tanner EDA simulation. Comparison of proposed GDI technique with the existing conventional technique shows that the average power is decreasing by respectively. By proposing the proper analysis and design of low power arithmetic circuits using reversible logic gates[5]. To reduce power of a GDI based full adder gates some more circuit level power management techniques should be used so that it can be useful for low power applications[12]. Execution of different kinds of logic gates and digital circuits have to be carried out in order to determine the fields of circuitry, where GDI is very much superior over other design styles[8].

V. BAR CHART



The above Bar chart shows that the results of using GDI logic(proposed), reduction in MOSFETS(20%), and low power consumption(80%)in the above-designed simulation.



## VI. CONCLUSION

Power Dissipation of Digital circuits can be reduced by 15% 25% by using appropriate logic and also it can be reduced by 20%-40% by lowering switching activity. Here, the Gate Diffusion Input Technique is analyzed for minimizing the power consumption and delay of static digital circuits. This technique as compared to other currently used logic design styles allows less power consumption and reduced propagation delay for the low-power design of combinational digital circuits with a minimum number of transistors. In this paper, basic building blocks of digital gates and few combinational circuits are analyzed using GDI and other CMOS techniques.

## VII. FUTURE ENHANCEMENT

The future work will be focused on reduction of power and time in any combinational circuits using multiplexers and FIR filters.

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