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A futuristic digital interface with a glowing globe in the center. The background is dark blue with various data visualizations, including bar charts, line graphs, and network diagrams. Text elements like 'BUSINESS', 'NETWORK SEARCH', 'LOADING 100%', and 'MEDIA' are visible. A person's hand is seen at the bottom, interacting with the interface.

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Design and low Power Asynchronous NoC Architecture with Buffer less Router

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ABSTRACT: Network-on-chip (NOC) has been well accepted for energy efficient on-chip communication for multiple-core systems. However, the NOC router uses very high power and the number of routers grows in proportion to the number of cores. Additionally, removing buffers from NOC routers results in performance degradation and network congestion overhead. Making NOC energy efficient without increasing network congestion. In the project we presented the MESH topology implementation for the NOC router. The advantage of mesh topology is that it is simple to add additional devices and the data flow is done through the HUB. So in recent times buffer-less routers based on deflective routing have been touted as a possible solution, but they suffer from issues like sequential port allocation and slow critical paths and also increased latency. In this project we propose a 2D 4x4 asynchronous mesh NOC architecture with a novel router design using XY routing algorithms. In the proposed router design, we have eliminated traditional input and output buffers and crossbar switches. We have integrated priority encoder and arbiter which efficiently solves the long critical path issues of traditional buffer-less routers by dynamically changing the port priority and hence starvation and live/dead lock problem and improving sector consumption (ie, as low as 43%). We have used parallel transmission which enables us to improve speed (up to 73%) and reduce power consumption (0.56w) by eliminating I/O buffers. In our project we have implemented four routers in mesh connection in which all the data flow is controlled by a hub. Each router is connected to some processing device that delivers or needs data from other devices. Our proposed router reduces total energy by 18% and 25%, respectively, with negligible performance overhead.

KEYWORDS: Network on chip, asynchronous circuit, buffer less router

I. INTRODUCTION

In the modern world everyone wants to use small items that contain many features and are low cost. It is only possible if the performance value is combined into one device or one chip that helps to achieve our goal and need. For this researcher to develop the concept of "Nano-technology". The Nano means something small, very small. Following this, the biggest challenge was how to integrate intellectual property with a variety of resources quickly and effectively. To overcome this situation researchers are introducing a new method called the "System on Chip" SOC, which is a growing topic in modern communication technology. It is a good solution for combining a number, the functionality of a single object or a chip. SOC is a device or integrated circuit that integrates all system components into a single electronic device or chip. One chip contains digital signals, analog signals and integrated signals and can be calculated in any range. The SOC configuration consists of processor circuits, time, bus system and power control. Advantages of SOC: Low power with minimal use, faster performance and lower cost per gate and so on. SOC calculations are reliable and efficient. The most important return of these devices is the integration of a large number of objects into one device and the connection between them. To avoid this kind of complex problem, a new process called "Network on Chip" was introduced. NOC is the integration of complex network systems into a single device or chip. This reduces the production costs of SOC, increases efficiency and reduces time consumption.



II. RELATED WORK

1. The performance of hyper mesh NoCs in FPGAs.

These days, the use of multiprocessor systems has become a very common solution. The growing complexity of tasks requires that computer systems continue to improve performance. In multicore systems with a small number of cores (2-10 cores), communication between the cores and other chip objects takes place successfully with the help of a standard bus. The bus is the data transfer infrastructure between the basic blocks.

2. Use of irregular topologies for the synthesis of networks-on-chip.

Such a network allows for the separation of chip objects, which handle data transfer, and computer units. Each computer unit connects to a network with an interface connected to a router that provides data transfer between units. At the same time NoC is a separate subsystem and does not affect the internal organization of a computer unit that can use old buses to connect its building materials.

3. Using the NS-2 network simulator for evaluating multi-Protocol label switching in network-on-Chip.

The low-level model was developed in the Verilog language with continuous testing of the performance of algorithms, as well as the calculation of chip resources taken after integration. The results obtained have allowed us to confirm the hypothesis regarding the excellent characteristics of NoC based on circulant topologies, small chip resources compared to the use of other components. However, although encouraging results have been obtained, high-level simulation is needed to analyze the distribution of traffic on networks and the effectiveness of the algorithm control system in them.

III. METHODOLOGY

For this project, we have chosen to design a Router-less Router with 5 I / O ports; four directional ports (E, W, N, S) and one local port. Local port installation and local port deployment provide a connection with the local processor or controller, and the control ports (east, west, north, and south) are used to connect other neighboring nodes to the network. Here the value of the installation port is equal to the port-put port number which makes the router Dead lock free. Router internal structure. Contains advanced coding block, Arbiter (scheduler) block, Routing Controller (XY routing block) and LEDR encoder-decoder block. remove cross / out and change cross baths to improve space and energy consumption. There is no need for visible channels in our build as it is a buffer design with an equal number of I / O ports. read / write function at router level), Efficient location (No interruptions, visible channels and crossbar switching) and efficient Power (buffers use appropriate static power: when not in Dynamic: while running RD / WR). In this project, we propose the construction of an Asynchronous 4x4 Mesh NOC with a Buffer-less router using the XY route to FPGA. In the proposed Router design, we have removed the standard crossbar switch and the Input / output buffer. This design offers improved performance in terms of location, speed and energy consumption.

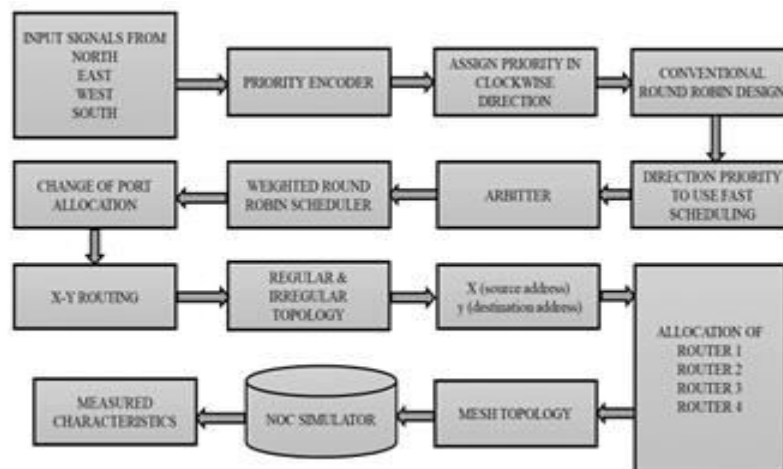


Figure 1:Block Diagram



IV. EXPERIMENTAL RESULTS

Asynchronous NOC architecture with buffer less counter was successfully designed and implemented. The output screenshots is given below

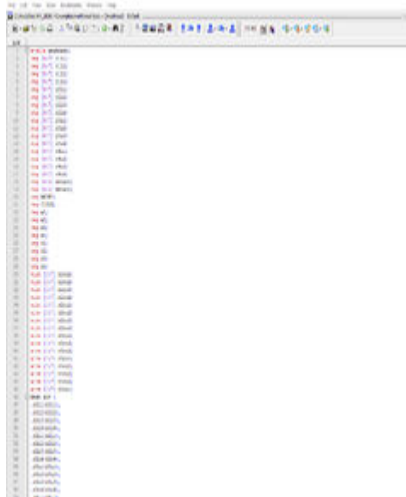


Figure 2: Verilog code for mesh topology

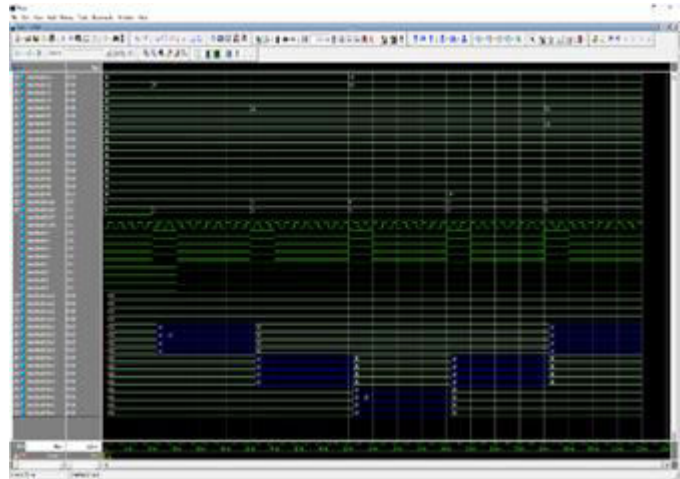


Figure 3: Output wave form for mesh topology

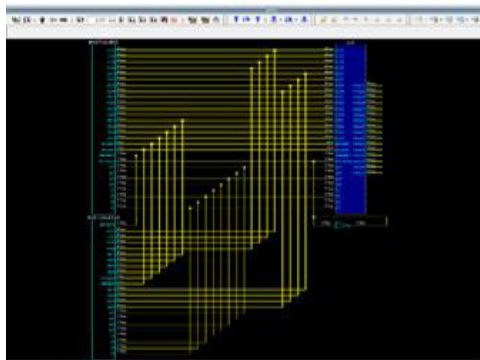


Figure 4: Schematic view for Mesh topology

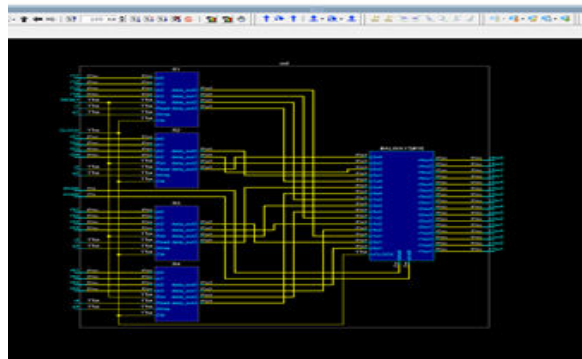


Figure 5: Router connection for Mesh topology

V. CONCLUSION

Introduced 2x dimensional 2 x 2 Asynchronous Mesh NOC Architecture with Router-less Router. In our design of the router system, we removed the I / O Buffer and replaced the traditional crossbar switch with Arbiter which handles port sharing efficiently at improved speeds and reduces hardware costs. Priority encoder and Arbiter together effectively solve hunger and Live / Deadlock problems. Local usage is reduced (12-43%) compared to a buffered router and a smaller sub-router. The corresponding transmission method used in our construction improves speed by (73-81%). Our most efficient design method for comprehensive communication software as fast as artificial intelligence, which enhances energy consumption and energy consumption. Our under-buffer design does not have the functionality of error detection and traffic congestion, our next step is to incorporate those structures into this design.



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