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Low-Power Ternary Content-Addressable Memory Design Based On a Voltage Self-Controlled Fin Field-Effect Transistor Segment

SHAIK.ASHIFUN BANU, M.HARI BABU

M.TECH 2nd Year, Department of Electronics and Communication Engineering, Specialization: VLSI&ES, QIS
College of Engineering and Technology, Ongole, Andhra Pradesh, India

Assistant Professor, Department of Electronics and Communication Engineering, College of Engineering and
Technology, Ongole, Andhra Pradesh, India

ABSTRACT: Ternary content-addressable memory (TCAM) is a popular component to use for fast and parallel data searching. However, with technology downscaling, TCAM consumes huge leakage power, which affects search performance. To control TCAM's leakage power consumption, this paper proposes a multiple-segment voltage self-controlled TCAM (VoSCT) that varies the back-gate voltages of fin field-effect transistors and the supply voltages of a TCAM entry. In the VoSCT, a TCAM entry is partitioned into several segments, and each segment operates in one of the three following modes: high-speed mode, low-power mode, and ultra-low-power mode. Examples that use a real routing table are employed to verify the feasibility of the proposed VoSCT, and the experimental results indicate that 38% of leakage power and 21% of total power can be reduced with only a 9% search delay increase and 4% area overhead increase compared with the traditional TCAM design.

I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.

During the mid-1920s, several inventors attempted devices that were intended to control current in solid-state diodes and convert them into triodes. Success did not come until after WWII, during which the attempt to improve silicon and germanium crystals for use as radar detectors led to improvements in fabrication and in the understanding of quantum mechanical states of carriers in semiconductors. Then scientists who had been diverted to radar development returned to solid-state device development. With the invention of transistors at Bell Labs in 1947, the field of electronics shifted from vacuum tubes to solid-state devices.

With the small transistor at their hands, electrical engineers of the 1950s saw the possibilities of constructing far more advanced circuits. As the complexity of circuits grew, problems arose. One problem was the size of the circuit. A complex circuit, like a computer, was dependent on speed. If the components of the computer were too large or the wires interconnecting them too long, the electric signals couldn't travel fast enough through the circuit, thus making the computer too slow to be effective.

Jack Kilby at Texas Instruments found a solution to this problem in 1958. Kilby's idea was to make all the components and the chip out of the same block (monolith) of semiconductor material. Kilby presented his idea to his



superiors, and was allowed to build a test version of his circuit. In September 1958, he had his first integrated circuit ready. Although the first integrated circuit was crude and had some problems, the idea was groundbreaking. By making all the parts out of the same block of material and adding the metal needed to connect them as a layer on top of it, there was no need for discrete components. No more wires and components had to be assembled manually. The circuits could be made smaller, and the manufacturing process could be automated. From here, the idea of integrating all components on a single silicon wafer came into existence, which led to development in small-scale integration (SSI) in the early 1960s, medium-scale integration (MSI) in the late 1960s, and then large-scale integration (LSI) as well as VLSI in the 1970s and 1980s, with tens of thousands of transistors on a single chip (later hundreds of thousands, then millions, and now billion).

Structured VLSI design is a modular methodology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabrics area. This is obtained by repetitive arrangement of rectangular macro blocks which can be interconnected using wiring by abutment. An example is partitioning the layout of an adder into a row of equal bit slices cells. In complex designs this structuring may be achieved by hierarchical nesting.

Structured VLSI design had been popular in the early 1980s, but lost its popularity later because of the advent of placement and routing tools wasting a lot of area by routing, which is tolerated because of the progress of Moore's Law. When introducing the hardware description language KARL in the mid' 1970s, Reiner Hartenstein coined the term "structured VLSI design" (originally as "structured LSI design"), echoing Edsger Dijkstra's structured programming approach by procedure nesting to avoid chaotic spaghetti-structured programs.

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.

II. LITERATURE SURVEY

Since the introduction of integrated circuits (ICs) in 1952 [1] and the realization of the first IC at Texas Instruments in 1958 [2], the last five decades witnessed a phenomenal growth of Silicon (Si) based microelectronics industry. Rapid advancements in this industry are achieved mainly due to continuous scaling or miniaturization of all electronics components (passive and active) integrated on the ICs. IC miniaturization techniques sustained the scaling of complementary metal oxide semiconductor (CMOS) devices and metallic interconnects that used for the connection of device terminals with power supply voltage [3]. Miniaturization in IC technology makes less testing requirements at system level, achieves significant cost savings and faster switching, and leads to compact, low power and highly reliable designs.

As a consequence, it provides faster and improved ICs for high definition digital television, digital receiver, DSP, high speed microprocessor, communication, business transactions, traffic control, space guidance, medical treatment, weather monitoring, internet, and many other commercial, industrial, and scientific enterprises [4]. Further, according to Moore's law, the number of transistors that can be manufactured on a single chip is expected to grow exponentially with time [5]. This prediction turned out to be true as illustrated in Figure 1.1 [6-7]. Figure 1.1 plots the decrement in number of transistors integrated on a single microprocessor chip as a function of time. As can be observed, integration density doubles in every 18 months. To meet the IC density predicted by Moore's law, technology scaling has been pursued aggressively until today since 1970s. The gate length of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is scaled down by a factor of 0.7 in every 2 years, as shown in Figure 1.1. Since 2006, at 65 nm technology node the gate length of a MOSFET has arrived at deep sub-micron/nano range. Today, technology node is 20 nm, and 14 nm has been expected as feature size in the near future [7-8].

Further, scaling down the gate length of CMOS technology in nano ranges results in various critical challenges and reliability issues. One of the issues is increased leakage current which occurs due to various quantum

mechanical tunneling including band-to-band tunneling, direct gate oxide tunneling, and source to drain tunneling [9]. Other issues are large process variations, the effects of crystal misalignments, the randomness of discrete doping, and increment of interface scatterings since the mean free path of electrons becomes comparable to component dimensions [8-9]. These device-level effects cause the current-voltage (I-V) characteristics to be substantially different from well-tempered MOSFET. As a result, researchers have major concerns regarding further improving device performance by scaling down the feature size of MOSFET.

Besides, circuit level effects such as short channel effects, increment in the resistance of metallic on-chip interconnects and power dissipation will surely reduce the suitability of MOSFET for advanced applications in time to come [10-13]. Researchers developed double-gate MOSFETs and FinFET/tri-gate devices [14-15] to reduce short channel effects. In these devices, gate is placed on two/three sides of the channel, which results in better control on the channel and considerable reduction in drain to source sub-threshold leakage current.

III. PROPOSED METHODOLOGY

The core of a TCAM is a TCAM cell array. A typical TG-FinFET-based TCAM cell consists of three major components: (1) an 8T XOR-type CAM cell that not only stores the actual data but also compares the stored data with the search data, (2) the mask cell, which is a 6T SRAM cell used for storing the mask bit to indicate whether this TCAM cell is in the “don’t care” state or not, and (3) an evaluation logic implemented with two TG-Fin FETs controlled by the mask bit and the CAM cell XOR result.

The evaluation logic pulls down the ML when TCAM is mismatched. As evident in Fig. 2, because the conventional TCAM uses the differential SL and differential bit-line schemes for performing the search and read-write operations, each TCAM column contains two SLs (SL,SL) and two bit-lines (BL,BL). In the horizontal dimension, in addition to the ML, each TCAM row also contains the data word-line (DWL) and the mask word-line (MWL) to write the data and mask bit individually. In contrast to the binary CAM cell, which only has “0” and “1” states, a TCAM cell has three states: “0”, “1”, and “don’t care” (or “X”). As shown in Table 2, the TCAM state is determined by the mask data (M) and the TCAM data (D). When M equals 0, representing that the TCAM cell is in the “don’t care” state, the evaluation result is a wild match, regardless of the values for TCAM data (D) and search data (S).

By contrast, when the mask bit is 1, the evaluation result is dependent on the values of D and S. When D is equal to S, the evaluation result is a normal match, and the ML holds its voltage as VDD. When D is not equal to S, which indicates a mismatch, the ML’s signal is pulled down to GND. In many applications, especially in the routing table of a router, the “don’t care” bits continuously appear in some segments. To minimize the leakage power consumption, the aforementioned IG-FinFET is used to design the VoSCT, and one TCAM cell of the VoSCT. In the VoSCT design, the back gates of p-type IG-FinFETs are controlled by VPB, which is set to VDD, and the back gates of n-type IG-FinFETs are controlled by VNB1, which is set to -0.1 V, except for N5, N6, N7, and N8 of the TCAM cell. These four transistors—N5, N6, N7, and N8, which affect the search performance of TCAM, are biased by VNB2.

The search performance can be enhanced when VNB2 is set to 0 V, and the leakage power can be reduced when VNB2 is set to -0.1 V. To maximize the leakage power reduction and minimize the search performance penalty, one TCAM entry is partitioned into several segments. As seen in for an entry consisting of n TCAM cells, the VoSCT partitions it into m segments, and each segment has k ($=n/m$) TCAM cells. For example, when a 32-bit data entry is partitioned into four segments, each segment has eight TCAM cells. Because m segments exist in one TCAM entry, and each segment operates in one of three power modes, the leakage power can be reduced dramatically.

In the VoSCT, a TCAM entry is partitioned into several segments, and each segment operates with one of three power modes, namely, a high-speed mode, low-power mode, and ultra-low-power mode; consequently, the back-gate voltages of IG-FinFETs as well as supply voltages can be self-controlled according to the MSB and LSB cells’ status for each segment.

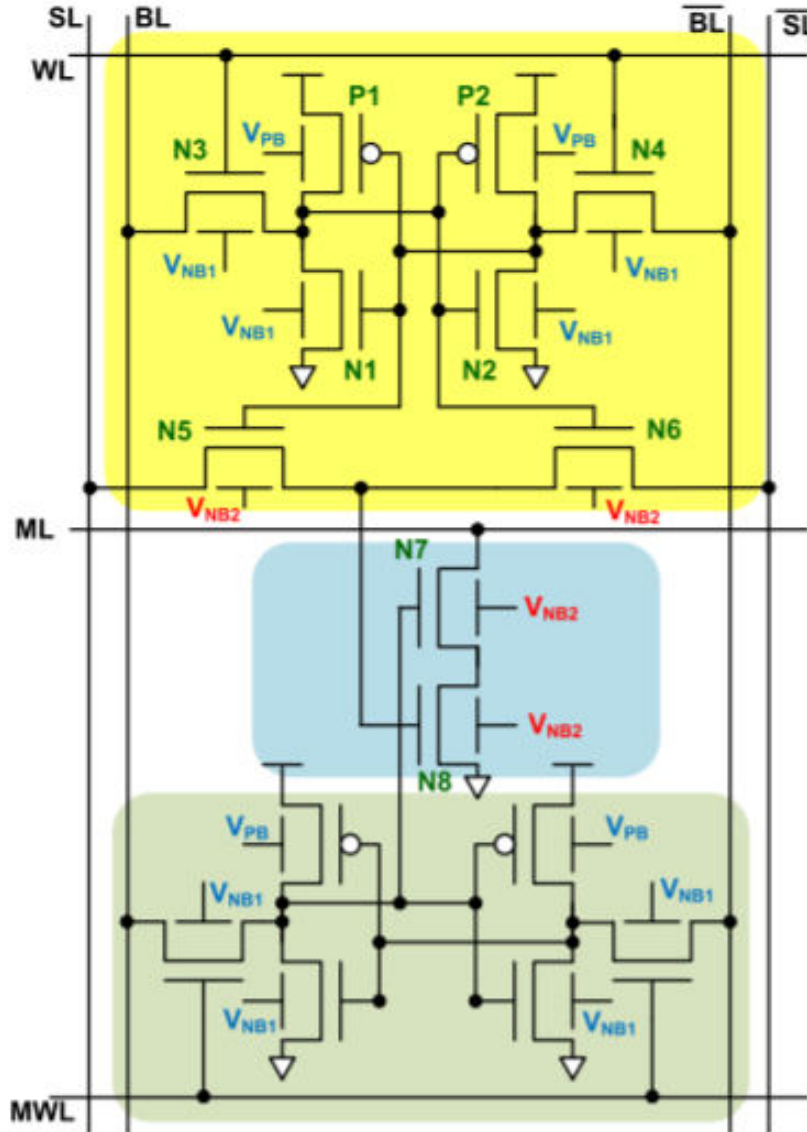


Figure 4.1: IG-FinFET-based TCAM in the VoSCT design.

To minimize the leakage power consumption, the aforementioned IG-FinFET is used to design the VoSCT, and one TCAM cell of the VoSCT. In the VoSCT design, the back gates of p-type IG-FinFETs are controlled by V_{PB} , which is set to V_{DD} , and the back gates of n-type IG-FinFETs are controlled by V_{NB1} , which is set to -0.1 V, except for N5, N6, N7, and N8 of the TCAM cell. These four transistors—N5, N6, N7, and N8, which affect the search performance of TCAM, are biased by V_{NB2} . The search performance can be enhanced when V_{NB2} is set to 0 V, and the leakage power can be reduced when V_{NB2} is set to -0.1 V. To maximize the leakage power reduction and minimize the search performance penalty, one TCAM entry is partitioned into several segments. As seen in for an entry consisting of n TCAM cells, the VoSCT partitions it into m segments, and each segment has k ($=n/m$) TCAM cells.



IV. RESULT & DISCUSSIONS

In our simulation, the Predictive Technology Model (PTM) 32-nm FinFET technology is utilized to implement the traditional TCAM and the VoSCT design. Use of the PTM, which bridges the process and material development and circuit simulation through compact device modeling, is essential for assessing the potential and limits of new technologies and supporting early design prototyping. For the traditional TCAM, $V_{NB} = 0.0$ V and $V_{PB} = 1.0$ V, and for the VoSCT, $V_{NB1} = -0.1$ V and $V_{PB} = V_{DD}$. The value of V_{NB2} depends on the power mode of the corresponding segment, which is listed in Table 4. To achieve voltage self-control, in the VoSCT, a 32-bit TCAM entry is partitioned into m segments, where $m = 2, 4, \text{ and } 8$, denoted as VoSCT_2, VoSCT_4, and VoSCT_8.

V. CONCLUSION

In this paper, the voltage self-controlled technique was used on the TCAM design to reduce the leakage power consumption. In the VoSCT, a TCAM entry is partitioned into several segments, and each segment operates with one of three power modes, namely, a high-speed mode, low-power mode, and ultra-low-power mode; consequently, the back-gate voltages of IG-FinFETs as well as supply voltages can be self-controlled according to the MSB and LSB cells' status for each segment. Based on the PTM 32-nm FinFET technology, the simulation results on real routing table data show that leakage power and total power consumption can be reduced by up to 38% and 21%, with a 9% search delay increase and 4% area overhead. The proposed VoSCT is suitable for those routing tables embedded in routers and gateways, especially for mobile communication environments.

REFERENCES

- [1] Baeg S. Low-power ternary content-addressable memory design using a segmented match line. *IEEE Trans Circuits Syst Regul Pap* 2008;55(6):1485–94 July.
- [2] Cheng YC, Chen JH, Wu TC, Chang YJ. Low leakage mask vertical control TCAM for network router. In: *Proc. IEEE Asia Pacific conference on circuits and systems (APCCAS)*, Oct; 2016. p. 469–72.
- [3] Chang YJ, Liao YH. Hybrid-Type CAM Design for both power and performance efficiency. *IEEE Trans Very Large Scale Integr VLSI Syst* 2008;16(8):965–74 Aug.
- [4] Tsai KL, Chang YJ, Cheng YC. Automatic charge balancing content addressable memory with self-control mechanism. *IEEE Trans Circuits Syst Regul Pap* 2014;61(10):2834–41 Oct.
- [5] Agarwal A, Hsu S, Mathew S, Anders M, Kaul H, Sheikh F, Krishnamurthy R. A 128×128b high-speed wide-AND match-line content addressable memory in 32nm CMOS. In: *Proc. IEEE European solid-state circuits conference (ESSCIRC)*, Sep.; 2011. p. 83–6.
- [6] Chang YJ, Tsai KL, Tsai HJ. Low leakage TCAM for IP lookup using two-side self-gating. *IEEE Trans Circuits Syst Regul Pap* 2013;60(6):1478–86 June.
- [7] Tawfik SA, Kursun V. Low power and stable FinFET SRAM with static independent gate bias for enhanced integration density. In: *Proc. IEEE international conference on electronics, circuits and systems (ICECS)*, Dec.; 2007. p. 443–6.
- [8] Chang MC, He KL, Wang YC. Design of asymmetric TCAM (Ternary Content-Addressable Memory) Cells Using FinFET. In: *Proc. IEEE 3rd global conference on consumer electronics (GCCE)*, Oct.; 2014. p. 358–9.
- [9] Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS), 2015 [Online]. Available: <http://www.itrs2.net/>.
- [10] Cao Y. What is Predictive Technology Model (PTM)? *ACM SIGDA Newslett* 2009;39(3) March.



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