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Design of Low-Power High-Performance 2–4 and 4–16 Mixed-Logic Line Decoders

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ABSTRACT: This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic 2–4 precoders combined with standard CMOS post decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

INTRODUCTION

TATIC cmos circuits are used for the vast majority of logic gates in integrated circuits [1]. They consist of complementary N-type metal-oxide-semiconductor (nMOS) pulldown and P-type metal-oxide semiconductor (pMOS) pullup networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2].

Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines or fewer if the n -bit coded information has unused combinations. The circuits examined here are n -to- m line decoders, which generate the $m = 2^n$ minterms of n input variables. TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count.

An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. Using a complementary input as the propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (AB) or implication (A+ B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A + B) function, either choice is equally efficient.

Finally, when implementing the NAND (A+ B) or NOR (AB) function, either choice results to a complementary propagate signal, perforce. Following a similar procedure with OR gates, a 2–4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well: I0 and I2 are implemented with TGL (using B as the propagate signal), and I1 and I3 are implemented with DVL (using A as the propagate signal). The B inverter can once again be elided. Inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby reducing power dissipation. The two new topologies are named “2–4LP” and “2–4LPI,” where “LP” stands for “low power” and “I” for “inverting.”

II. LITERATURE SURVEY

With the small transistor at their hands, electrical engineers of the 1950s saw the possibilities of constructing far more advanced circuits. As the complexity of circuits grew, problems arose. One problem was the size of the circuit. A complex circuit, like a computer, was dependent on speed. If the components of the computer were too large or the

wires interconnecting them too long, the electric signals couldn't travel fast enough through the circuit, thus making the computer too slow to be effective.

Jack Kilby at Texas Instruments found a solution to this problem in 1958. Kilby's idea was to make all the components and the chip out of the same block (monolith) of semiconductor material. Kilby presented his idea to his superiors, and was allowed to build a test version of his circuit. In September 1958, he had his first integrated circuit ready. Although the first integrated circuit was crude and had some problems, the idea was groundbreaking. By making all the parts out of the same block of material and adding the metal needed to connect them as a layer on top of it, there was no need for discrete components. No more wires and components had to be assembled manually. The circuits could be made smaller, and the manufacturing process could be automated.

From here, the idea of integrating all components on a single silicon wafer came into existence, which led to development in small-scale integration (SSI) in the early 1960s, medium-scale integration (MSI) in the late 1960s, and then large-scale integration (LSI) as well as VLSI in the 1970s and 1980s, with tens of thousands of transistors on a single chip (later hundreds of thousands, then millions, and now billion).

Structured VLSI design is a modular methodology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabrics area. This is obtained by repetitive arrangement of rectangular macro blocks which can be interconnected using wiring by abutment. An example is partitioning the layout of an adder into a row of equal bit slices cells. In complex designs this structuring may be achieved by hierarchical nesting.

III. PROPOSED METHODOLOGY

PTL can realize logic functions with fewer transistors and smaller logical effort than CMOS. However, cascading PTL circuits may cause degradation in performance due to the lack of driving capability. Therefore, a mixed-topology approach, i.e., alternating PTL and CMOS logic, can potentially deliver optimum results. The metrics considered for the comparison are: average power dissipation, worst-case delay and power-delay product (PDP). With continuous sub-micron scaling and low voltage operation, leakage power has become increasingly important as it dominates the dynamic one [12]. In our analysis, both leakage and active currents are considered and the total power dissipation is extracted from spice simulation, measured in nanowatts (nW). Regarding delay, we note the highest value that occurs among all I/O transitions, measured in picoseconds (ps). Finally, PDP is evaluated as average power*max delay and measured in electronvolts.

A 2–4 line decoder generates the 4 minterms D_0 – D_3 of 2 input variables A and B. Its logic operation is summarized in Table I. Depending on the input combination, one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2–4 decoder generates the complementary minterms I_0 – I_3 , thus the selected output is set to 0 and the rest are set to 1.

In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gates whereas an inverting decoder requires 2 inverters and 4 NAND gates both yielding 20 transistors.

4–16 Line Decoder With 2–4 Predecoders A 4–16 line decoder generates the 16 minterms D_0 – D_{15} of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms I_0 – I_{15} . Such circuits can be implemented using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2n predecoded lines that serve as inputs to the final stage decoder [1]. Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates, and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

we perform a variety of BSIM4-based spice simulations on the schematic level, in order to compare the proposed mixed-logic decoders with the conventional CMOS. The circuits are implemented using a 32 nm predictive technology model for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect [11]. For fair and unbiased comparison we use unit-size transistors exclusively ($L_n = L_p = 32$ nm, $W_n = W_p = 64$ nm) for all decoders.

ADVANTAGES

- This technique is to reduce the energy consumption level and to optimize the writing in the D memory functions.

- The proposed system is used to reduce the power consumption level.
- To proposed system is used to reduce the circuit complexity level.

Transistor 2–4 Low-Power Topology: Designing a 2–4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14. Let us assume that, out of the two inputs, namely, A and B, we aim to eliminate the B inverter from the circuit. The D0 minterm (AB) is implemented with a DVL gate, where A is used as the propagate signal. The D1 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. The D2 minterm (AB) is implemented with a DVL gate, where A is used as the propagate signal.

Finally, The D3 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. These particular choices completely avert the use of the complementary B signal; therefore, the B inverter can be eliminated from the circuit, resulting in a 14-transistor topology (9 nMOS and 5 pMOS). Following a similar procedure with OR gates, a 2–4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well: I0 and I2 are implemented with TGL (using B as the propagate signal), and I1 and I3 are implemented with DVL (using A as the propagate signal). The B inverter can once again be elided. Inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby reducing power dissipation. The two new topologies are named “2–4LP” and “2–4LPI,” where “LP” stands for “low power” and “I” for “inverting.”

Transistor 2–4 High-Performance Topology: The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D0 and I3. However, D0 and I3 can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology. The new 15T designs present a significant improvement in delay while only slightly increasing power dissipation. They are named “2–4HP” (9 nMOS, 6 pMOS) and “2–4HPI” (6 nMOS, 9 pMOS), where “HP” stands for “high performance” and “I” stands for “inverting.”

Integration in 4–16 Line Decoders: PTL can realize logic functions with fewer transistors and smaller logical effort than CMOS. However, cascading PTL circuits may cause degradation in performance due to the lack of driving capability. Therefore, a mixed-topology approach, i.e., alternating PTL and CMOS logic, can potentially deliver optimum results. We implemented four 4–16 decoders by using the four new 2–4 as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs.

The new topologies derived from this combination are the following: 4–16LP [Fig. 6(a)], which combines two 2–4LPI predecoders with a NOR-based postdecoder; 4–16HP [Fig. 6(b)], which combines two 2–4HPI predecoders with a NOR-based postdecoder; 4–16LPI [Fig. 6(c)], which combines two 2–4LP predecoders with a NAND-based postdecoder; and, finally, 4–16HPI [Fig. 6(d)], which combines two 2–4HP predecoders with a NAND-based postdecoder. The “LP” topologies have a total of 92 transistors, while the “HP” ones have 94, as opposed to 104 with pure CMOS.

Line Decoder With 2–4 Predecoders A 4–16 line decoder generates the 16 minterms D0–15 of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms I0–15. Such circuits can be implemented using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2n predecoded lines that serve as inputs to the final stage decoder [1]. Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates, and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each. A 4–16 line decoder generates the 16 minterms D0–15 of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms I0–15. Such circuits can be implemented using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2n predecoded lines that serve as inputs to the final stage decoder [1]. Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates, and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

IV. RESULTS AND DISCUSSION

A 4–16 line decoder generates the 16 minterms D0–15 of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms I0–15. Such circuits can be implemented using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2n predecoded lines that serve as inputs to the final stage decoder [1]. Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates, and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each. A 4–16 line decoder generates the 16 minterms D0–15 of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms I0–15. Such circuits can be implemented using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2n predecoded lines that serve as inputs to the final stage decoder [1]. Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates, and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

V. CONCLUSION

To be implemented on layout level, making them suitable for standard cell libraries and RTL design. The metrics considered for the comparison are: average power dissipation, worst-case delay and power-delay product (PDP). With continuous sub-micron scaling and low voltage operation, leakage power has become increasingly important as it dominates the dynamic one [12]. In our analysis, both leakage and active currents are considered and the total power dissipation is extracted from spice simulation, measured in nanowatts (nW). Regarding delay, we note the highest value that occurs among all I/O transitions, measured in picoseconds (ps). Finally, PDP is evaluated as average power*max delay and measured in electronvolts (eV).

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