



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJIRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 11, Issue 8, August 2022

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.118

9940 572 462

6381 907 438

ijirset@gmail.com

www.ijirset.com



Column Section Enabled 10T SRAM Utilizing Shared Diff-VDD Write and Dropped VDD Read for Power Reduction

Desu.Sai Sri Lakshmi, Veruva.Vishnuvardhan

Department of Electronics and Communication Engineering, Specialization: VLSI & ES, QIS College of Engineering and Technology, Prakasam, Ongole, Andhra Pradesh, India

Associate Professor, QIS College of Engineering and Technology, B.Tech(E.C.E , JNTUH)

M.Tech(E.C.E , ES, Vignan University), Ph.D (pursuing), Prakasam, Ongole, A.P, India

ABSTRACT: In recent days, the system's power consumption is important critically in modern VLSI circuits particularly for the low power application. In order to decrease the power, a power optimization technique must be used at various design levels. The low power use of logic cells is a proficient technique for decreasing the circuit level power. Dual Feedback edge triggered Flip Flop (DFET-FF) is considered in the proposed system. In this paper, quadruple cross-coupled storage cells (QUCCE) 10T and 12T are proposed in 130 nm CMOS technology. The QUCCE 10T and 12T are about the minimum critical charge of the conventional 6T, respectively. Compared with most of the considered state-of-the-art SRAM cells, both QUCCE 10T and 12T have comparable or better soft error tolerance, time performance, read static noise margins, and hold static noise margins, and besides, QUCCE 10T also has similar or lower costs in terms of area and leakage power. The QUCCE 10T is designed for high-density SRAMs at the nominal supply voltage. Furthermore, the QUCCE 12T saves more than 50% the read access time compared with most of the referential cells including the 6T, making it suitable for high speed SRAM designs, and it also has the best read margin, except for the traditional 8T, in terms of μ/σ ratio in the near threshold voltage region among all the other considered cells which nearly have no write failure in that region. Hence, the QUCCE 12T is a promising candidate for future highly reliable terrestrial low-voltage applications.

I. INTRODUCTION

Since the technology of complementary metal-oxide semiconductor (CMOS) scaling and low power consumption demand continues to make the Integrated Circuits (ICs) downwards supply voltage, attaining high radiation tolerance which becomes more and more challenging. The supply voltage scaling is regarded as the most effective one for reducing the consumption of power that enables magnitude reductions order once scaled down to the sub threshold region. In the application of space, the power consumption reduction is of most important, particularly once the power budget depends on solar power. Also, several space applications need inconsistent performance, and supply voltage scaling can allow consumption of optimized ICs power functioning in such an applications significantly.

As D flip-flops (DFFs) are the most significant building blocks employed for the realization of these ICs, which in turn makes the DFFs radiation tolerant to be the most significance to decrease the system's total error rate. Two extra access transistors assist in accomplishing the access of secondary cell through read and write actions. Some approaches for decreasing the active power has been recognized, of which clock gating is more predominant. The Clock gating is very beneficial one for the reduction of power consumed by power system. The three gating methods are familiar; the most common is synthesis-dependent, influential clock that allows signals based on the fundamental system logic. Unfortunately, to drive the redundant flip-flops (FFs) it leaves the common clock pulses. A method that depends on data-driven stops utmost of those and provides higher range of power savings, conversely



its implementation is application dependent and vague. A third method named Auto-Gated FFs (AGFF) is simple however produces small power savings comparatively.

D Flip-flops (DFFs) are regarded as the essential building blocks in sequential circuits of CMOS. In a sequential CMOS circuits, the major radiation source of induced errors are single event upsets (SEUs) and the techniques based on SEU mitigation depend on supply voltages frequently being as high as probable so as to accomplish superlative promising SEU tolerance.

II. LITERATURE SURVEY

Today's consumer needs small size, high speed, optimized power devices and more functionality. The Consumer demands a smaller battery size with longer life. The dissipation of Power is the major drawback of silicon computing devices at present. The Reduction of power has other favorable effects in addition, it imply less rigorous requirements for enhanced endurance, longer self-sufficiency, cooling in the battery operated devices case and lower power costs perceptibly. In the digital circuit the consumed Power is of two kinds: Dynamic power and Static power. Static power comprises of dissipated power because of currents leakage while dynamic power consists of short circuit power and capacitive switching power.

The difference in integration time occurrence involving similar input signals might lead to the differences to subsist in the output signal. In the meantime, in conservative high- range of dynamic system, clock signal is offered as an input to the entire pixels in spite of input signal.

D Flip-flops (DFFs) are fundamental building blocks in sequential CMOS circuits. In sequential CMOS circuits, single event upsets (SEUs) are the main source of radiation induced errors and SEU mitigation techniques often rely on supply voltages being as high as possible in order to attain the best possible SEU tolerance. As supply voltages scale down, internal nodes become more susceptible to SEUs due to the reduction of the critical charge (Q_{crit}) of the internal nodes . On the other hand, the most direct and dramatic means of reducing the power consumption of an integrated circuit (IC) is by reducing the supply voltage. Power consumption savings up to several orders of magnitude have been achieved, given that the transistors are operated in the subthreshold region . Another benefit of low supply voltage operation is that the Total Ionizing Dose(TID) induced leakage decreases . Low TID induced leakage is important for realizing both low power and reliable ICs. To the authors' knowledge, this work is the first to investigate the common impact of temporal and spatial hardening techniques on the SEU sensitivity of DFFs, as a function of a wide supply voltage range (180 mV to 1 V). Our results show that temporal hardening has higher impact on the SEU sensitivity of the proposed DFFs at supply voltages above 500 mV, while spatial hardening has higher impact on the SEU sensitivity at supply voltages below 500 mV. Furthermore, we also show that DFFs operated at low supply voltages can have good SEU tolerance at the same time as having increased energy efficiency. One of the proposed DFFs operated at a supply voltage of 500 mV without experiencing any SEUs, and while being 72% more energy efficient than a Dual Interlocked Storage Cell (DICE) DFF at 1 V supply voltage. The proposed DFF topology is implemented using three different configurations in terms of delay of the temporal elements and separation of the sensitive nodes. The DFFs are compared in terms of area, clk-to-Q delay, setup time, energy per transition and maximum frequency. Furthermore, a DICE-based DFF is also included in this paper in order to serve as a reference DFF. Spectre simulations are used for evaluating the DFF performance and heavy ion radiation testing is used for evaluating the SEU susceptibility of the DFFs.

III. PROPOSED METHODOLOGY

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip. With the small transistor at their hands, electrical engineers of the 1950s saw the possibilities of constructing far more advanced



circuits. As the complexity of circuits grew, problems arose. One problem was the size of the circuit. A complex circuit, like a computer, was dependent on speed. If the components of the computer were too large or the wires interconnecting them too long, the electric signals couldn't travel fast enough through the circuit, thus making the computer too slow to be effective.

Jack Kilby at Texas Instruments found a solution to this problem in 1958. Kilby's idea was to make all the components and the chip out of the same block (monolith) of semiconductor material. Kilby presented his idea to his superiors, and was allowed to build a test version of his circuit. In September 1958, he had his first integrated circuit ready. Although the first integrated circuit was crude and had some problems, the idea was groundbreaking. By making all the parts out of the same block of material and adding the metal needed to connect them as a layer on top of it, there was no need for discrete components. No more wires and components had to be assembled manually. The circuits could be made smaller, and the manufacturing process could be automated. From here, the idea of integrating all components on a single silicon wafer came into existence, which led to development in small-scale integration (SSI) in the early 1960s, medium-scale integration (MSI) in the late 1960s, and then large-scale integration (LSI) as well as VLSI in the 1970s and 1980s, with tens of thousands of transistors on a single chip (later hundreds of thousands, then millions, and now billion).

The input signal is one bit value from the search data register i.e. the input word to be compared against all the values stored in CAM arrays or the value to be stored in the CAM cell. Cell enable signal allows or prevents comparison

i.e. matching process meaning XOR-ing the stored bit value in the Flip-flop and the input bit. It not only requires huge memory area but unnecessary power is lost in bit comparisons even if pre-charge or pipeline method is used. For example, for fixed source IP and destination IP addresses computation will be performed over all the first 64 bits regardless of residual bit fields. In that regard an improvement can be achieved by statistical pre-computation along word's bits. Pre-computation stores some extra bits derived from the stored word and it is used in the initial search before the search of main word.

Selective pre-charge scheme basically divides the match line in two segments. In general following the same concept it can be divided in many number of segments thus forming a pipeline. If any stage is missed the subsequent stages are shut off resulting in power saving. The drawback of this scheme are the increased latency and area overhead due to the pipeline stages. Here is shown a power saving design sacrificing the speed i.e. increased delay but retaining the same circuit area. The basic idea behind the concept is the segmentation in the match line in a manner that every CAM cell forms a segment for its own as it is presented.

The main benefit for the proposed scheme comes from implementation with CAM cells. Namely, the output of a cell is simply the cell enable signal for the successive bit comparison thus mitigating extra gates to transfer the results from the cells. The disadvantage is increased propagation delay that comes from the three-state buffer and XNOR gate at each cell. Typical CAM consists of words length ranging from 36 to 144 bits and in practice it should be acceptable delay value. It should be noted that one cell segmentation approach presented here is a conceptual view rather than real power saving scheme that can be achieved on circular level.

Typical Single Event Effects (SEE) are single event transients (SET) and SEUs. SETs are transient voltage fluctuations which are induced by charge collection, as a result of an inbound particle interacting with the sensitive nodes (typically reverse biased source/drain), in a transistor [8]. These voltage fluctuations, although short in duration, can propagate to storage elements and cause an erroneous latched logic state, resulting in a SEU. A SEU can be defined as a change in the logic state of a memory element from a logic one to a logic zero or vice-versa. SEUs typically occur when inbound particles alter the voltage in sensitive nodes of memory elements in such a way that it results in a bit error. SEUs are non-destructive events; therefore, the affected logic can be rewritten or reset to regain proper operational behavior. Based on the nature of the SEEs described here, it is apparent that SEUs are a highly relevant topic for memory elements such as Static Random Access Memory (SRAM), latches and flip-flops.

An ultra low power and high sensitivity of joint clock gating dependent dual feedback edge triggered flip flop is designed. This in turn facilitates the error reduction in the concluding output signal. The implementation of flip flop based on both feedback and triggering process is more effective in the elimination of error occurrence. Also,

asynchronous clock gating techniques usage is introduced for the power consumption reduction. The proposed system utility is then demonstrated by the post-layout simulations.

The QUCCE 10T memory cell has four storage nodes A, Q, QN and B. The output nodes, Q and QN, are connected to the bit lines BL and BLB through pass gates N5 and N6 respectively. The two access transistors N5 and N6 are controlled by word line WL and will be enabled when WL is at high logic state. The stored '0' state for the proposed QUCCE 10T cell is taken into consideration. The logic states of nodes A, Q, QN and B are '1', '0', '1' and '0' respectively. In hold mode, the logic state of word line (WL) is set to be '0' and thus the two pass gates N5 and N6 are disabled. Each of the four nodes is determined by an NMOS transistor and a PMOS transistor in series. Transistors P1, N2, P3 and N4 are turned on while transistors N1, P2, N3 and P4 are turned off. For read operation, two bit-lines BL and BLB will be pre-charged to supply voltage in a first step and WL is set to be '1' state to activate access transistors N5 and N6 afterwards. As for the 'read 0' operation, BLB will maintain its original states without being changed, but BL will be discharged because N5 and N2 are turned on, creating a path from BL to ground. The voltage difference obtained from BL and BLB will be amplified by a differential sense amplifier and output the data stored in the memory cell. In order to obtain stable read operation, CR, the cell ratio defined as $(WN2/LN2)/(WN5/LN5)$ or $(WN3/LN3)/(WN6/LN6)$, should be set properly to acquire good RSNM and ensure integrated density at the same time. To change the original stored data of the QUCCE 10T cell, WL and BL are set to be '1' while BLB is set to be '0' to carry out the 'write 1' operation. Once the access transistors N5 and N6 are activated, BLB pulls down the potential at node QN through transistor N6 below the threshold voltage (V_{TH}) of transistor N2 resulting in N2 being turned off, and BL pulls up the potential at node Q through transistor N5 towards $(V_{DD}-V_{THn})$.

Meanwhile, the crosscoupled latch structure composed of transistor N2 and N3 will further amplify the voltage difference between node Q and QN, accelerating the buildup of voltage difference. Notice that N6 has to be stronger than P3 to realize this. The related pull-up ratio, PR1, is defined as $(WP2/LP2)/(WN5/LN5)$ or $(WP3/LP3)/(WN6/LN6)$. Furthermore, another cross-coupled latch structure composed of transistor P3 and P4 will amplify the voltage difference between node QN and B. In order to pull up the potential at node B, P4 has to be stronger than N4. The related pull-up ratio, PR2, is defined as $(WP4/LP4)/(WN4/LN4)$ or $(WP1/LP1)/(WN1/LN1)$. Considering PMOS transistor has smaller carrier mobility than NMOS transistor, to get a stronger P4 or P1 will cost more area overhead. In a successful write operation, nodes Q and QN will eventually be modified to new data. Transistors N1, P2, N3, and P4 are turned on, and transistors P1, N2, P3, and N4 are turned off. Nodes A, Q, QN and B are set to be '0', '1', '0' and '1' respectively.

ADVANTAGES

This technique is to reduce the energy consumption level and to optimize the writing in the D memory functions.

The proposed system is used to reduce the power consumption level.

To proposed system is used to reduce the circuit complexity level.

The proposed unit cell circuit employing the asynchronous clock-gating technique. As previously mentioned, the capacitor-reset block was designed with the DET-DFF. The proposed clock-gating technique can be employed to control the use of clock signals asynchronously in accordance with the input-signal current. The two clock-gating control signals (V_{gain} and V_{int}) are generated internally within the ROIC. The switch-enable signal (V_{gain}) is used to distinguish the low-gain mode from the high-gain mode at the system level, as shown in Table 1. When the switch-enable signal is high (i.e., $V_{gain} = 1$), multiple reset control of the 400-fF integration capacitor is performed. The integration-control signal (V_{int}) is used to control the integration time for all pixels within ROIC identically. When the integration-control signal is low (i.e., $V_{int} = 0$), photocurrent integration is performed. Likewise, if the switch-enable signal is low (i.e., $V_{gain} = 0$) or the integration-control signal is high (i.e., $V_{int} = 1$), the use of the clock signal becomes unnecessary. In this way, the proposed clock-gating technique serves to reduce the ROIC power consumption.

In the layout design, the proposed circuit containing multiple functions cannot be easily integrated into one pixel with a pixel size of $15 \mu\text{m} \times 15 \mu\text{m}$. This pixel size is the most commonly used size in commercial MWIR

detectors. As a result, four neighboring pixels (2×2 pixels) share the proposed unit cell circuit and the size of the unit cell circuit will subsequently be $30 \mu\text{m} \times 30 \mu\text{m}$. In addition, the four neighboring pixels and the proposed unit cell circuit are connected via the indium bump. The signal level at the end of the integration period is maintained, and the same is sent to the system during the read period. In the case of the high-gain mode, the clock-signal input (Vclk in) is deactivated during one frame.

In the case of the high-dynamic-range (HDR) mode with one reset, when the switch-enable signal is high (i.e., $V_{\text{gain}} = 1$), the clock-signal input (Vclk in) to the capacitor-reset block is activated, and a multiple-reset control of the 400-fF integration capacitor is performed. Additionally, when the integration-control signal is high (i.e., $V_{\text{int}} = 1$), the clock-signal input (Vclk in) to the capacitor-reset block is deactivated.

III. RESULTS AND DISCUSSION

To verify the efficiency of the clock-gating technique, the power consumption by the proposed 10T SRAM cell design based on clock gating technique, which employs the asynchronous clock-gating technique, was compared to those by the conventional high-dynamic-range. Table lists the results obtained upon comparison of the power consumed by the proposed with that consumed by conventional array. In this study, the effect of only the capacitor-reset blocks equipped with the clock-gating circuit was considered for power consumption comparison.

In this paper, we propose two quadruple cross-coupled latch-based SRAM bit-cells for highly reliable terrestrial applications. Compared with most of the considered SRAM cells, the proposed QUCCE 10T and 12T have comparable or better soft error tolerance, RSNMs, and HSNMs at nominal supply voltage. With regard to the robustness, the QUCCE 10T and 12T are about $2\times$ and $3.4\times$ the minimum critical charge of the conventional 6T respectively. However, the QUCCE 10T features a high write error rate in near threshold voltage region, which means it cannot be employed in low voltage applications even though it has high read stability. In addition, the QUCCE 10T has comparable or lower area overhead compared with most of the considered state-of-the-art soft error tolerant SRAM bit-cells. Hence, the QUCCE 10T is a good choice for highly reliable high-density terrestrial applications at nominal supply voltage. QUCCE 12T exhibits about 56% area and 50% leakage power penalties over the conventional 6T. Higher radiation tolerance may however be achieved by separating the sensitive nodes even further. Nevertheless, compared with most of the referential cells including the 6T, the QUCCE 12T saves more than 50% the read access time, making it suitable for high speed SRAM designs, and it also has the best read margin.

REFERENCES

- [1] Y. Reibel, L. Espuno, R. Taalat, A. Sultan, P. Cassaigne, and N. Matallah, "High performance infrared fast cooled detectors for missile applications," Proc. SPIE, vol. 9819, 2016, Art. no. 98190I.
- [2] R. Fraenkel, J. Haski, U. Mizrahi, L. Shkedy, and I. Shtrichman, "Cooled and uncooled infrared detectors for missile seekers," Proc. SPIE, vol. 9070, 2014, Art. no. 90700P.
- [3] B. K. McComas, "The art and science of missile defense sensor design," Proc. SPIE, vol. 9085, 2014, Art. no. 90850F.
- [4] O. Neshet, S. Elkind, and T. Markovitz, "Advantages of SCD detectors for missile warning system applications," Proc. SPIE, vol. 5612, pp. 32–41, 2004.
- [5] C. Y. Kim, D. H. Woo, and H. C. Lee, "High-dynamic-range ROIC with asynchronous self-controlled two-gain-mods for MWIR focal plane arrays," IEEE Sensors J., vol. 19, no. 2, pp. 615–622, Jan. 2019.
- [6] M. Afghahi and J. Yuan, "Double edge-triggered D-flip-flops for high-speed CMOS circuits," IEEE J. Solid-State Circuits, vol. 26, no. 8, pp. 1168–1170, Aug. 1991.
- [7] J. S. Wang, "A new true-single-phase-clocked double-edge-triggered flip-flop for low-power VLSI designs," in Proc. Int. Symp. IEEE Circuits Syst., 1997, vol. 3, pp. 1896–1899.



- [8] C. C. Yu and K. T. Chen, "A novel design of low power double edge-triggered flip-flop," in Proc. 5th Int. Conf. BioMed. Eng. Inf., 2012, pp. 1363–1366.
- [9] E. G. Friedman, Clock Distribution Networks in VLSI Circuits and Systems. New York, NY, USA: IEEE Press, 1995.
- [10] V. G. Oklobdzija, V. M. Stojanovic, D. M. Markovic, and N. M. Nedovic, Digital System Clocking: High-Performance and Low-Power Aspects. New York, NY, USA: Wiley-Interscience, 2003.
- [11] H. F. Benz, J. W. Gambles, S. R. Whitaker, K. J. Hass, G. K. Maki, and P.-S. Yeh, "Low power radiation tolerant vlsi for advanced spacecraft," in Proc. IEEE Aerospace Conf., 2002, vol. 5, pp. 2401–2406.
- [12] G. K. Maki and P. S. Yeh, "Radiation tolerant ultra low power cmos microelectronics: Technology development status," in Proc. Earth Science Technology Conf., Collage Park, MD, USA, 2002.
- [13] L. B. Freeman, "Critical charge calculations for a bipolar sram array," IBM J. Res. Develop., vol. 40, no. 1, pp. 119–129, Jan. 1996.
- [14] S. M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, "An analytical model for soft error critical charge of nanometric srams," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 9, pp. 1187–1195, Sep. 2009.
- [15] T. Heijmen, D. Giot, and P. Roche, "Factors that impact the critical charge of memory elements," in Proc. 12th IEEE Int. On-Line Testing Symp., 2006.
- [16] H. Soeleman, K. Roy, and B. C. Paul, "Robust subthreshold logic for ultra-low power operation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 9, no. 1, pp. 90–99, Feb. 2001.
- [17] M. A. Xapsos, G. P. Summers, and E. M. Jackson, "Enhanced total ionizing dose tolerance of bulk CMOS transistors fabricated for ultra-low power applications," IEEE Trans. Nucl. Sci., vol. 46, no. 6, pp. 1697–1701, Dec. 1999.
- [18] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 583–602, Jun. 2003.
- [19] N. A. Dodds, J. M. Hutson, J. A. Pellish, R. A. Reed, H. S. Kim, M. D. Berg, M. R. Friendlich, A. M. Phan, C. M. Seidleck, M. A. Xapsos, X. Deng, R. C. Baumann, R. D. Schrimpf, M. P. King, L. W. Massengill, and R. A. Weller, "Selection of well contact densities for latchup-immune minimal-area ics," IEEE. Trans. Nucl. Sci., vol. 57, no. 6, pp. 3575–3581, Dec. 2010.
- [20] T.-H. Chen, J. Chen, L. T. Clark, J. E. Knudsen, and G. Samson, "Ultra-low power radiation hardened by design memory circuits," IEEE Trans. Nucl. Sci., vol. 54, no. 6, pp. 2004–2011, Dec. 2007



INNO SPACE
SJIF Scientific Journal Impact Factor
Impact Factor: 8.118



ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 **9940 572 462**  **6381 907 438**  **ijirset@gmail.com**



www.ijirset.com

Scan to save the contact details